# PG2L50H_FBG484

(PK04005, V1.1)

(30.06.2022)

# Revisions History

## Document Revisions

| Version | Date of Release | Revisions |
|---|---|---|
| V1.1 | 30.06.2022 | Initial release. |
| | | |

# About this Manual

## Terms and Abbreviations

| Terms and Abbreviations | Meaning |
|---|---|
| POD | Package Outline Drawing |
| | |

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# Chapter 1 Introduction to Packaging

PG2L50H_FBG484 uses a Wire-Bond BGA type of packaging. Package size: 23x23mm; Number of balls: 484; Ball pitch: 1.0mm; Maximum package thickness: 2.33mm.

# Chapter 2 Package Dimension and Pin Definitions

## 2.1 Package Dimension

Table 2-1 Dimensional Values

Unit: millimeter

| Dimension Symbol | Value | | | Dimension Symbol | Value | | |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | Min. | Typ. | Max. |
| A | 2.07 | 2.20 | 2.33 | E1 | - | 21.00 | - |
| A1 | 0.37 | 0.47 | 0.57 | E2 | 19.30 | 19.50 | 19.70 |
| A2 | 1.12 | 1.17 | 1.22 | E3 | - | 14.70 | - |
| b | 0.50 | 0.60 | 0.70 | e | - | 1.00 | - |
| c | 0.51 | 0.56 | 0.61 | aaa | - | 0.20 | - |
| D | 22.80 | 23.00 | 23.20 | ccc | - | 0.20 | - |
| D1 | - | 21.00 | - | ddd | - | 0.15 | - |
| D2 | 19.30 | 19.50 | 19.70 | eee | - | 0.25 | - |
| D3 | - | 14.70 | - | fff | | 0.10 | |
| E | 22.80 | 23.00 | 23.20 | Ball Diam | | 0.60 | |

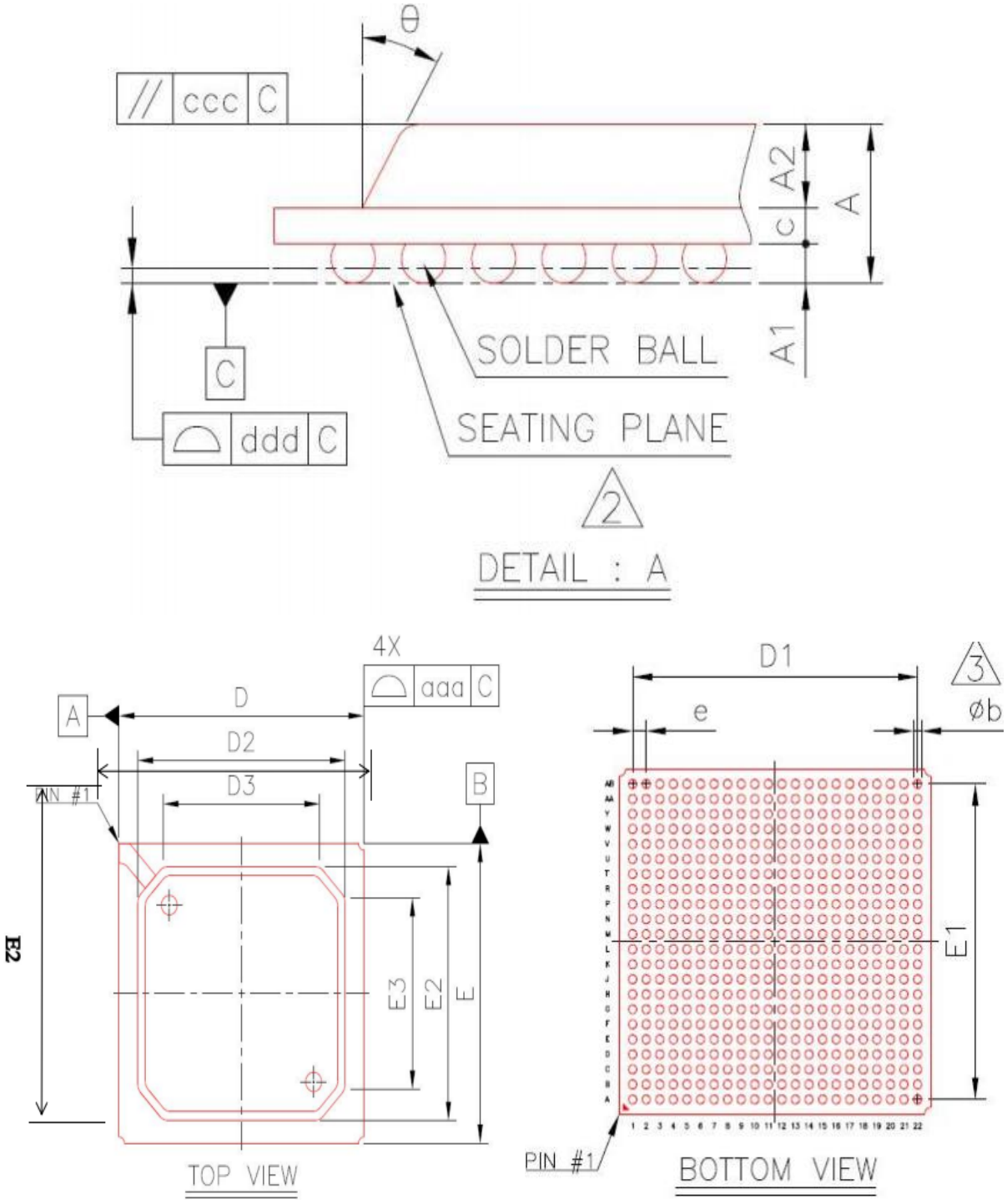


Figure 2-1 Package Outline Dimension (POD)

## 2.2 Pin Definitions

PG2L50H_FBG484 has 250 user IOs.

Table 2-2 Product Pin Definitions

| PIN Name | PIN Type | PIN Direction | PIN Description |
|---|---|---|---|
| **General PIN** | | | |
| DIFFIO_XX_GY_NN[P,N] | General | Input/Output | General pin;<br>(1) "DIFFIO" indicates the pin supports differential input/output and can be used for transmitting and receiving LVDS signals;<br>(2) " XX " indicates bank numbers, which can be L3, L4, L5, R4, R5;<br>(3) " G " indicates belonging to a memory group;<br>(4) " Y " indicates the group number in a bank, each of which contains four groups;<br>(5) "NN" indicates the sequence number of programmable IO pairs in a bank, increasing from 0, a bank contains 24 difference pairs;<br>(6) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end;<br>During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.<br>During configuration, all general pins remain in Tri-state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. |
| SIO_XX_NN | General | Input/Output | General pin;<br>(1) " SIO " indicates the pin only supports single ended input/output;<br>(2) " XX " indicates bank numbers, which can be L3, L4, L5, R4, R5;<br>(3) "NN" indicates the sequence number of programmable IO in a bank, increasing from 0, a bank contains 2 single ended IOs;<br>During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.<br>During configuration, all general pins remain in Tri-state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. |
| **Configuration PIN** | | | |
| INIT_FLAG_N | Dedicated | Bidirectional (open-drain) | Initialization and configuration status dedicated pin:<br>When it is low, it indicates that the FPGA is being initialized (clear configuration memory) or a configuration error has occurred.<br>The pin has an internal weak pull-up resistor that is enabled during configuration;<br>When the FPGA powers up completion, the pin is driven to low level. Once the FPGA completes initialization, the pin is released. During the power up and initialization process, this pin can accept an external low-level input to delay the configuration process. |

| PIN Name | PIN Type | PIN Direction | PIN Description |
|---|---|---|---|
| | | | When the FPGA detects high level input on this pin after initialization, the FPGA starts the configuration process. During configuration, this pin serves as an output for the configuration error indication state, low level indicates that an error occurred.<br>This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K.<br>After the configuration is complete, user can configure weak pull-up or float state for this pin. |
| CFG_DONE | Dedicated | Bidirectional (open-drain) | Dedicated configuration status pin, built in weak pull-up resistor about 10K.<br>Output as the configuration completion indicator, high level indicates that the configuration is complete. This pin is an open-drain output. When the FPGA powers up completion, the pin is driven to low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.<br>After the configuration is complete, the pin can be driven externally to low level, Once the internal start-up timing finds that the external DONE pin is low and the internal start-up circuit stops until the external pin is high.<br>After the configuration is complete, user can configure weak pull-up or float state for this pin. |
| RSTN | Dedicated | Input | Dedicated configuration reset pin, built in weak pull-up resistor and always effective.<br>For restarting configuration logic and configuration memory, active-low.<br>When this pin is low, the FPGA configuration memory is emptied and a new configuration process begins. The configuration logic reset begins with the falling edge of the pin, and the configuration process begins with the rising edge of the pin.<br>This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K.<br>Keeping this pin low during power up does not put the FPGA configuration logic in a reset state.<br>After the configuration is complete, user can configure weak pull-up or float state for this pin. |
| CFG_CLK | Dedicated | Input/Output | Configuration clock pin. Except for the JTAG configuration mode, the configuration process of the FPGA is synchronize by this clock in other modes.<br>In the slave SPI, slave serial and slave parallel configuration modes, the pin serves as a clock input to obtain configuration data from external sources.<br>In the master SPI configuration mode, the pin serves as a clock output to obtain configuration data from external sources and an external pull-up resistor of 1K is required.<br>When the clock is not needed (such as in the JTAG mode), this pin is in the High-Z state.<br>After the configuration is complete, user can configure weak pull-up or float state for this pin. |
| TCK | Dedicated | Input | Test clock input pin compliant with IEEE STD 1149.1 and provides a clock for the JTAG chain of the FPGA.<br>Internal weak pull-up resistor is connected to VCCIOCFG and always effective. |
| TMS | Dedicated | Input | Dedicated JTAG test mode selection input pin. |

| PIN Name | PIN Type | PIN Direction | PIN Description |
|---|---|---|---|
| | | | Internal weak pull-up resistor is connected to VCCIOCFG and always effective. |
| TDI | Dedicated | Input | Dedicated JTAG test data input pin.<br>Internal weak pull-up resistor is connected to VCCIOCFG and always effective. |
| TDO | Dedicated | Input | Dedicated JTAG test data output pin<br>Internal weak pull-up resistor is connected to VCCIOCFG and always effective. |
| MODE_2 | Dedicated | Input | Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K,or connected to VSS via an external pull-down resistor of no more than 1K. |
| MODE_1 | Dedicated | Input | Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K,or connected to VSS via an external pull-down resistor of no more than 1K. |
| MODE_0 | Dedicated | Input | Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K,or connected to VSS via an external pull-down resistor of no more than 1K. |
| SCBV | Dedicated | Input | The pin is always effective on BANKCFG, but only on BANK which the multiplexing configuration pins is located during configuration.<br>When the voltage of VCCIOCFG is 2.5V or 3.3V, the pin must be connected to high level and can be connected directly to the VCCIOCFG. When the voltage of VCCIOCFG is 1.8V or lower, the pin must be connected to low level and can be connected directly to the ground.<br>Note: The pin must be used in conjunction with the software, and the SCBV selection in the bitstream setting must be consistent with the hardware setting. For details about the SCBV pin pull-up/pull-down level corresponds to the configured BANK power, see “UG040012_Logos2 Family Hardware Design Guide”. |
| FCS_N | Multiplexed | Output | Multi-function configuration pin, used for the Master SPI configuration mode.<br>(1) In the Master SPI X1, X2 and X4 modes, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K.<br>(2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.<br>(3) After the configuration is complete, the pin serves as a general pin. |
| MOSI_D0 | Multiplexed | Input/Output | Multi-function configuration data pin.<br>(1) “MOSI”, in the master SPI X1 mode; this pin used for serial data output and connects to the data input pin of the external SPI flash (such as DQ0,D,SI,IO0, etc). After the command and address are sent to the external SPI flash, the pin output high-Z or weak pull-up, depending on the state of the IO_STATUS_C |

| PIN Name | PIN Type | PIN Direction | PIN Description |
|---|---|---|---|
| | | | pin.<br>(2) In the master SPI X2, X4 and X8 modes, the pin is bidirectional data port, as command and address output to the external SPI flash. Receive the lowest bit data from the external SPI flash. The pin connects to the bidirectional data pin of the external SPI flash (such as DQ0,D,SI,IO0, etc).<br>(3) " D0" , in the slave parallel mode, this pin serves as the D[0] bit of the data bus.<br>(4) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state.<br>(5) After the configuration is complete, the pin serves as a general pin. |
| MISO_D1_DI | Multiplexed | Input/Output | Multi-function configuration data pin.<br>(1) In the master SPI X1 mode, "MISO" serves as data input and connects to the data output pin of the external SPI flash (such as DQ1,Q,SO,IO1, etc).<br>(2) In the master SPI X2, X4 and X8 modes, "D1" connects to the second serial data output pin of the external SPI flash (such as DQ1,Q,SO,IO1, etc).<br>(3) In the slave parallel mode, this pin serves as the D[1] bit of the data bus.<br>(4) In the slave serial mode, "D1" serves as data input pin.<br>(5) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. In the other configuration modes(such as JTAG), the state on the pin is ignored<br>(6) After the configuration is complete, the pin serves as a general pin. |
| D[2, 3] | Multiplexed | Input/Output | Multi-function configuration data pin.<br>(1) In the master SPI X4 and X8 modes, serve as data input and connects to the data output pin of the external SPI flash. "D2" connects to the third bit data output pin of the external SPI flash (such as DQ2,W#, WP#,IO2, etc). "D3" connects to the fourth bit data output pin of the external SPI flash (such as DQ3, HOLD#, IO3, etc). These pins should be connected to VCCIO via an external weak pull-up resistor of 4.7K.<br>(2) In the slave parallel mode, these pins serve as the D[3:2] bits of the data bus.<br>(3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state.<br>(4) After the configuration is complete, these pins serve as general pins. |
| D[4, 5 , 6, 7] | Multiplexed | Input/Output | Multi-function configuration data pin.<br>(1) In the master SPI X8 mode, connect to the second flash in the same way as D[3:0].<br>(2) In the slave parallel mode, these pins serve as the D[7:4] bits of the data bus.<br>(3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state.<br>(4) After the configuration is complete, these pins serve as general pins. |
| D[8, …, 15] | Multiplexed | Input/Output | Multi-function configuration data pin.<br>(1)In the slave parallel X16 and X32 modes, serve as |

| PIN Name | PIN Type | PIN Direction | PIN Description |
|---|---|---|---|
| | | | the D[15:8] bits of the data bus.<br>(2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state.<br>(3) After the configuration is complete, these pins serve as general pins. |
| D[16, …,31]_A[0, …,15] | Multiplexed | Input/Output | Multi-function configuration data pin.<br>(1) In the slave parallel X32 mode, serve as the D[31:16] bits of the data bus.<br>(2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state.<br>(3) After the configuration is complete, these pins serve as general pins. |
| A[16,…,28] | Multiplexed | Output | Multi-function configuration pin.<br>(1) During initialization, these pins not be used and serve as general pins in a high-Z or weak pull-up state.<br>(2) After the configuration is complete, these pins serve as general pins. |
| CS_N | Multiplexed | Input | Multi-function configuration pin. For chip select input. Active low.<br>(1) When it is low level, this pin enables the slave parallel mode configuration interface. In the slave parallel configuration mode, the external controller can select the slave parallel bus of the FPGA by controlling this pin. Or this pin connected to the previous FPGA CSO_DOUT pin in the slave parallel configuration chain.<br>(2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state.<br>(3) After the configuration is complete, the pin serves as a general pin. |
| RWSEL | Multiplexed | Input | Multi-function configuration pin. For selecting the read/write input in the slave parallel configuration mode (high for read and low for write).<br>(1) When it is high level, the slave parallel configuration mode reads data from the data bus.<br>(2) When it is low level, the slave parallel configuration mode writes data to the data bus.<br>(3) Read and write can be switched only when CS_N is high level.<br>(4) After the configuration is complete, the pin serves as a general pin.<br>(5) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. |
| CSO_DOUT | Multiplexed | Output(OD), Output | Multi-function configuration pin. Needed for cascade.<br>(1) In the master SPI X1 mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state.<br>(2) In the slave serial configuration mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. |

| PIN Name | PIN Type | PIN Direction | PIN Description |
|---|---|---|---|
| | | | (3) In the slave parallel cascade configuration mode, this pin serves as a chip select signal open-drain output, connects to downstream chip CS_N pin and should be connected to VCCIO via an external pull-up resistor of 330Ω.<br>(4) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. |
| VS[0 , 1] | Multiplexed | Output | Multi-function configuration pin.<br>After the configuration is complete, these pins serve as general pins. |
| IO_STATUS_C | Multiplexed | Input | Multi-function configuration pin, used for controlling whether the weak pull-up resistors for all general pins are enabled during the configuration process.<br>(1) When it is set to "0", the internal pull-up resistors for all general pins are enabled.<br>(2) When it is set to "1", the internal pull-up resistors for all general pins are disabled.<br>(3)It is recommended that the pin connects to VCCIO via an external weak pull-up resistor.<br>(4)The pin can connect to VCCIO or VSS, either directly or via an external resistor of no more than 1K.<br>(5) This pin must not be left floating before or during configuration. |
| ECCLKIN | Multiplexed | Input | The external clock input for the Master configuration mode, which is an optional external clock input to the configuration logic.<br>(1) In the master SPI mode, the FPGA can select this clock input as the configuration clock for the configuration logic. This clock can be divided (Depends on the settings in the bitstream) and output from the CFG_CLK pin.<br>(2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. |
| BFOE_N | Multiplexed | Output | Multi-function configuration pin.<br>After the configuration is complete, the pin serves as a. general pin. |
| BFWE_FCS2_N | Multiplexed | Output | Multi-function configuration pin used for the master SPI X8 configuration modes.<br>(1) In the Master SPI X8 mode, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K.<br>(2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state.<br>(3) After the configuration is complete, the pin as a general pin. |
| BADRVO_N | Multiplexed | Output | Multi-function configuration pin.<br>After the configuration is complete, the pin serves as a. general pin. |
| **Clock PIN** | | | |
| GMCLK | Multiplexed | Input | Multiplexing global multi-regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL, PPLL, and also drive the multi-regional clock buffer. When not used as clock input, these pins serve as general pins, and when the differential pair is |

| PIN Name | PIN Type | PIN Direction | PIN Description |
|---|---|---|---|
| | | | connected to a single ended clock source, only the positive end of the differential pair needs to be connected. When these pins serve as single regional clock sources, they are able to drive all the IO clock buffers and regional clock buffers of the BANK. |
| GSCLK | Multiplexed | Input | Multiplexing global single regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL and PPLL. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. They are able to drive all the IO clock buffers and regional clock buffers of the BANK. |
| **Memory Interface PIN** | | | |
| DQS | Multiplexed | N/A | DDR DQS PIN, each memory group contains two pins. |
| **Reference PIN** | | | |
| VREF | Multiplexed | N/A | Input reference voltage pins. When not used as external reference voltage pins, these pins serve as general pins, |
| **Power/ Ground PIN** | | | |
| VCC | Dedicated | Power | Core logic power, 1.0V. Power supply for core logic |
| VCC_DRM | Dedicated | Power | DRM power, 1.0V. Dedicated power supply for DRM. If the voltage is the same as VCC, it can be connected to VCC at the board. |
| VCCA | Dedicated | Power | Analog power, 1.8V. Power supply for internal analog circuit. |
| VCCIO[L3 , L4, L5, R4, R5, CFG] | Dedicated | Power | IO BANK power. |
| VCCB | Dedicated | Power | Key memory backup battery power supply voltage, 1.0V~1.9V.<br>When the key function is not used, the pin needs to be connected to the VCCA or ground. |
| VSS | Dedicated | Ground | Ground |
| **ADC PIN** | | | |
| VCCADC | Dedicated | Power | ADC analog power, 1.8V. Power supply for ADC analog circuit. |
| VSSADC | Dedicated | Ground | GND relative to VCCADC |
| VAADC_P | Dedicated | Input | ADC dedicated analog differential input (Positive). |
| VAADC_N | Dedicated | Input | ADC dedicated analog differential input (Negative). |
| VREFADC_P | Dedicated | N/A | 1.255V ADC reference voltage pin. |
| VREFADC_N | Dedicated | N/A | ADC reference voltage ground. |
| VAA[0,.., 15]P,VA A[0,.., 15]N | Multiplexed | Input | ADC differential analog input signals. |
| TSDP | Dedicated | N/A | Positive pin of the temperature sensor diode. When not used temperature diode, the pin needs to be connected to the VSS. When temperature sensor diode is to be used, then appropriate external temperature monitoring chip is required. |
| TSDN | Dedicated | N/A | Negative pin of the temperature sensor diode. |
| **HSST PIN** | | | |
| HSSTAVCC_QR3 | Dedicated | Power | 1.0V analog power pins, power supply for HSST internal transmit and receive circuit. |

| PIN Name | PIN Type | PIN Direction | PIN Description |
|---|---|---|---|
| HSSTAVCCPLL_Q R3 | Dedicated | Power | 1.2V analog power pin, Power supply for HSST internal PLL. |
| HSSTVSSA_PLL_QR3 | Dedicated | Ground | Analog ground, it can be connected to VSS at the PCB. |
| HSSTRREF_QR3 | Dedicated | Input | Calibration resistance input pin of the terminal resistance calibration circuit. |
| HSSTREFCLK[0, 1] P_QR3 | Dedicated | Input | Positive end of differential clock input pin, provide a reference clock to HSST. |
| HSSTREFCLK[0, 1] N_QR3 | Dedicated | Input | Negative end of differential clock input pin, provide a reference clock to HSST. |
| HSSTTX[0, 1,2,3][ P, N]_QR3 | Dedicated | Output | Channel differential outputs of HSST. Each HSST has 4 pairs. |
| HSSTRX[0, 1,2,3][ P, N]_QR3 | Dedicated | Input | Channel differential inputs of HSST. Each HSST has 4 pairs. |

### 2.2.1 Pin Name List

Table 2-3 Pin Name List

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| L3 | SIO_L3_00 | F15 | | 44.0027 | |
| L3 | DIFFIO_L3_G0_00P | F13 | IO_1_P | 53.4552 | L3_G0 |
| L3 | DIFFIO_L3_G0_00N | F14 | IO_1_N | 61.8799 | L3_G0 |
| L3 | DIFFIO_L3_G0_01P | F16 | IO_2_P | 42.1479 | L3_G0 |
| L3 | DIFFIO_L3_G0_01N | E17 | IO_2_N | 42.6294 | L3_G0 |
| L3 | DIFFIO_L3_G0_02P_DQS | C14 | IO_3_P | 88.9143 | L3_G0_DQS |
| L3 | DIFFIO_L3_G0_02N_DQS | C15 | IO_3_N | 97.7626 | L3_G0_DQS |
| L3 | DIFFIO_L3_G0_03P | E13 | IO_4_P | 88.4521 | L3_G0 |
| L3 | DIFFIO_L3_G0_03N | E14 | IO_4_N | 92.098 | L3_G0 |
| L3 | DIFFIO_L3_G0_04P | E16 | IO_5_P | 87.2326 | L3_G0 |
| L3 | DIFFIO_L3_G0_04N | D16 | IO_5_N | 88.1214 | L3_G0 |
| L3 | DIFFIO_L3_G0_05P | D14 | IO_6_P | 80.9852 | L3_G0 |
| L3 | DIFFIO_L3_G0_05N_VREF | D15 | IO_6_N | 75.3445 | L3_G0 |
| L3 | DIFFIO_L3_G1_06P | B15 | IO_7_P | 94.3549 | L3_G1 |
| L3 | DIFFIO_L3_G1_06N | B16 | IO_7_N | 103.082 | L3_G1 |
| L3 | DIFFIO_L3_G1_07P | C13 | IO_8_P | 90.7063 | L3_G1 |
| L3 | DIFFIO_L3_G1_07N | B13 | IO_8_N | 91.8746 | L3_G1 |
| L3 | DIFFIO_L3_G1_08P_DQS | A15 | IO_9_P | 107.661 | L3_G1_DQS |
| L3 | DIFFIO_L3_G1_08N_DQS | A16 | IO_9_N | 110.684 | L3_G1_DQS |
| L3 | DIFFIO_L3_G1_09P | A13 | IO_10_P | 104.806 | L3_G1 |
| L3 | DIFFIO_L3_G1_09N | A14 | IO_10_N | 104.764 | L3_G1 |
| L3 | DIFFIO_L3_G1_10P_GSCLK | B17 | IO_11_P | 92.782 | L3_G1 |
| L3 | DIFFIO_L3_G1_10N_GSCLK | B18 | IO_11_N | 90.4571 | L3_G1 |
| L3 | DIFFIO_L3_G1_1P_GMCLK | D17 | IO_12_P | 73.1576 | L3_G1 |
| L3 | DIFFIO_L3_G1_11N_GMCLK | C17 | IO_12_N | 75.0874 | L3_G1 |
| L3 | DIFFIO_L3_G2_12P_GMCLK | C18 | IO_13_P | 81.7606 | L3_G2 |
| L3 | DIFFIO_L3_G2_12N_GMCLK | C19 | IO_13_N | 85.2818 | L3_G2 |
| L3 | DIFFIO_L3_G2_13P_GSCLK | E19 | IO_14_P | 67.02 | L3_G2 |
| L3 | DIFFIO_L3_G2_13N_GSCLK | D19 | IO_14_N | 73.0285 | L3_G2 |
| L3 | DIFFIO_L3_G2_14P_DQS | F18 | IO_15_P | 76.3187 | L3_G2_DQS |
| L3 | DIFFIO_L3_G2_14N_DQS | E18 | IO_15_N | 77.1489 | L3_G2_DQS |
| L3 | DIFFIO_L3_G2_15P | B20 | IO_16_P | 108.264 | L3_G2 |
| L3 | DIFFIO_L3_G2_15N | A20 | IO_16_N | 117.146 | L3_G2 |
| L3 | DIFFIO_L3_G2_16P | A18 | IO_17_P | 108.414 | L3_G2 |
| L3 | DIFFIO_L3_G2_16N | A19 | IO_17_N | 115.277 | L3_G2 |
| L3 | DIFFIO_L3_G2_17P | F19 | IO_18_P | 66.3317 | L3_G2 |
| L3 | DIFFIO_L3_G2_17N | F20 | IO_18_N | 74.4915 | L3_G2 |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| L3 | DIFFIO_L3_G3_18P | D20 | IO_19_P | 85.8106 | L3_G3 |
| L3 | DIFFIO_L3_G3_18N_VREF | C20 | IO_19_N | 88.1833 | L3_G3 |
| L3 | DIFFIO_L3_G3_19P | C22 | IO_20_P | 101.803 | L3_G3 |
| L3 | DIFFIO_L3_G3_19N | B22 | IO_20_N | 102.893 | L3_G3 |
| L3 | DIFFIO_L3_G3_20P_DQS | B21 | IO_21_P | 111.893 | L3_G3_DQS |
| L3 | DIFFIO_L3_G3_20N_DQS | A21 | IO_21_N | 124.92 | L3_G3_DQS |
| L3 | DIFFIO_L3_G3_21P | E22 | IO_22_P | 90.5867 | L3_G3 |
| L3 | DIFFIO_L3_G3_21N | D22 | IO_22_N | 88.9613 | L3_G3 |
| L3 | DIFFIO_L3_G3_22P | E21 | IO_23_P | 83.6004 | L3_G3 |
| L3 | DIFFIO_L3_G3_22N | D21 | IO_23_N | 83.1138 | L3_G3 |
| L3 | DIFFIO_L3_G3_23P | G21 | IO_24_P | 80.5045 | L3_G3 |
| L3 | DIFFIO_L3_G3_23N | G22 | IO_24_N | 85.0294 | L3_G3 |
| L3 | SIO_L3_01 | F21 | | 72.7581 | |
| L4 | SIO_L4_00 | J16 | | 39.4275 | |
| L4 | DIFFIO_L4_G0_00P_VAA1P | H13 | IO_25_P | 129.658 | L4_G0 |
| L4 | DIFFIO_L4_G0_00N_VAA1N | G13 | IO_25_N | 120.441 | L4_G0 |
| L4 | DIFFIO_L4_G0_01P_VAA2P | G15 | IO_26_P | 71.7382 | L4_G0 |
| L4 | DIFFIO_L4_G0_01N_VAA2N | G16 | IO_26_N | 72.1065 | L4_G0 |
| L4 | DIFFIO_L4_G0_02P_DQS_VAA3P | J14 | IO_27_P | 89.5295 | L4_G0_DQS |
| L4 | DIFFIO_L4_G0_02N_DQS_VAA3N | H14 | IO_27_N | 85.7419 | L4_G0_DQS |
| L4 | DIFFIO_L4_G0_03P | G17 | IO_28_P | 66.1949 | L4_G0 |
| L4 | DIFFIO_L4_G0_03N | G18 | IO_28_N | 65.8194 | L4_G0 |
| L4 | DIFFIO_L4_G0_04P_VAA5P | J15 | IO_29_P | 69.5211 | L4_G0 |
| L4 | DIFFIO_L4_G0_04N_VAA5N | H15 | IO_29_N | 67.0896 | L4_G0 |
| L4 | DIFFIO_L4_G0_05P | H17 | IO_30_P | 60.143 | L4_G0 |
| L4 | DIFFIO_L4_G0_05N_VREF | H18 | IO_30_N | 61.6479 | L4_G0 |
| L4 | DIFFIO_L4_G1_06P_VAA7P | J22 | IO_31_P | 83.9608 | L4_G1 |
| L4 | DIFFIO_L4_G1_06N_VAA7N | H22 | IO_31_N | 84.4974 | L4_G1 |
| L4 | DIFFIO_L4_G1_07P_VAA8P | H20 | IO_32_P | 74.3615 | L4_G1 |
| L4 | DIFFIO_L4_G1_07N_VAA8N | G20 | IO_32_N | 77.2897 | L4_G1 |
| L4 | DIFFIO_L4_G1_08P_DQS_VAA9P | K21 | IO_33_P | 75.4039 | L4_G1_DQS |
| L4 | DIFFIO_L4_G1_08N_DQS_VAA9N | K22 | IO_33_N | 83.1404 | L4_G1_DQS |
| L4 | DIFFIO_L4_G1_09P_VAA10P | M21 | IO_34_P | 86.1757 | L4_G1 |
| L4 | DIFFIO_L4_G1_09N_VAA10N | L21 | IO_34_N | 86.1397 | L4_G1 |
| L4 | DIFFIO_L4_G1_10P_GSCLK | J20 | IO_35_P | 69.6028 | L4_G1 |
| L4 | DIFFIO_L4_G1_10N_GSCLK | J21 | IO_35_N | 78.6076 | L4_G1 |
| L4 | DIFFIO_L4_G1_11P_GMCLK | J19 | IO_36_P | 60.7004 | L4_G1 |
| L4 | DIFFIO_L4_G1_11N_GMCLK | H19 | IO_36_N | 57.8748 | L4_G1 |
| L4 | DIFFIO_L4_G2_12P_GMCLK | K18 | IO_37_P | 49.2586 | L4_G2 |
| L4 | DIFFIO_L4_G2_12N_GMCLK | K19 | IO_37_N | 51.6258 | L4_G2 |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| L4 | DIFFIO_L4_G2_13P_GSCLK | L19 | IO_38_P | 65.7914 | L4_G2 |
| L4 | DIFFIO_L4_G2_13N_GSCLK | L20 | IO_38_N | 68.6927 | L4_G2 |
| L4 | DIFFIO_L4_G2_14P_DQS | N22 | IO_39_P | 83.2729 | L4_G2_DQS |
| L4 | DIFFIO_L4_G2_14N_DQS_BADR VO_N | M22 | IO_39_N | 82.8885 | L4_G2_DQS |
| L4 | DIFFIO_L4_G2_15P_A28 | M18 | IO_40_P | 57.5797 | L4_G2 |
| L4 | DIFFIO_L4_G2_15N_A27 | L18 | IO_40_N | 54.5498 | L4_G2 |
| L4 | DIFFIO_L4_G2_16P_A26 | N18 | IO_41_P | 88.2872 | L4_G2 |
| L4 | DIFFIO_L4_G2_16N_A25 | N19 | IO_41_N | 80.5187 | L4_G2 |
| L4 | DIFFIO_L4_G2_17P_A24 | N20 | IO_42_P | 78.1013 | L4_G2 |
| L4 | DIFFIO_L4_G2_17N_A23 | M20 | IO_42_N | 68.6895 | L4_G2 |
| L4 | DIFFIO_L4_G3_18P_A22 | K13 | IO_43_P | 104.486 | L4_G3 |
| L4 | DIFFIO_L4_G3_18N_VREF_A21 | K14 | IO_43_N | 109.569 | L4_G3 |
| L4 | DIFFIO_L4_G3_19P_A20 | M13 | IO_44_P | 92.5727 | L4_G3 |
| L4 | DIFFIO_L4_G3_19N_A19 | L13 | IO_44_N | 96.5738 | L4_G3 |
| L4 | DIFFIO_L4_G3_20P_DQS | K17 | IO_45_P | 104.084 | L4_G3_DQS |
| L4 | DIFFIO_L4_G3_20N_DQS_A18 | J17 | IO_45_N | 95.2635 | L4_G3_DQS |
| L4 | DIFFIO_L4_G3_21P_A17 | L14 | IO_46_P | 73.7165 | L4_G3 |
| L4 | DIFFIO_L4_G3_21N_A16 | L15 | IO_46_N | 64.4338 | L4_G3 |
| L4 | DIFFIO_L4_G3_22P_BFOE_N | L16 | IO_47_P | 58.6904 | L4_G3 |
| L4 | DIFFIO_L4_G3_22N_BFWE_FCS2 _N | K16 | IO_47_N | 66.6165 | L4_G3 |
| L4 | DIFFIO_L4_G3_23P_VS1 | M15 | IO_48_P | 52.4272 | L4_G3 |
| L4 | DIFFIO_L4_G3_23N_VS0 | M16 | IO_48_N | 52.1856 | L4_G3 |
| L4 | SIO_L4_01 | M17 | | 53.7739 | |
| L5 | SIO_L5_00 | P20 | | 67.7697 | |
| L5 | DIFFIO_L5_G0_00P_MOSI_D0 | P22 | IO_49_P | 84.71 | L5_G0 |
| L5 | DIFFIO_L5_G0_00N_MISO_D1_DI | R22 | IO_49_N | 79.7674 | L5_G0 |
| L5 | DIFFIO_L5_G0_01P_D2 | P21 | IO_50_P | 71.0448 | L5_G0 |
| L5 | DIFFIO_L5_G0_01N_D3 | R21 | IO_50_N | 68.6379 | L5_G0 |
| L5 | DIFFIO_L5_G0_02P_DQS_IO_STATUS_C | U22 | IO_51_P | 96.5853 | L5_G0_DQS |
| L5 | DIFFIO_L5_G0_02N_DQS_ECCLK IN | V22 | IO_51_N | 99.1145 | L5_G0_DQS |
| L5 | DIFFIO_L5_G0_03P_D4 | T21 | IO_52_P | 89.3231 | L5_G0 |
| L5 | DIFFIO_L5_G0_03N_D5 | U21 | IO_52_N | 98.2167 | L5_G0 |
| L5 | DIFFIO_L5_G0_04P_D6 | P19 | IO_53_P | 72.244 | L5_G0 |
| L5 | DIFFIO_L5_G0_04N_D7 | R19 | IO_53_N | 62.0139 | L5_G0 |
| L5 | DIFFIO_L5_G0_05P_FCS_N | T19 | IO_54_P | 74.5971 | L5_G0 |
| L5 | DIFFIO_L5_G0_05N_VREF_D8 | T20 | IO_54_N | 66.2227 | L5_G0 |
| L5 | DIFFIO_L5_G1_06P_D9 | W21 | IO_55_P | 102.89 | L5_G1 |
| L5 | DIFFIO_L5_G1_06N_D10 | W22 | IO_55_N | 110.811 | L5_G1 |
| L5 | DIFFIO_L5_G1_07P_D11 | AA20 | IO_56_P | 122.41 | L5_G1 |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| L5 | DIFFIO_L5_G1_07N_D12 | AA21 | IO_56_N | 127.275 | L5_G1 |
| L5 | DIFFIO_L5_G1_08P_DQS_N | Y21 | IO_57_P | 104.222 | L5_G1_DQS |
| L5 | DIFFIO_L5_G1_08N_DQS_D13 | Y22 | IO_57_N | 103.9 | L5_G1_DQS |
| L5 | DIFFIO_L5_G1_09P_D14 | AB21 | IO_58_P | 119.156 | L5_G1 |
| L5 | DIFFIO_L5_G1_09N_D15 | AB22 | IO_58_N | 119.965 | L5_G1 |
| L5 | DIFFIO_L5_G1_10P_GSCLK | U20 | IO_59_P | 75.4609 | L5_G1 |
| L5 | DIFFIO_L5_G1_10N_GSCLK | V20 | IO_59_N | 79.7254 | L5_G1 |
| L5 | DIFFIO_L5_G1_11P_GMCLK | W19 | IO_60_P | 85.2746 | L5_G1 |
| L5 | DIFFIO_L5_G1_11N_GMCLK | W20 | IO_60_N | 86.1377 | L5_G1 |
| L5 | DIFFIO_L5_G2_12P_GMCLK | Y18 | IO_61_P | 100.507 | L5_G2 |
| L5 | DIFFIO_L5_G2_12N_GMCLK | Y19 | IO_61_N | 95.2638 | L5_G2 |
| L5 | DIFFIO_L5_G2_13P_GSCLK | V18 | IO_62_P | 86.1606 | L5_G2 |
| L5 | DIFFIO_L5_G2_13N_GSCLK | V19 | IO_62_N | 76.9529 | L5_G2 |
| L5 | DIFFIO_L5_G2_14P_DQS_RWSEL | AA19 | IO_63_P | 99.7792 | L5_G2_DQS |
| L5 | DIFFIO_L5_G2_14N_DQS_CSO_D OUT | AB20 | IO_63_N | 99.3412 | L5_G2_DQS |
| L5 | DIFFIO_L5_G2_15P_CS_N | V17 | IO_64_P | 83.2403 | L5_G2 |
| L5 | DIFFIO_L5_G2_15N_D31_A15 | W17 | IO_64_N | 76.5707 | L5_G2 |
| L5 | DIFFIO_L5_G2_16P_D30_A14 | AA18 | IO_65_P | 108.191 | L5_G2 |
| L5 | DIFFIO_L5_G2_16N_D29_A13 | AB18 | IO_65_N | 98.3891 | L5_G2 |
| L5 | DIFFIO_L5_G2_17P_D28_A12 | U17 | IO_66_P | 66.1155 | L5_G2 |
| L5 | DIFFIO_L5_G2_17N_D27_A11 | U18 | IO_66_N | 62.1274 | L5_G2 |
| L5 | DIFFIO_L5_G3_18P_D26_A10 | P14 | IO_67_P | 85.6241 | L5_G3 |
| L5 | DIFFIO_L5_G3_18N_VREF_D25_A9 | R14 | IO_67_N | 82.3999 | L5_G3 |
| L5 | DIFFIO_L5_G3_19P_D24_A8 | R18 | IO_68_P | 58.3729 | L5_G3 |
| L5 | DIFFIO_L5_G3_19N_D23_A7 | T18 | IO_68_N | 50.6074 | L5_G3 |
| L5 | DIFFIO_L5_G3_20P_DQS | N17 | IO_69_P | 80.9891 | L5_G3_DQS |
| L5 | DIFFIO_L5_G3_20N_DQS_D22_A 6 | P17 | IO_69_N | 78.3503 | L5_G3_DQS |
| L5 | DIFFIO_L5_G3_21P_D21_A5 | P15 | IO_70_P | 66.1866 | L5_G3 |
| L5 | DIFFIO_L5_G3_21N_D20_A4 | R16 | IO_70_N | 64.4195 | L5_G3 |
| L5 | DIFFIO_L5_G3_22P_D19_A3 | N13 | IO_71_P | 93.0743 | L5_G3 |
| L5 | DIFFIO_L5_G3_22N_D18_A2 | N14 | IO_71_N | 95.0011 | L5_G3 |
| L5 | DIFFIO_L5_G3_23P_D17_A1 | P16 | IO_72_P | 64.3564 | L5_G3 |
| L5 | DIFFIO_L5_G3_23N_D16_A0 | R17 | IO_72_N | 68.7269 | L5_G3 |
| L5 | SIO_L5_01 | N15 |  | 43.0079 |  |
| R4 | SIO_R4_00 | F4 |  | 75.4033 |  |
| R4 | DIFFIO_R4_G0_00P_VAA4P | B1 | IO_73_P | 129.212 | R4_G0 |
| R4 | DIFFIO_R4_G0_00N_VAA4N | A1 | IO_73_N | 132.344 | R4_G0 |
| R4 | DIFFIO_R4_G0_01P_VAA6P | C2 | IO_74_P | 104.235 | R4_G0 |
| R4 | DIFFIO_R4_G0_01N_VAA6N | B2 | IO_74_N | 108.831 | R4_G0 |
| R4 | DIFFIO_R4_G0_02P_DQS_VAA11 P | E1 | IO_75_P | 95.4297 | R4_G0_DQS |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| R4 | DIFFIO_R4_G0_02N_DQS_VAA11 N | D1 | IO_75_N | 97.4938 | R4_G0_DQS |
| R4 | DIFFIO_R4_G0_03P | E2 | IO_76_P | 93.7992 | R4_G0 |
| R4 | DIFFIO_R4_G0_03N | D2 | IO_76_N | 102.593 | R4_G0 |
| R4 | DIFFIO_R4_G0_04P_VAA12P | G1 | IO_77_P | 86.4057 | R4_G0 |
| R4 | DIFFIO_R4_G0_04N_VAA12N | F1 | IO_77_N | 88.2271 | R4_G0 |
| R4 | DIFFIO_R4_G0_05P | F3 | IO_78_P | 88.0001 | R4_G0 |
| R4 | DIFFIO_R4_G0_05N_VREF | E3 | IO_78_N | 89.8198 | R4_G0 |
| R4 | DIFFIO_R4_G1_06P_VAA13P | K1 | IO_79_P | 105.418 | R4_G1 |
| R4 | DIFFIO_R4_G1_06N_VAA13N | J1 | IO_79_N | 102.588 | R4_G1 |
| R4 | DIFFIO_R4_G1_07P_VAA14P | H2 | IO_80_P | 83.3581 | R4_G1 |
| R4 | DIFFIO_R4_G1_07N_VAA14N | G2 | IO_80_N | 81.3597 | R4_G1 |
| R4 | DIFFIO_R4_G1_08P_DQS_VAA15 P | K2 | IO_81_P | 113.587 | R4_G1_DQS |
| R4 | DIFFIO_R4_G1_08N_DQS_VAA15 N | J2 | IO_81_N | 103.649 | R4_G1_DQS |
| R4 | DIFFIO_R4_G1_09P_VAA0P | J5 | IO_82_P | 63.4776 | R4_G1 |
| R4 | DIFFIO_R4_G1_09N_VAA0N | H5 | IO_82_N | 73.3559 | R4_G1 |
| R4 | DIFFIO_R4_G1_10P_GSCLK | H3 | IO_83_P | 78.9072 | R4_G1 |
| R4 | DIFFIO_R4_G1_10N_GSCLK | G3 | IO_83_N | 88.53 | R4_G1 |
| R4 | DIFFIO_R4_G1_11P_GMCLK | H4 | IO_84_P | 72.2016 | R4_G1 |
| R4 | DIFFIO_R4_G1_11N_GMCLK | G4 | IO_84_N | 82.3152 | R4_G1 |
| R4 | DIFFIO_R4_G2_12P_GMCLK | K4 | IO_85_P | 84.7389 | R4_G2 |
| R4 | DIFFIO_R4_G2_12N_GMCLK | J4 | IO_85_N | 84.3055 | R4_G2 |
| R4 | DIFFIO_R4_G2_13P_GSCLK | L3 | IO_86_P | 72.1023 | R4_G2 |
| R4 | DIFFIO_R4_G2_13N_GSCLK | K3 | IO_86_N | 69.2169 | R4_G2 |
| R4 | DIFFIO_R4_G2_14P_DQS | M1 | IO_87_P | 92.8671 | R4_G2_DQS |
| R4 | DIFFIO_R4_G2_14N_DQS | L1 | IO_87_N | 84.3568 | R4_G2_DQS |
| R4 | DIFFIO_R4_G2_15P | M3 | IO_88_P | 73.6557 | R4_G2 |
| R4 | DIFFIO_R4_G2_15N | M2 | IO_88_N | 72.7605 | R4_G2 |
| R4 | DIFFIO_R4_G2_16P | K6 | IO_89_P | 82.0852 | R4_G2 |
| R4 | DIFFIO_R4_G2_16N | J6 | IO_89_N | 81.9025 | R4_G2 |
| R4 | DIFFIO_R4_G2_17P | L5 | IO_90_P | 69.688 | R4_G2 |
| R4 | DIFFIO_R4_G2_17N | L4 | IO_90_N | 76.5251 | R4_G2 |
| R4 | DIFFIO_R4_G3_18P | N4 | IO_91_P | 79.0432 | R4_G3 |
| R4 | DIFFIO_R4_G3_18N_VREF | N3 | IO_91_N | 72.0662 | R4_G3 |
| R4 | DIFFIO_R4_G3_19P | R1 | IO_92_P | 103.419 | R4_G3 |
| R4 | DIFFIO_R4_G3_19N | P1 | IO_92_N | 103.446 | R4_G3 |
| R4 | DIFFIO_R4_G3_20P_DQS | P5 | IO_93_P | 80.7115 | R4_G3_DQS |
| R4 | DIFFIO_R4_G3_20N_DQS | P4 | IO_93_N | 74.116 | R4_G3_DQS |
| R4 | DIFFIO_R4_G3_21P | P2 | IO_94_P | 88.2188 | R4_G3 |
| R4 | DIFFIO_R4_G3_21N | N2 | IO_94_N | 87.6737 | R4_G3 |
| R4 | DIFFIO_R4_G3_22P | M6 | IO_95_P | 57.3366 | R4_G3 |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| R4 | DIFFIO_R4_G3_22N | M5 | IO_95_N | 58.6733 | R4_G3 |
| R4 | DIFFIO_R4_G3_23P | P6 | IO_96_P | 63.9982 | R4_G3 |
| R4 | DIFFIO_R4_G3_23N | N5 | IO_96_N | 58.6343 | R4_G3 |
| R4 | SIO_R4_01 | L6 | | 47.8462 | |
| R5 | SIO_R5_00 | T3 | | 92.5382 | |
| R5 | DIFFIO_R5_G0_00P | T1 | IO_97_P | 117.71 | R5_G0 |
| R5 | DIFFIO_R5_G0_00N | U1 | IO_97_N | 109.243 | R5_G0 |
| R5 | DIFFIO_R5_G0_01P | U2 | IO_98_P | 113.922 | R5_G0 |
| R5 | DIFFIO_R5_G0_01N | V2 | IO_98_N | 123.636 | R5_G0 |
| R5 | DIFFIO_R5_G0_02P_DQS | R3 | IO_99_P | 98.6603 | R5_G0_DQS |
| R5 | DIFFIO_R5_G0_02N_DQS | R2 | IO_99_N | 98.5989 | R5_G0_DQS |
| R5 | DIFFIO_R5_G0_03P | W2 | IO_100_P | 129.061 | R5_G0 |
| R5 | DIFFIO_R5_G0_03N | Y2 | IO_100_N | 134.311 | R5_G0 |
| R5 | DIFFIO_R5_G0_04P | W1 | IO_101_P | 113.508 | R5_G0 |
| R5 | DIFFIO_R5_G0_04N | Y1 | IO_101_N | 112.353 | R5_G0 |
| R5 | DIFFIO_R5_G0_05P | U3 | IO_102_P | 97.9758 | R5_G0 |
| R5 | DIFFIO_R5_G0_05N_VREF | V3 | IO_102_N | 98.0589 | R5_G0 |
| R5 | DIFFIO_R5_G1_06P | AA1 | IO_103_P | 127.185 | R5_G1 |
| R5 | DIFFIO_R5_G1_06N | AB1 | IO_103_N | 129.766 | R5_G1 |
| R5 | DIFFIO_R5_G1_07P | AB3 | IO_104_P | 131.327 | R5_G1 |
| R5 | DIFFIO_R5_G1_07N | AB2 | IO_104_N | 131.061 | R5_G1 |
| R5 | DIFFIO_R5_G1_08P_DQS | Y3 | IO_105_P | 113.346 | R5_G1_DQS |
| R5 | DIFFIO_R5_G1_08N_DQS | AA3 | IO_105_N | 111.926 | R5_G1_DQS |
| R5 | DIFFIO_R5_G1_09P | AA5 | IO_106_P | 121.055 | R5_G1 |
| R5 | DIFFIO_R5_G1_09N | AB5 | IO_106_N | 115.145 | R5_G1 |
| R5 | DIFFIO_R5_G1_10P_GSCLK | Y4 | IO_107_P | 105.919 | R5_G1 |
| R5 | DIFFIO_R5_G1_10N_GSCLK | AA4 | IO_107_N | 107.173 | R5_G1 |
| R5 | DIFFIO_R5_G1_11P_GMCLK | V4 | IO_108_P | 98.4916 | R5_G1 |
| R5 | DIFFIO_R5_G1_11N_GMCLK | W4 | IO_108_N | 97.3706 | R5_G1 |
| R5 | DIFFIO_R5_G2_12P_GMCLK | R4 | IO_109_P | 76.5076 | R5_G2 |
| R5 | DIFFIO_R5_G2_12N_GMCLK | T4 | IO_109_N | 74.5597 | R5_G2 |
| R5 | DIFFIO_R5_G2_13P_GSCLK | T5 | IO_110_P | 79.6201 | R5_G2 |
| R5 | DIFFIO_R5_G2_13N_GSCLK | U5 | IO_110_N | 74.8451 | R5_G2 |
| R5 | DIFFIO_R5_G2_14P_DQS | W6 | IO_111_P | 91.1608 | R5_G2_DQS |
| R5 | DIFFIO_R5_G2_14N_DQS | W5 | IO_111_N | 90.3878 | R5_G2_DQS |
| R5 | DIFFIO_R5_G2_15P | U6 | IO_112_P | 86.9713 | R5_G2 |
| R5 | DIFFIO_R5_G2_15N | V5 | IO_112_N | 89.9189 | R5_G2 |
| R5 | DIFFIO_R5_G2_16P | R6 | IO_113_P | 76.3969 | R5_G2 |
| R5 | DIFFIO_R5_G2_16N | T6 | IO_113_N | 84.4228 | R5_G2 |
| R5 | DIFFIO_R5_G2_17P | Y6 | IO_114_P | 87.4999 | R5_G2 |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| R5 | DIFFIO_R5_G2_17N | AA6 | IO_114_N | 88.1913 | R5_G2 |
| R5 | DIFFIO_R5_G3_18P | V7 | IO_115_P | 87.5513 | R5_G3 |
| R5 | DIFFIO_R5_G3_18N_VREF | W7 | IO_115_N | 87.6331 | R5_G3 |
| R5 | DIFFIO_R5_G3_19P | AB7 | IO_116_P | 96.385 | R5_G3 |
| R5 | DIFFIO_R5_G3_19N | AB6 | IO_116_N | 96.1584 | R5_G3 |
| R5 | DIFFIO_R5_G3_20P_DQS | V9 | IO_117_P | 83.2041 | R5_G3_DQS |
| R5 | DIFFIO_R5_G3_20N_DQS | V8 | IO_117_N | 78.7716 | R5_G3_DQS |
| R5 | DIFFIO_R5_G3_21P | AA8 | IO_118_P | 94.0513 | R5_G3 |
| R5 | DIFFIO_R5_G3_21N | AB8 | IO_118_N | 96.5192 | R5_G3 |
| R5 | DIFFIO_R5_G3_22P | Y8 | IO_119_P | 63.931 | R5_G3 |
| R5 | DIFFIO_R5_G3_22N | Y7 | IO_119_N | 76.4183 | R5_G3 |
| R5 | DIFFIO_R5_G3_23P | W9 | IO_120_P | 60.5622 | R5_G3 |
| R5 | DIFFIO_R5_G3_23N | Y9 | IO_120_N | 55.3008 | R5_G3 |
| R5 | SIO_R5_01 | U7 |  | 63.183 |  |
|  | HSSTRX0N_QR3 | C9 | IO_121_N | 67.9925 |  |
|  | HSSTRX0P_QR3 | D9 | IO_121_P | 75.4841 |  |
|  | HSSTRX1N_QR3 | A10 | IO_122_N | 100.463 |  |
|  | HSSTRX1P_QR3 | B10 | IO_122_P | 100.318 |  |
|  | HSSTRX2N_QR3 | C11 | IO_123_N | 82.4767 |  |
|  | HSSTRX2P_QR3 | D11 | IO_123_P | 102.061 |  |
|  | HSSTRX3N_QR3 | A8 | IO_124_N | 100.893 |  |
|  | HSSTRX3P_QR3 | B8 | IO_124_P | 99.4223 |  |
|  | HSSTTX0N_QR3 | C7 | IO_125_N | 91.6053 |  |
|  | HSSTTX0P_QR3 | D7 | IO_125_P | 97.0165 |  |
|  | HSSTTX1N_QR3 | A6 | IO_126_N | 99.9758 |  |
|  | HSSTTX1P_QR3 | B6 | IO_126_P | 109.374 |  |
|  | HSSTTX2N_QR3 | C5 | IO_127_N | 89.0322 |  |
|  | HSSTTX2P_QR3 | D5 | IO_127_P | 98.2966 |  |
|  | HSSTTX3N_QR3 | A4 | IO_128_N | 108.389 |  |
|  | HSSTTX3P_QR3 | B4 | IO_128_P | 119.49 |  |
|  | HSSTREFCLK0N_QR3 | E6 | IO_129_N | 63.5031 |  |
|  | HSSTREFCLK0P_QR3 | F6 | IO_129_P | 61.8517 |  |
|  | HSSTREFCLK1N_QR3 | E10 | IO_130_N | 72.6599 |  |
|  | HSSTREFCLK1P_QR3 | F10 | IO_130_P | 76.4009 |  |
|  | HSSTRREF_QR3 | F8 |  | 46.4071 |  |
|  | HSSTAVCC _QR3 | F9 |  |  |  |
|  | HSSTAVCCPLL_QR3 | B5 |  |  |  |
|  | HSSTAVCCPLL_QR3 | B7 |  |  |  |
|  | HSSTAVCCPLL_QR3 | B9 |  |  |  |
|  | HSSTAVCCPLL_QR3 | B11 |  |  |  |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| | HSSTAVCCPLL_QR3 | C4 | | | |
| | HSSTAVCCPLL_QR3 | C8 | | | |
| | HSSTAVCC_QR3 | D6 | | | |
| | HSSTAVCC_QR3 | D10 | | | |
| | HSSTAVCC_QR3 | E8 | | | |
| | HSSTAVCC_QR3 | F7 | | | |
| | HSSTVSSA_PLL_QR3 | G7 | | | |
| | HSSTVSSA_PLL_QR3 | G8 | | | |
| | HSSTVSSA_PLL_QR3 | G9 | | | |
| | CFG_CLK | L12 | | 66.926 | |
| | CFG_DONE | G11 | | 107.399 | |
| | INIT_FLAG_N | U12 | | 46.2996 | |
| | MODE_0 | U11 | | 53.2374 | |
| | MODE_1 | U10 | | 54.6131 | |
| | MODE_2 | U9 | | 51.975 | |
| | NC1 | AA16 | | 76.1278 | |
| | NC2 | AA14 | | 62.22 | |
| | RSTN | N12 | | 37.1212 | |
| | SCBV | U8 | | 79.7938 | |
| | TCK | V12 | | 141.14 | |
| | TDI | R13 | | 101.441 | |
| | TDO | U13 | | 130.699 | |
| | TMS | T13 | | 119.822 | |
| | TSDN | N9 | IO_131_N | 103.3 | |
| | TSDP | N10 | IO_131_P | 103.483 | |
| | VAADC_N | M9 | IO_132_N | 84.5682 | |
| | VAADC_P | L10 | IO_132_P | 82.8515 | |
| | VREFADC_N | L9 | IO_133_N | 101.206 | |
| | VREFADC_P | M10 | IO_133_P | 97.3387 | |
| | VCCIOL3 | A17 | | | |
| | VCCIOL3 | B14 | | | |
| | VCCIOR4 | C1 | | | |
| | VCCIOL3 | C21 | | | |
| | VCCIOL3 | D18 | | | |
| | VCCB | E12 | | | |
| | VCCIOL3 | E15 | | | |
| | VCCIOR4 | F2 | | | |
| | VCCIOCFG | F12 | | | |
| | VCCIOL3 | F22 | | | |
| | VCCIOL4 | G19 | | | |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| | VCCIOR4 | H6 | | | |
| | VCC | H8 | | | |
| | VCC | H10 | | | |
| | VCCA | H12 | | | |
| | VCCIOL4 | H16 | | | |
| | VCCIOR4 | J3 | | | |
| | VCC | J7 | | | |
| | VCC | J9 | | | |
| | VCC_DRM | J11 | | | |
| | VCCIOL4 | J13 | | | |
| | VCC | K8 | | | |
| | VCCADC | K10 | | | |
| | VCCA | K12 | | | |
| | VCCIOL4 | K20 | | | |
| | VCC | L7 | | | |
| | VCC_DRM | L11 | | | |
| | VCCIOL4 | L17 | | | |
| | VCCIOR4 | M4 | | | |
| | VCC | M8 | | | |
| | VCCA | M12 | | | |
| | VCCIOL5 | M14 | | | |
| | VCCIOR4 | N1 | | | |
| | VCC | N7 | | | |
| | VCC_DRM | N11 | | | |
| | VCCIOL4 | N21 | | | |
| | VCC | P8 | | | |
| | VCC | P10 | | | |
| | VCCA | P12 | | | |
| | VCCIOL5 | P18 | | | |
| | VCCIOR5 | R5 | | | |
| | VCC | R7 | | | |
| | VCC | R9 | | | |
| | VCCA | R11 | | | |
| | VCCIOL5 | R15 | | | |
| | VCCIOR5 | T2 | | | |
| | VCC | T8 | | | |
| | VCC | T10 | | | |
| | VCCIOCFG | T12 | | | |
| | VCCIOL5 | T22 | | | |
| | VCCIOL5 | U19 | | | |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| | VCCIOR5 | V6 | | | |
| | VCCIOL6 | V16 | | | |
| | VCCIOR5 | W3 | | | |
| | VCCIOL6 | W13 | | | |
| | VCCIOL6 | Y10 | | | |
| | VCCIOL5 | Y20 | | | |
| | VCCIOR5 | AA7 | | | |
| | VCCIOL6 | AA17 | | | |
| | VCCIOR5 | AB4 | | | |
| | VCCIOL6 | AB14 | | | |
| | VSS | A2 | | | |
| | VSS | A3 | | | |
| | VSS | A5 | | | |
| | VSS | A7 | | | |
| | VSS | A9 | | | |
| | VSS | A11 | | | |
| | VSS | A12 | | | |
| | VSS | A22 | | | |
| | VSS | B3 | | | |
| | VSS | B12 | | | |
| | VSS | B19 | | | |
| | VSS | C3 | | | |
| | VSS | C6 | | | |
| | VSS | C10 | | | |
| | VSS | C12 | | | |
| | VSS | C16 | | | |
| | VSS | D3 | | | |
| | VSS | D4 | | | |
| | VSS | D8 | | | |
| | VSS | D12 | | | |
| | VSS | D13 | | | |
| | VSS | E4 | | | |
| | VSS | E5 | | | |
| | VSS | E7 | | | |
| | VSS | E9 | | | |
| | VSS | E11 | | | |
| | VSS | E20 | | | |
| | VSS | F5 | | | |
| | VSS | F11 | | | |
| | VSS | F17 | | | |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| | VSS | G5 | | | |
| | VSS | G6 | | | |
| | VSS | G10 | | | |
| | VSS | G12 | | | |
| | VSS | G14 | | | |
| | VSS | H1 | | | |
| | VSS | H7 | | | |
| | VSS | H9 | | | |
| | VSS | H11 | | | |
| | VSS | H21 | | | |
| | VSS | J8 | | | |
| | VSS | J10 | | | |
| | VSS | J12 | | | |
| | VSS | J18 | | | |
| | VSS | K5 | | | |
| | VSS | K7 | | | |
| | VSSADC | K9 | | | |
| | VSS | K11 | | | |
| | VSS | K15 | | | |
| | VSS | L2 | | | |
| | VSS | L8 | | | |
| | VSS | L22 | | | |
| | VSS | M7 | | | |
| | VSS | M11 | | | |
| | VSS | M19 | | | |
| | VSS | N6 | | | |
| | VSS | N8 | | | |
| | VSS | N16 | | | |
| | VSS | P3 | | | |
| | VSS | P7 | | | |
| | VSS | P9 | | | |
| | VSS | P11 | | | |
| | VSS | P13 | | | |
| | VSS | R8 | | | |
| | VSS | R10 | | | |
| | VSS | R12 | | | |
| | VSS | R20 | | | |
| | VSS | T7 | | | |
| | VSS | T9 | | | |
| | VSS | T11 | | | |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| | VSS | T17 | | | |
| | VSS | U4 | | | |
| | VSS | U14 | | | |
| | VSS | V1 | | | |
| | VSS | V11 | | | |
| | VSS | V21 | | | |
| | VSS | W8 | | | |
| | VSS | W18 | | | |
| | VSS | Y5 | | | |
| | VSS | Y15 | | | |
| | VSS | AA2 | | | |
| | VSS | AA12 | | | |
| | VSS | AA22 | | | |
| | VSS | AB9 | | | |
| | VSS | AB19 | | | |
| | NC | T14 | | | |
| | NC | T15 | | | |
| | NC | T16 | | | |
| | NC | U15 | | | |
| | NC | U16 | | | |
| | NC | V10 | | | |
| | NC | V13 | | | |
| | NC | V14 | | | |
| | NC | V15 | | | |
| | NC | W10 | | | |
| | NC | W11 | | | |
| | NC | W12 | | | |
| | NC | W14 | | | |
| | NC | W15 | | | |
| | NC | W16 | | | |
| | NC | Y11 | | | |
| | NC | Y12 | | | |
| | NC | Y13 | | | |
| | NC | Y14 | | | |
| | NC | Y16 | | | |
| | NC | Y17 | | | |
| | NC | AA9 | | | |
| | NC | AA10 | | | |
| | NC | AA11 | | | |
| | NC | AA13 | | | |

| Bank Name | Pin Name(Function name) | Pin Number | Differential Pair | Time Delay(ps) | DQS Group |
|---|---|---|---|---|---|
| | NC | AA15 | | | |
| | NC | AB10 | | | |
| | NC | AB11 | | | |
| | NC | AB12 | | | |
| | NC | AB13 | | | |
| | NC | AB15 | | | |
| | NC | AB16 | | | |
| | NC | AB17 | | | |

# Chapter 3 Thermal Resistance

Table 3-1 Thermal Resistance

| **θJA(℃/W) (Flow: 0m/s)** | **θJB (℃/W)** | **θJC (℃/W)** | **θJA(℃/W) (Flow: 1m/s)** | **θJA(℃/W) (Flow: 2m/s)** |
|---|---|---|---|---|
| 17.1 | 11.6 | 6.9 | 14.9 | 13.6 |

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