PK02012_PGL50G_MBG324

(V1.1)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.1	26.08.2022	Initial release

About this Manual

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Terms and Abbreviations	Meaning
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PGL50G_MBG324 uses a Wire Bonded BGA type of packaging. Its package size is 15mmx15mm, with 324 solder balls, a pitch of 0.8mm and a maximum package thickness of 1.45mm.

Chapter 2 Package Dimension

Table 2-1 Dimensional Values

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	1.15	1.30	1.45	c	0.22	0.26	0.30
A1	0.30	0.35	0.40	e	-	0.8	-
A2	0.91	0.96	1.01	b	0.40	0.45	0.50
D	14.9	15.0	15.1	aaa	-	-	0.15
E	14.9	15.0	15.1	ccc	-	-	0.15
D1	-	13.6	-	ddd	-	-	0.20
E1	-	13.6	-	eee	-	-	0.15

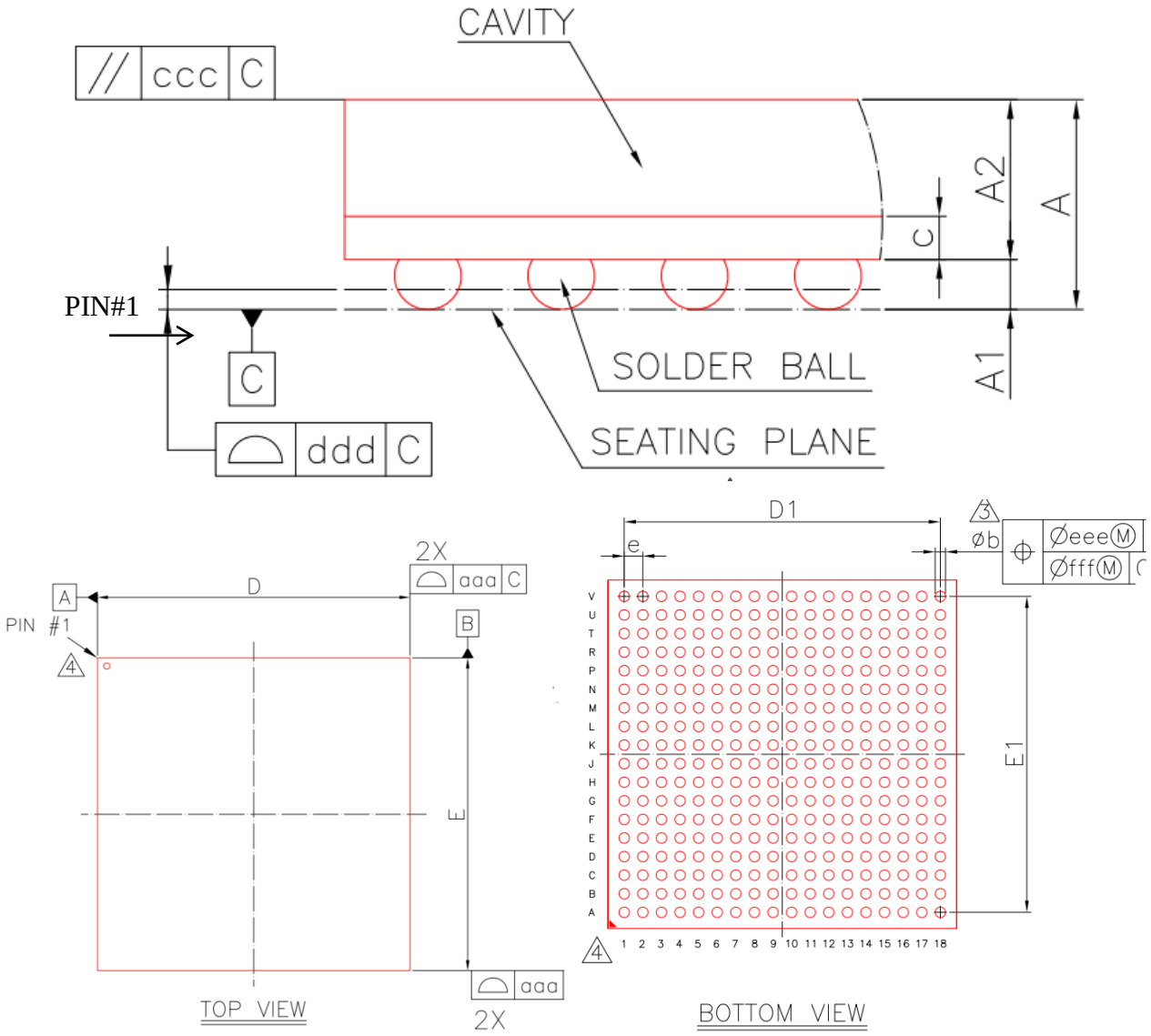

Figure 2-1 Package Outline Dimension (POD)

Note: PIN#1 is the first pin position of the chip

Chapter 3 Pin Definitions

PGL50G_MBG324 has 218 user IOs.

Table 3-1 Device Pin Definitions

PIN name	PIN type	PIN description
User IO PIN		
DIFFIO_[0,1,2,3]_[0…n][N,P]	I/O	USER IO: (1) "DIFFIO" indicates the pin supports differential input/output and can be used for transmitting and receiving LVDS signals; (2) "B[0,1,2,3]" indicates bank numbers; (3) "[0…n]" indicates the number of programmable I/O pairs in a bank; (4) In "[N,P]", "P" indicates the positive side of the differential pair and "N" indicates the negative side; (5) Before or during configuration, when IO_STATUS_C=0, enable internal pull-up resistors, when IO_STATUS_C=1, switch off internal pull-up resistors; (6) In user mode, Unused I/Os default to PLLDOWN, but can be set to PLLUP, PLLDOWN, or UNUSED via bitstream;
DIFFI_[0,1,2,3]_[0…n]_[N,P]	I/O	USER IO: (1) "DIFFI" indicates the pin only supports differential input and can receive differential input signals; (2) "B[0,1,2,3]" indicates bank numbers; (3) "[0…n]" indicates the number of programmable I/O pairs in a bank; (4) In "[N,P]", "P" indicates the positive side of the differential pair and "N" indicates the negative side; (5) Before or during configuration, when IO_STATUS_C=0, enable internal pull-up resistors, when IO_STATUS_C=1, switch off internal pull-up resistors; (6) In user mode, Unused I/Os default to PLLDOWN, but can be set to PLLUP, PLLDOWN, or UNUSED via bitstream;
Multiplexed Pin		
Configurable Multiplexed PIN		
MODE_1	input	Configurable multiplexed pin, used for selecting between master and slave configuration modes: (1) MODE_1="0", master mode; (2) MODE_1="1", slave mode.
MODE_0	input	Configurable multiplexed pin, used for selecting between parallel and serial configuration modes: (1) MODE_0="0", parallel configuration; (2) MODE_0="1", serial configuration.
INIT_FLAG_N	Bidirectional (open-drain)	Initialization and configuration status pin: (1) When it is Low, it indicates that the FPGA's

PIN name	PIN type	PIN description
		internal CRAM is being cleared, and this pin will be released by internal control upon completion. (2) If this pin is pulled Low externally, it will delay the configuration process; (3) If this pin is Low during configuration, it indicates an internal configuration error occurred; (4) This pin is an open-drain output and should be connected to VCCIO2 via an external pull-up resistor.
CFG_CLK	input, output	Configurable multiplexed clock pin: (1) In the slave mode, this pin serves as a clock input to obtain configuration data from external sources; (2) In the master mode, this pin serves as a clock output to obtain configuration data from external sources; (3) When the clock is not needed (such as in the JTAG mode), this pin is in the high-Z state.
ECCLK	input	Configurable multiplexed clock pin: Optional external configuration clock input pin in the master mode
CS_N	input,, output	Configurable multiplexed pin: (1) In the Slave Parallel configuration mode, this pin enables the parallel configuration mode data interface at a low voltage; (2) In the SPI x1 mode, when this pin is connected to the Slave Data input interface of the SPI Flash, FPGA will send instructions and initial address to the SPI Flash; (3) In the SPI x2 and x4 modes, this pin also serves as the bit 0 bit of the data bus.
CSO_N	output	Configurable multiplexed pin: (1) In the parallel configuration mode, it serves as the cascaded chip-select signal output; (2) In the master SPI mode, it serves as the chip-select signal output.
D0	input	Configurable multiplexed data pins: (1) In the SPI x1 mode, this pin connects to the Slave Data output interface of the SPI Flash, and FPGA receives serial data from the SPI Flash, i.e., Master Input/Slave Output; (2) In the SPI x2 and x4 modes, this pin also serves as the bit 1 of the SPI data bus; (3) In the parallel or BPI mode, this pin serves as the lowest bit of the data bus (4) In the Slave Serial mode, this pin serves as data input.
D[1,2]	input, output	Configurable multiplexed data pins: (1) In the SPI x2 and x4 modes, D[1] acts as the bit 2 of the data and D[2] as the bit 3of the data; (2) In the parallel mode, this pin serves as the bit[1:2] of the data bus.
D[3, 4, 5…15]	input, output	Configurable multiplexed data pins: (1) In the Parallel mode with x8 width, D[7:3] serves as the bit[7:3] of the data bus; (2) In the Parallel mode with x16 width, D[15:3] serves as the bit[15:3] of the data bus.

PIN name	PIN type	PIN description
RWSEL	input	Configurable multiplexed pin, for selecting the read/write input in the Slave Parallel configuration mode: (1) When it is High, the Slave Parallel configuration mode reads data from the data bus; (2) When it is Low, the Slave Parallel configuration mode writes data to the data bus; (3) Read and write can be switched only when CS_N is High.
DOUT_BUSY	output	Configurable multiplexed pin: (1) During readback in the parallel slave mode, it indicates device status; a High output signifies data read from the bus is invalid; (2) In the serial configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK (3) In the SPI configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK.
IO_STATUS_C	input	Configurable multiplexed pin, used for controlling whether the pull-up resistors for all user IOs are enabled during the configuration process: (1) When it is set to "0", the internal pull-up resistors for user IOs are enabled before or during configuration; (2) When it is set to "1", the internal pull-up resistors for user IOs are disabled before or during configuration; (3) This pin must not be left floating before or during configuration.
ADR[0, 1, …, 25]	output	Multiplexed configuration pin, address output in BPI configuration mode; (1) After configuration is complete, it can be used as user IO.
BFWE_N	output	Multi-function configuration pin, used for providing a low-voltage write-enable signal for parallel NOR FLASH in the BPI configuration mode.
BFOE_N	output	Multi-function configuration pin, used for providing a low-voltage output-enablesignal for parallel NOR FLASH in the BPI configuration mode.
BFCE_N	output	Multi-function configuration pin, used for providing a low-voltage chip-select control signal for parallel NOR FLASH in the BPI configuration mode；
BHDC	output	In BPI mode, there is High output during the configuration
BLDC	output	In BPI mode, there is Low output during the configuration
Clock Pin		
GCLK[0,1,2,3…,30,31]	input	Dedicated global clock pin. Can also serve as a general user I/O, 8 pins for each bank When it serves as a differential clock input, GCLK[1,3,5,…,27,29,31] are the internal valid input.
PLL[1,2,3,4,5]_CLK[0,1,2,…,13,14,15]	input	Optional PLL reference clock input, PLL can directly input the clock from these pins. Optional PLL feedback clock input, PLL can externally feedback the clock from these pins.

PIN name	PIN type	PIN description
		Also used as general I/Os.
External Memory Interface PIN		
DQS[0,1,2,3,4,5,6,7,8][#]_[1,3]	DQS	Multi-function pin. Used to connect to the DQS/DQS# signal pins of external memory. Also used as general user I/Os.
DQ[0,1,2,3,4,5,6,7,8][#]_[1,3]	DQ	Multi-function pin, can connect to the DQ signal pins of external memory. Also used as general user I/Os.
Reference Pin		
VREF_[B0,B1,B2,B3]	input	External reference power pin, for providing reference voltage input for each BANK.
Dedicated Pin		
CFG_DONE	Bidirectional (open-drain)	Dedicated configuration status pin. Serves as a status output, driven Low before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.
RST_N	input	Dedicated configuration pin, internally weak pull-up, for restarting the configuration process, active-low. It is recommended that users externally pull up the RST_N with a resistor when using this pin. When this pin is Low, the FPGA enters a reset state, and all IOs are in the high-Z state.
TCK	input	Dedicated JTAG test clock input pin
TMS	input	Dedicated JTAG test mode selection input pin
TDI	input	Dedicated JTAG test data input pin
TDO	output	Dedicated JTAG test data output pin
Power Pin, Ground Pin		
VCC	POWER	Core power supply, 1.2V. Power supply for core logic
VCCAUX	POWER	Auxiliary power, 3.3V.
VCCEFUSE	POWER	eFuse power pin; should be used in the following two situations: When the configuration of eFuse function is needed, this pin is connected to 3.3V power and should be powered up according to the recommended power-up sequence. After configuration, the voltage can be maintained at 3.3V or grounded after powering down according to the power-down sequence requirements; it should not be left floating. No need to configure the eFuse function. This pin should be grounded.
VCCIO[0,1,2,3]	POWER	IO BANK power
VSS	GROUND	GND
Reserved Pin		
NC		No need to be connected, left floating
CMPCS_B		No need to be connected, left floating
STAND_BY		No need to be connected, left floating

Chapter 4 Pin Name list

Table 4-1 Pin Name List

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
BANK0	DIFFIO_B0_0P/IO_STATUS_C	D4	IO_1_P	38.086	
BANK0	DIFFIO_B0_0N/VREF_B0	C4	IO_1_N	37.383	
BANK0	DIFFIO_B0_1P	B2	IO_2_P	41.263	
BANK0	DIFFIO_B0_1N	A2	IO_2_N	40.665	
BANK0	DIFFIO_B0_2P	D6	IO_3_P	39.522	
BANK0	DIFFIO_B0_2N	C6	IO_3_N	40.596	
BANK0	DIFFIO_B0_3P	B3	IO_4_P	39.110	
BANK0	DIFFIO_B0_3N	A3	IO_4_N	39.884	
BANK0	DIFFIO_B0_4P	B4	IO_5_P	37.704	
BANK0	DIFFIO_B0_4N	A4	IO_5_N	38.328	
BANK0	DIFFIO_B0_6P	C5	IO_6_P	38.961	
BANK0	DIFFIO_B0_6N	A5	IO_6_N	36.218	
BANK0	DIFFIO_B0_7P	C7	IO_7_P	38.592	
BANK0	DIFFIO_B0_7N	A7	IO_7_N	32.032	
BANK0	DIFFIO_B0_9P	B6	IO_8_P	30.744	
BANK0	DIFFIO_B0_9N/VREF_B0	A6	IO_8_N	32.356	
BANK0	DIFFIO_B0_10P	D8	IO_9_P	39.597	
BANK0	DIFFIO_B0_10N	C8	IO_9_N	41.734	
BANK0	DIFFIO_B0_11P	B8	IO_10_P	30.408	
BANK0	DIFFIO_B0_11N	A8	IO_10_N	31.241	
BANK0	DIFFIO_B0_13P/GCLK19/PLL1_CLK0	D9	IO_11_P	32.317	
BANK0	DIFFIO_B0_13N/GCLK18/PLL1_CLK1	C9	IO_11_N	29.843	
BANK0	DIFFIO_B0_14P/GCLK17/PLL1_CLK2	B9	IO_12_P	34.476	
BANK0	DIFFIO_B0_14N/GCLK16/PLL1_CLK3	A9	IO_12_N	35.837	
BANK0	DIFFIO_B0_15P/GCLK15/PLL1_CLK4	D11	IO_13_P	31.745	
BANK0	DIFFIO_B0_15N/GCLK14/PLL1_CLK5	C11	IO_13_N	32.066	
BANK0	DIFFIO_B0_16P/GCLK13/PLL1_CLK6	C10	IO_14_P	36.548	
BANK0	DIFFIO_B0_16N/GCLK12/PLL1_CLK7	A10	IO_14_N	35.329	
BANK0	DIFFIO_B0_17P	G9	IO_15_P	57.793	
BANK0	DIFFIO_B0_17N/VREF_B0	F9	IO_15_N	54.123	

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
BANK0	DIFFIO_B0_23P	B11	IO_16_P	30.873	
BANK0	DIFFIO_B0_23N	A11	IO_16_N	31.533	
BANK0	DIFFIO_B0_24P	B12	IO_17_P	30.592	
BANK0	DIFFIO_B0_24N	A12	IO_17_N	30.827	
BANK0	DIFFIO_B0_25P	C13	IO_18_P	34.648	
BANK0	DIFFIO_B0_25N	A13	IO_18_N	31.886	
BANK0	DIFFIO_B0_26P	B14	IO_19_P	34.280	
BANK0	DIFFIO_B0_26N/VREF_B0	A14	IO_19_N	34.199	
BANK0	DIFFIO_B0_27P	F13	IO_20_P	45.507	
BANK0	DIFFIO_B0_27N	E13	IO_20_N	43.095	
BANK0	DIFFIO_B0_28P	C15	IO_21_P	42.879	
BANK0	DIFFIO_B0_28N	A15	IO_21_N	42.439	
BANK0	DIFFIO_B0_29P	D14	IO_22_P	30.350	
BANK0	DIFFIO_B0_29N	C14	IO_22_N	24.860	
BANK0	DIFFIO_B0_30P	B16	IO_23_P	39.195	
BANK0	DIFFIO_B0_30N	A16	IO_23_N	40.426	
BANK1	DIFFI_B1_0P	F15	IO_24_P	39.318	DQ0_B1/DQ0_B1_GATE_OUT
BANK1	DIFFI_B1_0N/VREF_B1	F16	IO_24_N	37.534	DQ0_B1/DQ0_B1_GATE_IN
BANK1	DIFFI_B1_14P	C17	IO_25_P	40.745	DQ2_B1
BANK1	DIFFI_B1_14N	C18	IO_25_N	42.161	DQ2_B1
BANK1	DIFFI_B1_15P	F14	IO_26_P	45.849	DQS2_B1
BANK1	DIFFI_B1_15N	G14	IO_26_N	49.699	DQS2#_B1
BANK1	DIFFI_B1_16P	D17	IO_27_P	39.610	DQ2_B1
BANK1	DIFFI_B1_16N	D18	IO_27_N	40.483	DQ2_B1
BANK1	DIFFI_B1_17P	H12	IO_28_P	89.418	DQ2_B1
BANK1	DIFFI_B1_17N	G13	IO_28_N	87.849	DQ2_B1
BANK1	DIFFI_B1_18P	E16	IO_29_P	53.225	DQ2_B1
BANK1	DIFFI_B1_18N	E18	IO_29_N	51.958	DQ2_B1
BANK1	DIFFI_B1_19P	K12	IO_30_P	85.226	DQ2_B1/DQ2_B1_GATE_OUT
BANK1	DIFFI_B1_19N	K13	IO_30_N	82.940	DQ2_B1/DQ2_B1_GATE_IN
BANK1	DIFFI_B1_20P	F17	IO_31_P	42.302	DQ3_B1
BANK1	DIFFI_B1_20N	F18	IO_31_N	44.281	DQ3_B1
BANK1	DIFFI_B1_21P	H13	IO_32_P	56.251	DQ3_B1
BANK1	DIFFI_B1_21N	H14	IO_32_N	51.430	DQ3_B1
BANK1	DIFFI_B1_22P	H15	IO_33_P	37.838	DQS3_B1

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
BANK1	DIFFI_B1_22N	H16	IO_33_N	36.588	DQS3#_B1
BANK1	DIFFI_B1_23P	G16	IO_34_P	45.898	DQ3_B1
BANK1	DIFFI_B1_23N	G18	IO_34_N	39.862	DQ3_B1
BANK1	DIFFI_B1_24P	J13	IO_35_P	60.371	DQ3_B1
BANK1	DIFFI_B1_24N	K14	IO_35_N	59.219	DQ3_B1
BANK1	DIFFI_B1_25P/GCLK11/PLL1_CLK8/PLL4_CLK0/PLL5_CLK0	L12	IO_36_P	64.196	DQ3_B1
BANK1	DIFFI_B1_25N/GCLK10/PLL1_CLK9/PLL4_CLK1/PLL5_CLK1	L13	IO_36_N	58.723	DQ3_B1
BANK1	DIFFI_B1_26P/GCLK9/PLL1_CLK10/PLL4_CLK2/PLL5_CLK2	K15	IO_37_P	38.050	DQ3_B1/DQ3_B1_GATE_OUT
BANK1	DIFFI_B1_26N/GCLK8/PLL1_CLK11/PLL4_CLK3/PLL5_CLK3	K16	IO_37_N	32.983	DQ3_B1/DQ3_B1_GATE_IN
BANK1	DIFFI_B1_27P/GCLK7/PLL2_CLK0/PLL3_CLK0	L15	IO_38_P	38.562	DQ4_B1
BANK1	DIFFI_B1_27N/GCLK6/PLL2_CLK1/PLL3_CLK1	L16	IO_38_N	33.149	DQ4_B1
BANK1	DIFFI_B1_28P/GCLK5/PLL2_CLK2/PLL3_CLK2	H17	IO_39_P	38.628	DQ4_B1
BANK1	DIFFI_B1_28N/GCLK4/PLL2_CLK3/PLL3_CLK3	H18	IO_39_N	35.893	DQ4_B1
BANK1	DIFFI_B1_29P	J16	IO_40_P	48.038	DQ4_B1
BANK1	DIFFI_B1_29N	J18	IO_40_N	46.942	DQ4_B1
BANK1	DIFFI_B1_30P	K17	IO_41_P	29.382	DQS4_B1
BANK1	DIFFI_B1_30N	K18	IO_41_N	29.225	DQS4#_B1
BANK1	DIFFI_B1_31P	L17	IO_42_P	34.622	DQ4_B1
BANK1	DIFFI_B1_31N	L18	IO_42_N	35.516	DQ4_B1
BANK1	DIFFI_B1_32P	M16	IO_43_P	34.634	DQ4_B1
BANK1	DIFFI_B1_32N	M18	IO_43_N	33.840	DQ4_B1
BANK1	DIFFI_B1_33P	N17	IO_44_P	50.194	DQ5_B1/DQ4_B1_GATE_OUT
BANK1	DIFFI_B1_33N	N18	IO_44_N	49.284	DQ5_B1/DQ4_B1_GATE_IN
BANK1	DIFFI_B1_34P	P17	IO_45_P	51.923	DQ5_B1
BANK1	DIFFI_B1_34N	P18	IO_45_N	51.766	DQ5_B1
BANK1	DIFFI_B1_35P	N15	IO_46_P	49.343	DQS5_B1
BANK1	DIFFI_B1_35N	N16	IO_46_N	45.443	DQS5#_B1
BANK1	DIFFI_B1_36P	T17	IO_47_P	59.435	DQ5_B1
BANK1	DIFFI_B1_36N	T18	IO_47_N	59.652	DQ5_B1
BANK1	DIFFI_B1_37P	U17	IO_48_P	67.211	DQ5_B1
BANK1	DIFFI_B1_37N	U18	IO_48_N	67.327	DQ5_B1

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
BANK1	DIFFI_B1_38P	M14	IO_49_P	42.753	DQ5_B1
BANK1	DIFFI_B1_38N/VREF_B1	N14	IO_49_N	42.822	DQ5_B1
BANK1	DIFFI_B1_43P	L14	IO_50_N	60.952	DQ6_B1
BANK1	DIFFI_B1_43N	M13		61.455	DQ6_B1
BANK1	DIFFI_B1_55P	P15	IO_51_P	44.785	
BANK1	DIFFI_B1_55N/DOUT_BUSY	P16	IO_51_N	42.264	
BANK2	DIFFIO_B2_1N/CSO_N	V3	IO_52_N	40.384	
BANK2	DIFFIO_B2_1P/INIT_FLAG_N	U3	IO_52_P	39.523	
BANK2	DIFFIO_B2_2N/D9	P6	IO_53_N	44.413	
BANK2	DIFFIO_B2_2P/D8	N5	IO_53_P	44.548	
BANK2	DIFFIO_B2_3N	V4	IO_54_N	39.832	
BANK2	DIFFIO_B2_3P	T4	IO_54_P	39.506	
BANK2	DIFFIO_B2_4N/D6	T3	IO_55_N	59.277	
BANK2	DIFFIO_B2_4P/D5	R3	IO_55_P	59.446	
BANK2	DIFFIO_B2_14N/D4	V5	IO_56_N	48.413	
BANK2	DIFFIO_B2_14P/D3	U5	IO_56_P	49.462	
BANK2	DIFFIO_B2_15N/RWSEL/VREF_B2	T5	IO_57_N	42.009	
BANK2	DIFFIO_B2_15P/D7	R5	IO_57_P	46.360	
BANK2	DIFFIO_B2_16N	P7	IO_58_N	49.389	
BANK2	DIFFIO_B2_16P	N6	IO_58_P	49.609	
BANK2	DIFFIO_B2_17N	T7	IO_59_N	42.692	
BANK2	DIFFIO_B2_17P	R7	IO_59_P	44.394	
BANK2	DIFFIO_B2_18N	V6	IO_60_N	52.258	
BANK2	DIFFIO_B2_18P	T6	IO_60_P	55.349	
BANK2	DIFFIO_B2_19N	P8	IO_61_N	51.136	
BANK2	DIFFIO_B2_19P	N7	IO_61_P	51.647	
BANK2	DIFFIO_B2_20N	V7	IO_62_N	44.682	
BANK2	DIFFIO_B2_20P	U7	IO_62_P	45.343	
BANK2	DIFFIO_B2_22N/VREF_B2	V8	IO_63_N	42.439	
BANK2	DIFFIO_B2_22P	U8	IO_63_P	42.634	
BANK2	DIFFIO_B2_23N	N8	IO_64_N	54.952	
BANK2	DIFFIO_B2_23P	M8	IO_64_P	55.912	
BANK2	DIFFIO_B2_24N/GCLK28/PLL4_CLK4/PLL5_CLK4	V9	IO_65_N	29.520	
BANK2	DIFFIO_B2_24P/GCLK29/PLL4_CLK5/PLL5_CLK5	T9	IO_65_P	36.869	
BANK2	DIFFIO_B2_25N/GCLK30/PLL4_CLK6/PLL5_CLK6/D15	T8	IO_66_N	57.311	
BANK2	DIFFIO_B2_25P/GCLK31/PLL4_CLK7/PLL5_CLK7/D14	R8	IO_66_P	56.202	

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
BANK2	DIFFIO_B2_26N/GCLK0/PLL4_CLK8/PLL5_CLK8/ECCLK	V10	IO_67_N	38.556	
BANK2	DIFFIO_B2_26P/GCLK1/PLL4_CLK9/PLL5_CLK9/D13	U10	IO_67_P	40.119	
BANK2	DIFFIO_B2_27N/GCLK2/PLL4_CLK10/PLL5_CLK10	T10	IO_68_N	47.495	
BANK2	DIFFIO_B2_27P/GCLK3/PLL4_CLK11/PLL5_CLK11	R10	IO_68_P	54.571	
BANK2	DIFFIO_B2_28N	V11	IO_69_N	42.440	
BANK2	DIFFIO_B2_28P	U11	IO_69_P	43.650	
BANK2	DIFFIO_B2_29N	N9	IO_70_N	60.511	
BANK2	DIFFIO_B2_29P	M10	IO_70_P	59.490	
BANK2	DIFFIO_B2_31N	P11	IO_71_N	51.968	
BANK2	DIFFIO_B2_31P	N10	IO_71_P	52.965	
BANK2	DIFFIO_B2_32N	V12	IO_72_N	36.323	
BANK2	DIFFIO_B2_32P	T12	IO_72_P	36.765	
BANK2	DIFFIO_B2_35N/VREF_B2	T11	IO_73_N	35.301	
BANK2	DIFFIO_B2_35P	R11	IO_73_P	40.658	
BANK2	DIFFIO_B2_36N	N11	IO_74_N	58.501	
BANK2	DIFFIO_B2_36P	M11	IO_74_P	58.149	
BANK2	DIFFIO_B2_37N/D12	V13	IO_75_N	32.941	
BANK2	DIFFIO_B2_37P/D11	U13	IO_75_P	33.420	
BANK2	DIFFIO_B2_38N/D10	P12	IO_76_N	61.671	
BANK2	DIFFIO_B2_38P/MODE_1	N12	IO_76_P	66.116	
BANK2	DIFFIO_B2_39N/D2	V14	IO_77_N	34.214	
BANK2	DIFFIO_B2_39P/D1	T14	IO_77_P	40.935	
BANK2	DIFFIO_B2_46N	V15	IO_78_N	33.804	
BANK2	DIFFIO_B2_46P	U15	IO_78_P	33.711	
BANK2	DIFFIO_B2_52N/CS_N	T13	IO_79_N	63.343	
BANK2	DIFFIO_B2_52P/D0	R13	IO_79_P	72.007	
BANK2	DIFFIO_B2_53N	V16	IO_80_N	40.570	
BANK2	DIFFIO_B2_53P	U16	IO_80_P	42.518	
BANK2	DIFFIO_B2_54N/MODE_0	T15	IO_81_N	40.597	
BANK2	DIFFIO_B2_54P/CFG_CLK	R15	IO_81_P	38.470	
BANK3	DIFFI_B3_0N/VREF_B3	C1	IO_82_N	34.682	DQ0_B3/DQ0_B3_GATE_IN
BANK3	DIFFI_B3_0P	C2	IO_82_P	34.744	DQ0_B3/DQ0_B3_GATE_OUT
BANK3	DIFFI_B3_14N	F5	IO_83_N	42.731	DQ2_B3
BANK3	DIFFI_B3_14P	F6	IO_83_P	47.629	DQ2_B3

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
BANK3	DIFFI_B3_15N	D3	IO_84_N	42.470	DQS2#_B3
BANK3	DIFFI_B3_15P	E4	IO_84_P	45.257	DQS2_B3
BANK3	DIFFI_B3_16N	E1	IO_85_N	41.729	DQ2_B3
BANK3	DIFFI_B3_16P	E3	IO_85_P	46.697	DQ2_B3
BANK3	DIFFI_B3_17N	D1	IO_86_N	56.108	DQ2_B3
BANK3	DIFFI_B3_17P	D2	IO_86_P	57.996	DQ2_B3
BANK3	DIFFI_B3_18N	F3	IO_87_N	33.044	DQ2_B3
BANK3	DIFFI_B3_18P	F4	IO_87_P	38.492	DQ2_B3
BANK3	DIFFI_B3_19N	G6	IO_88_N	65.799	DQ2_B3/DQ2_B3_GATE_IN
BANK3	DIFFI_B3_19P	H7	IO_88_P	66.553	DQ2_B3/DQ2_B3_GATE_OUT
BANK3	DIFFI_B3_20N	H5	IO_89_N	45.063	DQ3_B3/DQ3_B3_GATE_IN
BANK3	DIFFI_B3_20P	H6	IO_89_P	46.956	DQ3_B3/DQ3_B3_GATE_OUT
BANK3	DIFFI_B3_21N	F1	IO_90_N	51.222	DQ3_B3
BANK3	DIFFI_B3_21P	F2	IO_90_P	51.997	DQ3_B3
BANK3	DIFFI_B3_22N	J6	IO_91_N	50.849	DQ3_B3
BANK3	DIFFI_B3_22P	J7	IO_91_P	53.108	DQ3_B3
BANK3	DIFFI_B3_23N	G1	IO_92_N	44.302	DQ3_B3
BANK3	DIFFI_B3_23P	G3	IO_92_P	46.399	DQ3_B3
BANK3	DIFFI_B3_24N	K6	IO_93_N	54.000	DQS3#_B3
BANK3	DIFFI_B3_24P	L7	IO_93_P	56.876	DQS3_B3
BANK3	DIFFI_B3_25N/GCLK20/PLL1_CLK12/PLL4_CLK4/PLL5_CLK4	H3	IO_94_N	45.832	DQ3_B3
BANK3	DIFFI_B3_25P/GCLK21/PLL1_CLK13/PLL4_CLK5/PLL5_CLK5	H4	IO_94_P	57.290	DQ3_B3
BANK3	DIFFI_B3_26N/GCLK22/PLL1_CLK14/PLL4_CLK6/PLL5_CLK6	K5	IO_95_N	44.432	DQ3_B3/DQ4_B3_GATE_IN
BANK3	DIFFI_B3_26P/GCLK23/PLL1_CLK15/PLL4_CLK7/PLL5_CLK7	L5	IO_95_P	44.748	DQ3_B3/DQ4_B3_GATE_OUT
BANK3	DIFFI_B3_27N/GCLK24/PLL2_CLK4/PLL3_CLK4	K3	IO_96_N	39.718	DQ4_B3
BANK3	DIFFI_B3_27P/GCLK25/PLL2_CLK5/PLL3_CLK5	K4	IO_96_P	46.732	DQ4_B3
BANK3	DIFFI_B3_28N/GCLK26/PLL2_CLK6/PLL3_CLK6	H1	IO_97_N	36.741	DQ4_B3
BANK3	DIFFI_B3_28P/GCLK27/PLL2_CLK7/PLL3_CLK7	H2	IO_97_P	39.497	DQ4_B3
BANK3	DIFFI_B3_29N	J1	IO_98_N	45.196	DQ4_B3

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
BANK3	DIFFI_B3_29P	J3	IO_98_P	49.343	DQ4_B3
BANK3	DIFFI_B3_30N	L3	IO_99_N	39.200	DQS4#_B3
BANK3	DIFFI_B3_30P	L4	IO_99_P	40.899	DQS4_B3
BANK3	DIFFI_B3_31N	K1	IO_100_N	40.670	DQ4_B3
BANK3	DIFFI_B3_31P	K2	IO_100_P	42.636	DQ4_B3
BANK3	DIFFI_B3_32N	L1	IO_101_N	42.317	DQ4_B3
BANK3	DIFFI_B3_32P	L2	IO_101_P	42.468	DQ4_B3
BANK3	DIFFI_B3_33N	M1	IO_102_N	37.300	DQ5_B3
BANK3	DIFFI_B3_33P	M3	IO_102_P	50.920	DQ5_B3
BANK3	DIFFI_B3_34N	N1	IO_103_N	48.363	DQ5_B3
BANK3	DIFFI_B3_34P	N2	IO_103_P	43.127	DQ5_B3
BANK3	DIFFI_B3_35N	P1	IO_104_N	44.721	DQS5#_B3
BANK3	DIFFI_B3_35P	P2	IO_104_P	46.413	DQS5_B3
BANK3	DIFFI_B3_36N	T1	IO_105_N	51.812	DQ5_B3
BANK3	DIFFI_B3_36P	T2	IO_105_P	51.979	DQ5_B3
BANK3	DIFFI_B3_37N	U1	IO_106_N	56.117	DQ5_B3
BANK3	DIFFI_B3_37P	U2	IO_106_P	58.628	DQ5_B3
BANK3	DIFFI_B3_38N/VREF_B3	M5	IO_107_N	50.391	DQ5_B3
BANK3	DIFFI_B3_38P	L6	IO_107_P	51.673	DQ5_B3
BANK3	DIFFI_B3_56N	P3	IO_108_N	36.326	DQ8_B3
BANK3	DIFFI_B3_56P	P4	IO_108_P	37.276	DQ8_B3
BANK3	DIFFI_B3_57N/VREF_B3	N3	IO_109_N	49.305	DQ8_B3
BANK3	DIFFI_B3_57P	N4	IO_109_P	50.674	DQ8_B3
	TCK	A17		38.664	
	TMS	B18		43.431	
	TDI	D15		31.024	
	TDO	D16		30.631	
	CMPCS_B	P13		55.642	
	RST_N	V2		42.758	
	CFG_DONE	V17		40.696	
	VCC	G7			
	VCC	H9			
	VCC	H11			
	VCC	J8			
	VCC	J10			
	VCC	K9			
	VCC	K11			
	VCC	L8			
	VCC	L10			

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	VCC	M7			
	VCC	M12			
	VCCAUX	B1			
	VCCAUX	B17			
	VCCAUX	E5			
	VCCAUX	E9			
	VCCAUX	E14			
	VCCAUX	G10			
	VCCAUX	J12			
	VCCAUX	K7			
	VCCAUX	M9			
	VCCAUX	P5			
	VCCAUX	P10			
	VCCAUX	P14			
	VCCIO0	B5			
	VCCIO0	B10			
	VCCIO0	B15			
	VCCIO0	D7			
	VCCIO0	D13			
	VCCIO0	E10			
	VCCIO1	E17			
	VCCIO1	G15			
	VCCIO1	J14			
	VCCIO1	J17			
	VCCIO1	M15			
	VCCIO1	R17			
	VCCIO2	P9			
	VCCIO2	R6			
	VCCIO2	R12			
	VCCIO2	U4			
	VCCIO2	U9			
	VCCIO2	U14			
	VCCIO3	E2			
	VCCIO3	G4			
	VCCIO3	J2			
	VCCIO3	J5			
	VCCIO3	M4			
	VCCIO3	R2			
	VCCEFUSE	R14			

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	VSS	A1			
	VSS	A18			
	VSS	B7			
	VSS	B13			
	VSS	C3			
	VSS	C16			
	VSS	D5			
	VSS	D10			
	VSS	E15			
	VSS	G2			
	VSS	G5			
	VSS	G12			
	VSS	G17			
	VSS	H8			
	VSS	H10			
	VSS	J4			
	VSS	J9			
	VSS	J11			
	VSS	J15			
	VSS	K8			
	VSS	K10			
	VSS	L9			
	VSS	L11			
	VSS	M2			
	VSS	M6			
	VSS	M17			
	VSS	N13			
	VSS	R1			
	VSS	R4			
	VSS	R9			
	VSS	R18			
	VSS	T16			
	VSS	U6			
	VSS	U12			
	VSS	V1			
	VSS	V18			
	NC	C12			
	NC	D12			
	NC	E6			

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	NC	E7			
	NC	E8			
	NC	E11			
	NC	E12			
	NC	F7			
	NC	F8			
	NC	F10			
	NC	F11			
	NC	F12			
	NC	G8			
	NC	G11			
	STAND_BY	R16			

Chapter 5 Thermal Resistance

Table 5-1 Thermal Resistance Data

θJA(°C/W) (Flow: 0m/s)	**θJB (°C/W)**	**θJC (°C/W)**	**θJA(°C/W) (Flow: 1m/s)**	**θJA(°C/W) (Flow: 2m/s)**
19.9	11.3	5.6	17.4	15.7

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