PK03005_PGC1KG_FBG256

(V1.7)

(10.06. 2022)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.7	10.06. 2022	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

The PGC1KG_FBG256 device is packaged with a Wire Bond Ball Grid Array. Its package size is 17x17mm, with 256 solder balls, a pitch of 1.0mm, and a maximum package thickness of 1.57mm.

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Data

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
D	16.9	17.0	17.1	A	1.27	1.42	1.57
D1	-	15.0	-	A1	0.32	0.37	0.42
E	16.9	17.0	17.1	A2	1.0	1.05	1.10
E1	-	15.0	-	c	0.31	0.35	0.39
b	0.45	0.5	0.55	e	-	1.0	-
aaa	0.200			ddd	0.200		
bbb	0.250			eee	0.250		
fff	0.100						

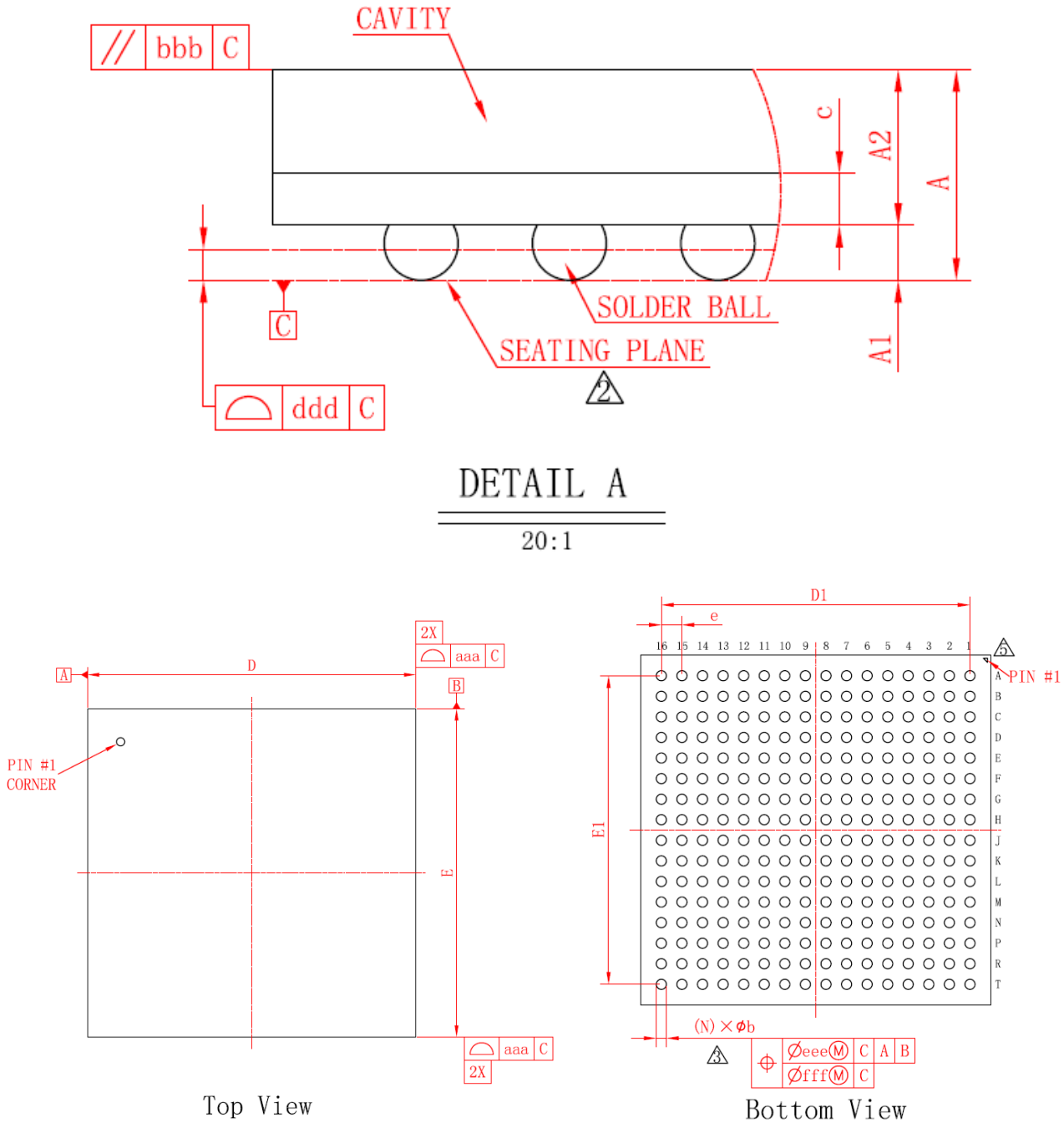

Figure 2-1 Package Outline Dimension (POD)

Note: PIN #1 indicates the position of the first pin.

2.2 Pin Description

The PGC1KG_FBG256 device has 207 user I/Os.

Table 2-2 Device Pin Definitions

Pin Name	Pin Type	Direction	Pin Description
User I/O Pin			
DIFF[I,IO]_XX_NN[P,N]	User pin	Input/Output	User I/O. (1) DIFFI indicates support for differential signal input

Pin Name	Pin Type	Direction	Pin Description
			and pseudo-differential output; DIFFIO indicates support for differential signal input and true differential output, which can be used for transmitting and receiving LVDS signals; (2) “XX” denotes the Bank number, with possible values being B0, B1, B2, B3, B4, and B5; (3) “NN” denotes the sequence number of the programmable I/O group within the Bank, starting from 0 and increasing incrementally; (4) [P,N]: “P” denotes the positive side of the differential pair, and “N” denotes the negative side; During power-up, the user I/O is at a low voltage; After power-up is complete but before configuration, the general user I/O is at pull-down status; During configuration, the user I/O is at pull-down status;
Configuration[1]			
INIT_FLAG_N	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When used as a configuration pin: During power-up, it is at a low voltage; After power-up is complete before configuration, it is open-drain at weak pull-up status; During configuration, it is open-drain at weak pull-up status; During initialization, the pin can be driven to a low voltage by an external input to indicate an error or to delay configuration. During configuration, the pin serves as an indicator output for configuration errors, where a low voltage indicates an error has occurred;
CFG_DONE	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When it is used as configuration pin, it serves as an indicator output for configuration completion, where a high voltage indicates configuration is complete; Before or during configuration, the pin is driven to a low voltage; after configuration is complete, the pin can continue to be driven to a low voltage by an external source. If the internal start-up timing detects CFG_DONE at a low voltage, the internal start-up circuitry maintains its state until CFG_DONE goes high to continue the start-up process;
RSTN	Multi-function pin	Input	Configurable multiplexed reset pin, with an internal weak pull-up resistor. When it is used as a reset pin, it serves to restart the configuration process, active low. At this situation, it must be pulled up with an external resistor (internal weak pull-up resistor typically has a value of over 20kOhms, with a relatively weak pull-up strength); when the pin is at a low voltage, the CPLD enters reset state, with all I/Os in a weak pull-down status;
CFG_CLK	Multi-function pin	Input/Output	Configurable multiplexed clock pin, with an internal weak pull-up resistor. When it is used as a configuration pin: In slave SPI configuration mode, the pin serves as a clock input to acquire configuration data from an external source; In master SPI configuration mode, the pin serves as a clock output to acquire configuration data from an external source; in this mode, a 1kOhms pull-up resistor

Pin Name	Pin Type	Direction	Pin Description
			is needed; Master SPI mode and slave SPI mode are allowed to be enabled simultaneously, but using them at the same time is not permitted;
TCK	Multi-function pin	Input	Multiplexed JTAG test clock input pin; requires an external 4.7kOhms pull-down resistor;
TMS	Multi-function pin	Input	Multiplexed JTAG test mode select input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDI	Multi-function pin	Input	Multiplexed JTAG test data input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDO	Multi-function pin	Output	Multiplexed JTAG test data output pin; with an internal weak pull-up resistor, pulled up to VCCIO0.
JTAGEN	Multi-function pin	Input	Optional JTAG port behaviour control pin, usually used in user mode, when JTAG pins are configured as configuration I/Os, this pin is user I/O, with the state controlled by the user; when JTAG pins serve as user I/Os, JTAGEN serves as a dedicated input used to control the availability of JTAG pins; the default state is weak pull-down; when JTAGEN is configured as a dedicated I/O: (1) When at a low voltage, the JTAG pins function as user I/Os; (2) When at a high voltage, the JTAG pins function as JTAG configuration port.
FCS_N	Multi-function pin	Output	Configurable multiplexed pin, used for master SPI configuration mode, (1) In master SPI mode, outputs an active-low chip select signal to an external Flash; (2) After configuration is completed, it can be used as a user I/O.
MISO_SO	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MISO, serial data input in master SPI mode; (2) SO, serial data output in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
MOSI_SI	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MOSI, serial data output in master SPI mode; (2) SI, serial data input in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
FCSI_N	Multi-function pin	Input	Configurable multiplexed pin, with an internal weak pull-up resistor; In slave SPI mode, active-low chip select input.
SCL	Multi-function pin	Input (Open-drain)	Configurable multiplexed pin, clock input in slave I2C mode; requires an external weak pull-up resistor.
SDA	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, data input/output in I2C mode; requires an external weak pull-up resistor.
SPAL_CLK	Multi-function pin	Input	Clock input in slave parallel X16 configuration mode.
SPAL_CS_N	Multi-function pin	Input	Chip select input in slave parallel X16 configuration mode. Active-low

Pin Name	Pin Type	Direction	Pin Description
SPAL_RDWR_N	Multi-function pin	Input	Read/write control input in slave parallel X16 configuration mode; 1: read; 0: write.
SPAL_BUSY	Multi-function pin	Output	Busy indicator in slave parallel X16 configuration mode; During readback, if the data is not ready, SPAL_BUSY changes to high voltage.
SPAL_D15~SPAL_D0	Multi-function pin	Input/Output	Data bus in slave parallel X16 configuration mode.
Clock, PLL			
CLK[0,1,2][P,N]_[B0,B1,…,B5]	Multi-function pin	Input	Global clock input pin; can also be used as user I/O; (1) [0,1,2]: clock pin numbers; (2) [P,N]: positive and negative sides of the differential clock pins; (3) [B0,B1,…,B5]: bank numbers.
PLL[0,1]_CLKIN_[P,N]	Multi-function pin	Input	PLL input. PLL can choose to directly input a clock from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
PLL[0,1]_CLKFB_[P,N]	Multi-function pin	Input	Optional PLL feedback clock input. PLL can select to feedback clock externally from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
Power			
VCC		Power	External power supply of 2.5V or 3.3V, providing power to the core logic.
VCCIO[0,1,2,3,4,5]		Power	I/O Bank power.
VSS		Ground	Ground associated with VCC;

Note:

1. When the configured multi-function pin is used as a user I/O, its status is the same as the user I/O pin.

2.2.1 Pinout Diagram

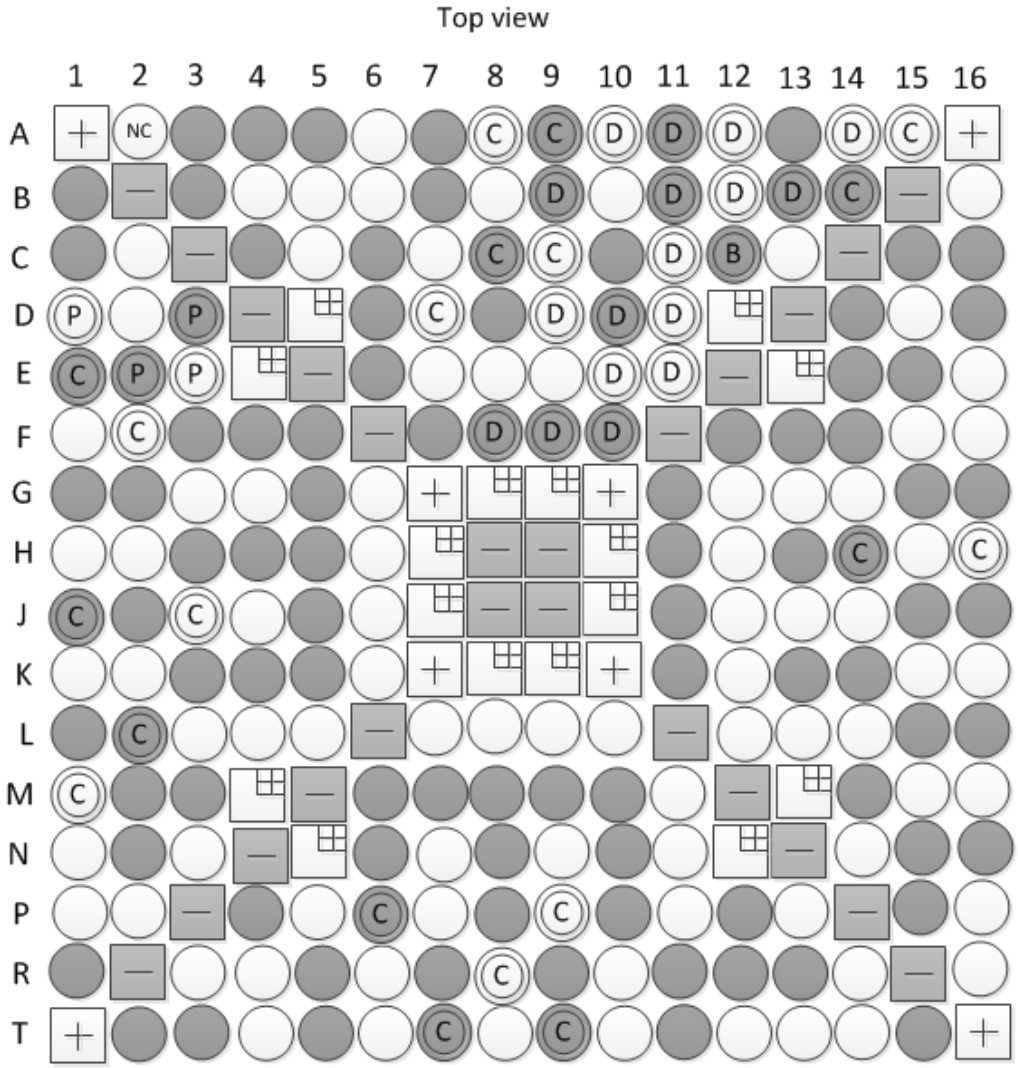

Figure 2-2 Pinout Diagram

Note: The Pinout symbols are explained as below:

General IO	DIFFIO*	COMP(N) TRUE(P)
Multiplex IO	DIFFIO*/D0~D31 DIFFIO*/CLK* DIFFIO*/PLL*	D D C C P P
Power , Ground	VSS VCC VCCIO	

Figure 2-3 Pinout Symbols

2.2.2 IO Banks

Top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A			B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	
B	B5		B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0		B1
C	B5	B5		B0	B0	B0	B0	B0	B0	B0	B0	B0	B0		B1	B1
D	B5	B5	B5			B0	B0	B0	B0	B0	B0			B1	B1	B1
E	B5	B5	B5			B0	B0	B0	B0	B0	B0			B1	B1	B1
F	B5	B5	B5	B5	B5		B0	B0	B0	B0		B1	B1	B1	B1	B1
G	B4	B5	B5	B5	B5	B5					B1	B1	B1	B1	B1	B1
H	B4	B4	B4	B4	B4	B5					B1	B1	B1	B1	B1	B1
J	B4	B4	B4	B4	B4	B4					B1	B1	B1	B1	B1	B1
K	B4	B4	B4	B3	B3	B4					B1	B1	B1	B1	B1	B1
L	B3	B3	B3	B3	B3		B2	B2	B2	B2		B1	B1	B1	B1	B1
M	B3	B3	B3			B2	B2	B2	B2	B2	B2			B1	B1	B1
N	B3	B3	B3			B2	B2	B2	B2	B2	B2			B1	B1	B1
P	B3	B3		B2	B2	B2	B2	B2	B2	B2	B2	B2	B2		B1	B1
R	B3		B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2		B1
T		B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	

Figure 2-4 IO Banks

2.2.3 Power and GND Placement

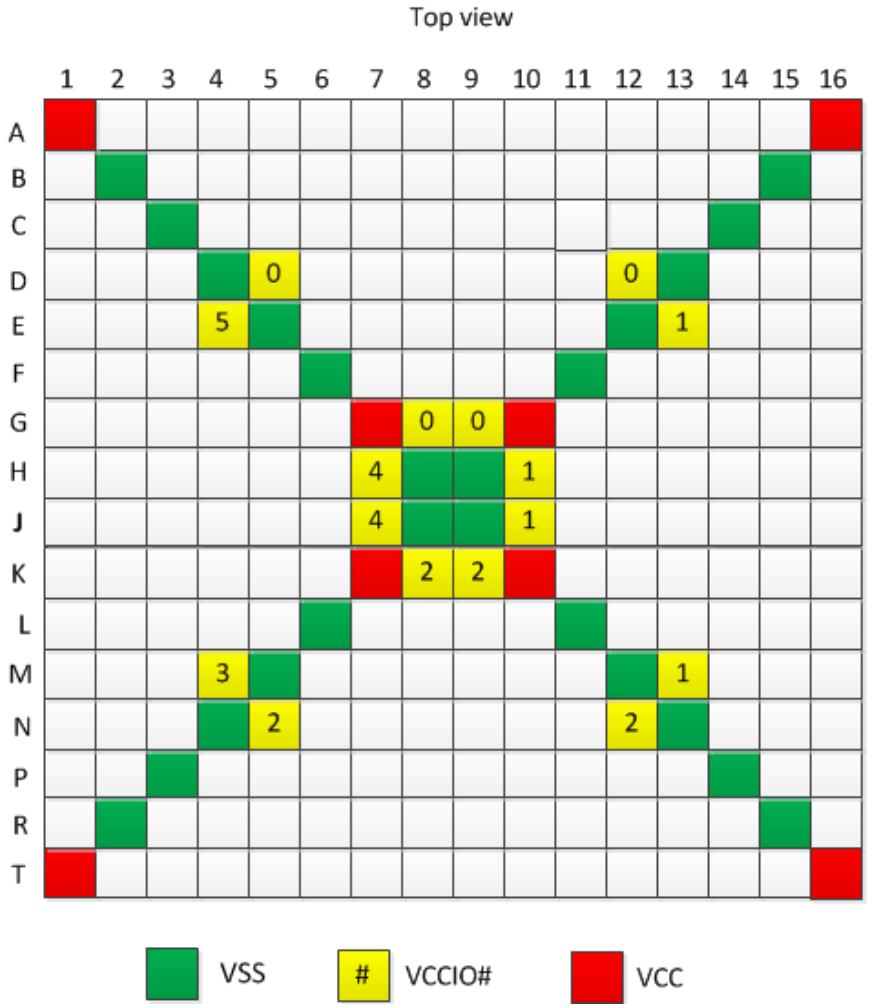

Figure 2-5 Power and GND Placement

2.2.4 Pin Name List

Table 2-3 Pin Name List

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFI_B0_0N/CFG_DONE	C13	IO_1_N	71.48
B0	DIFFI_B0_0P/INIT_FLAG_N	A13	IO_1_P	74.62
B0	DIFFIO_B0_1N/SPAL_CLK	A15	IO_2_N	83.95
B0	DIFFIO_B0_1P/SPAL_CS_N	B14	IO_2_P	82.3
B0	DIFFIO_B0_3N/SPAL_RDWR_N	B12	IO_4_N	60.25
B0	DIFFIO_B0_3P/SPAL_BUSY	C12	IO_4_P	49.57
B0	DIFFI_B0_4N/SPAL_D15	A14	IO_5_N	71.99
B0	DIFFI_B0_4P/SPAL_D14	B13	IO_5_P	87.43
B0	DIFFIO_B0_5N/SPAL_D13	A12	IO_6_N	72.11
B0	DIFFIO_B0_5P/SPAL_D12	B11	IO_6_P	68.13
B0	DIFFI_B0_6N/SPAL_D11	D11	IO_7_N	61.66
B0	DIFFI_B0_6P/SPAL_D10	F10	IO_7_P	60.91
B0	DIFFIO_B0_7N/SPAL_D9	C11	IO_8_N	68.72
B0	DIFFIO_B0_7P/SPAL_D8	A11	IO_8_P	69.88
B0	DIFFI_B0_8N/RSTN	B10	IO_9_N	58.51
B0	DIFFI_B0_8P/JTAGEN	C10	IO_9_P	55.46
B0	DIFFIO_B0_9N/SPAL_D7	E10	IO_10_N	51.99
B0	DIFFIO_B0_9P/SPAL_D6	D10	IO_10_P	50.35
B0	DIFFI_B0_10N/SPAL_D5	E11	IO_11_N	65.63
B0	DIFFI_B0_10P/SPAL_D4	F9	IO_11_P	64.33
B0	DIFFIO_B0_11N/SPAL_D3	A10	IO_12_N	68.4
B0	DIFFIO_B0_11P/SPAL_D2	B9	IO_12_P	66.67
B0	DIFFI_B0_12N/SDA/CLK0N_B0	C9	IO_13_N	70.19
B0	DIFFI_B0_12P/SCL/CLK0P_B0	A9	IO_13_P	69.89
B0	DIFFIO_B0_13N/SPAL_D1	D9	IO_14_N	46.91
B0	DIFFIO_B0_13P/SPAL_D0	F8	IO_14_P	48.34
B0	DIFFI_B0_14N	E9	IO_15_N	38.98
B0	DIFFI_B0_14P	D8	IO_15_P	50.07
B0	DIFFIO_B0_15N/CLK1N_B0	A8	IO_16_N	67.13
B0	DIFFIO_B0_15P/CLK1P_B0	C8	IO_16_P	67.65
B0	DIFFI_B0_16N/TMS	B8	IO_17_N	64.92
B0	DIFFI_B0_16P/TCK	A7	IO_17_P	67.73
B0	DIFFIO_B0_17N	E8	IO_18_N	43.04
B0	DIFFIO_B0_17P	F7	IO_18_P	32.46
B0	DIFFI_B0_18N	D7	IO_19_N	56.94
B0	DIFFI_B0_18P	E6	IO_19_P	57.01
B0	DIFFIO_B0_19N	C7	IO_20_N	45.35

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFIO_B0_19P	B7	IO_20_P	47.17
B0	DIFFI_B0_20N/TDI	A6	IO_21_N	59.58
B0	DIFFI_B0_20P/TDO	C6	IO_21_P	68.69
B0	DIFFIO_B0_21N	E7	IO_22_N	52.42
B0	DIFFIO_B0_21P	D6	IO_22_P	49.08
B0	DIFFI_B0_22N	B4	IO_23_N	93.33
B0	DIFFI_B0_22P	A3	IO_23_P	78.43
B0	DIFFIO_B0_23N	B6	IO_24_N	68.04
B0	DIFFIO_B0_23P	A5	IO_24_P	70.63
B0	DIFFIO_B0_25N	C5	IO_26_N	71.88
B0	DIFFIO_B0_25P	A4	IO_26_P	73.97
B0	DIFFI_B0_26P	B3	IO_27_P	68.27
B0	DIFFIO_B0_27N	B5	IO_28_N	73.76
B0	DIFFIO_B0_27P	C4	IO_28_P	74.05
B1	DIFFI_B1_0P	D14	IO_29_P	78.1
B1	DIFFI_B1_0N	E15	IO_29_N	78.45
B1	DIFFI_B1_1P	C15	IO_30_P	88.6
B1	DIFFI_B1_1N	B16	IO_30_N	93.49
B1	DIFFI_B1_2P	D16	IO_31_P	77.26
B1	DIFFI_B1_2N	E14	IO_31_N	71.73
B1	DIFFI_B1_3P	C16	IO_32_P	96.53
B1	DIFFI_B1_3N	D15	IO_32_N	98.34
B1	DIFFI_B1_4P	E16	IO_33_P	73.5
B1	DIFFI_B1_4N	F15	IO_33_N	74.04
B1	DIFFI_B1_5P	F13	IO_34_P	57.03
B1	DIFFI_B1_5N	G12	IO_34_N	55.57
B1	DIFFI_B1_6P	F14	IO_35_P	65.96
B1	DIFFI_B1_6N	F16	IO_35_N	58.35
B1	DIFFI_B1_7P	F12	IO_36_P	55.38
B1	DIFFI_B1_7N	G13	IO_36_N	57.4
B1	DIFFI_B1_8P	G15	IO_37_P	57.45
B1	DIFFI_B1_8N	G14	IO_37_N	54.67
B1	DIFFI_B1_9P	G11	IO_38_P	54.52
B1	DIFFI_B1_9N	H12	IO_38_N	53.3
B1	DIFFI_B1_10P	G16	IO_39_P	56.27
B1	DIFFI_B1_10N	H15	IO_39_N	64.83
B1	DIFFI_B1_11P	H13	IO_40_P	55.98
B1	DIFFI_B1_11N	J12	IO_40_N	54.16
B1	DIFFI_B1_12P/CLK0P_B1	H14	IO_41_P	66.46

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B1	DIFFI_B1_12N/CLK0N_B1	H16	IO_41_N	68.17
B1	DIFFI_B1_13P	J16	IO_42_P	67.18
B1	DIFFI_B1_13N	J14	IO_42_N	65.16
B1	DIFFI_B1_14P	J15	IO_43_P	53.99
B1	DIFFI_B1_14N	K16	IO_43_N	68.37
B1	DIFFI_B1_15P	H11	IO_44_P	55.66
B1	DIFFI_B1_15N	J13	IO_44_N	51.92
B1	DIFFI_B1_16P	K14	IO_45_P	55.66
B1	DIFFI_B1_16N	K15	IO_45_N	48.74
B1	DIFFI_B1_17P	J11	IO_46_P	55.52
B1	DIFFI_B1_17N	L12	IO_46_N	55.17
B1	DIFFI_B1_18P	L16	IO_47_P	57.65
B1	DIFFI_B1_18N	L14	IO_47_N	65.67
B1	DIFFI_B1_19P	K13	IO_48_P	39.7
B1	DIFFI_B1_19N	K12	IO_48_N	41.69
B1	DIFFI_B1_20P	L15	IO_49_P	71.64
B1	DIFFI_B1_20N	M16	IO_49_N	72.5
B1	DIFFI_B1_21P	K11	IO_50_P	51.15
B1	DIFFI_B1_21N	L13	IO_50_N	55.42
B1	DIFFI_B1_22P	M14	IO_51_P	53.25
B1	DIFFI_B1_22N	M15	IO_51_N	65.07
B1	DIFFI_B1_23P	N15	IO_52_P	87.1
B1	DIFFI_B1_23N	P16	IO_52_N	74.54
B1	DIFFI_B1_24P	N16	IO_53_P	75.83
B1	DIFFI_B1_24N	N14	IO_53_N	73.6
B1	DIFFI_B1_25P	P15	IO_54_P	82.59
B1	DIFFI_B1_25N	R16	IO_54_N	79.2
B2	DIFFI_B2_0N	R14	IO_55_N	87.19
B2	DIFFI_B2_0P	T15	IO_55_P	90.03
B2	DIFFI_B2_1N/MOSI_SI	P13	IO_56_N	75.56
B2	DIFFI_B2_1P/FCSI_N	R12	IO_56_P	78.98
B2	DIFFI_B2_3N	T13	IO_58_N	77.26
B2	DIFFI_B2_3P	P12	IO_58_P	71.11
B2	DIFFI_B2_4N	T14	IO_59_N	93.04
B2	DIFFI_B2_4P	R13	IO_59_P	94.28
B2	DIFFI_B2_5N	T12	IO_60_N	73.1
B2	DIFFI_B2_5P	R11	IO_60_P	72.32
B2	DIFFI_B2_6N	N11	IO_61_N	56.07
B2	DIFFI_B2_6P	M10	IO_61_P	50.87

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B2	DIFFI_B2_7N	P11	IO_62_N	68.28
B2	DIFFI_B2_7P	T11	IO_62_P	59.59
B2	DIFFI_B2_8N	M11	IO_63_N	58.45
B2	DIFFI_B2_8P	N10	IO_63_P	58.95
B2	DIFFI_B2_9N	R10	IO_64_N	48.55
B2	DIFFI_B2_9P	P10	IO_64_P	55.62
B2	DIFFI_B2_10N	L10	IO_65_N	56.75
B2	DIFFI_B2_10P	M9	IO_65_P	53.03
B2	DIFFI_B2_11N	T10	IO_66_N	66.42
B2	DIFFI_B2_11P	R9	IO_66_P	63.43
B2	DIFFI_B2_12N	N9	IO_67_N	59.46
B2	DIFFI_B2_12P	M8	IO_67_P	56.73
B2	DIFFI_B2_13N/CLK1N_B2	P9	IO_68_N	65.96
B2	DIFFI_B2_13P/CLK1P_B2	T9	IO_68_P	64.59
B2	DIFFI_B2_14N	L9	IO_69_N	58.06
B2	DIFFI_B2_14P	N8	IO_69_P	57.25
B2	DIFFI_B2_15N	T8	IO_70_N	69.15
B2	DIFFI_B2_15P	P8	IO_70_P	62.93
B2	DIFFI_B2_16N	L8	IO_71_N	64.7
B2	DIFFI_B2_16P	M6	IO_71_P	64.79
B2	DIFFI_B2_17N/CLK0N_B2	R8	IO_72_N	64.73
B2	DIFFI_B2_17P/CLK0P_B2	T7	IO_72_P	67.5
B2	DIFFI_B2_18N	N7	IO_73_N	54.49
B2	DIFFI_B2_18P	M7	IO_73_P	57.72
B2	DIFFI_B2_19N	P7	IO_74_N	62.7
B2	DIFFI_B2_19P	R7	IO_74_P	52.91
B2	DIFFI_B2_20N	L7	IO_75_N	56.14
B2	DIFFI_B2_20P	N6	IO_75_P	56.69
B2	DIFFI_B2_21N/MISO_SO	T6	IO_76_N	73.93
B2	DIFFI_B2_21P/CFG_CLK	P6	IO_76_P	64.08
B2	DIFFI_B2_22N	R4	IO_77_N	79.66
B2	DIFFI_B2_22P	T3	IO_77_P	85.19
B2	DIFFI_B2_23N	R6	IO_78_N	71.92
B2	DIFFI_B2_23P	T5	IO_78_P	70.98
B2	DIFFI_B2_25N	P5	IO_80_N	66.93
B2	DIFFI_B2_25P/FCS_N	R5	IO_80_P	69.46
B2	DIFFI_B2_26N	R3	IO_81_N	86.81
B2	DIFFI_B2_26P	T2	IO_81_P	83.59
B2	DIFFI_B2_27N	T4	IO_82_N	78.56

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B2	DIFFI_B2_27P	P4	IO_82_P	72.9
B3	DIFFI_B3_0P	L1	IO_83_P	57.18
B3	DIFFI_B3_0N	L3	IO_83_N	70.22
B3	DIFFI_B3_1P	K4	IO_84_P	57.69
B3	DIFFI_B3_1N	L5	IO_84_N	57.75
B3	DIFFI_B3_2P/CLK0P_B3	L2	IO_85_P	69.71
B3	DIFFI_B3_2N/CLK0N_B3	M1	IO_85_N	72.16
B3	DIFFI_B3_3P	K5	IO_86_P	44.9
B3	DIFFI_B3_3N	L4	IO_86_N	35.01
B3	DIFFI_B3_4P	M3	IO_87_P	66.17
B3	DIFFI_B3_4N	N1	IO_87_N	72.48
B3	DIFFI_B3_5P	N2	IO_88_P	76.98
B3	DIFFI_B3_5N	P1	IO_88_N	78.17
B3	DIFFI_B3_6P	M2	IO_89_P	68.51
B3	DIFFI_B3_6N	N3	IO_89_N	63.74
B3	DIFFI_B3_7P	R1	IO_90_P	83.97
B3	DIFFI_B3_7N	P2	IO_90_N	78.48
B4	DIFFI_B4_0P	G1	IO_91_P	61.81
B4	DIFFI_B4_0N	H2	IO_91_N	49.43
B4	DIFFI_B4_1P	H4	IO_92_P	57.88
B4	DIFFI_B4_1N	J6	IO_92_N	55.55
B4	DIFFI_B4_2P	H3	IO_93_P	61.65
B4	DIFFI_B4_2N	H1	IO_93_N	53.6
B4	DIFFI_B4_3P/CLK0P_B4	J1	IO_94_P	68.36
B4	DIFFI_B4_3N/CLK0N_B4	J3	IO_94_N	63.18
B4	DIFFI_B4_4P	J2	IO_95_P	68.78
B4	DIFFI_B4_4N	K1	IO_95_N	67.66
B4	DIFFI_B4_5P	H5	IO_96_P	54.22
B4	DIFFI_B4_5N	J4	IO_96_N	54.94
B4	DIFFI_B4_6P	K3	IO_97_P	42.19
B4	DIFFI_B4_6N	K2	IO_97_N	58.68
B4	DIFFI_B4_7P	J5	IO_98_P	44.45
B4	DIFFI_B4_7N	K6	IO_98_N	54.48
B5	DIFFI_B5_0P/PLL0_CLKFB_P	D3	IO_99_P	73.81
B5	DIFFI_B5_0N/PLL0_CLKFB_N	D1	IO_99_N	79.97
B5	DIFFI_B5_1P	B1	IO_100_P	79.76
B5	DIFFI_B5_1N	C2	IO_100_N	71.03
B5	DIFFI_B5_2P/PLL0_CLKIN_P	E2	IO_101_P	67.59
B5	DIFFI_B5_2N/PLL0_CLKIN_N	E3	IO_101_N	51.7

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B5	DIFFI_B5_3P	C1	IO_102_P	69.93
B5	DIFFI_B5_3N	D2	IO_102_N	76.79
B5	DIFFI_B5_4P/CLK0P_B5	E1	IO_103_P	72.86
B5	DIFFI_B5_4N/CLK0N_B5	F2	IO_103_N	68
B5	DIFFI_B5_5P	F4	IO_104_P	51.79
B5	DIFFI_B5_5N	G6	IO_104_N	55.12
B5	DIFFI_B5_6P	F3	IO_105_P	60.8
B5	DIFFI_B5_6N	F1	IO_105_N	73.66
B5	DIFFI_B5_7P	G5	IO_106_P	60.47
B5	DIFFI_B5_7N	G4	IO_106_N	59.97
B5	DIFFI_B5_8P	G2	IO_107_P	58.51
B5	DIFFI_B5_8N	G3	IO_107_N	45.02
B5	DIFFI_B5_9P	F5	IO_108_P	62.07
B5	DIFFI_B5_9N	H6	IO_108_N	59.82
	VCC	A1		
	VCC	A16		
	VCC	G7		
	VCC	G10		
	VCC	K7		
	VCC	K10		
	VCC	T1		
	VCC	T16		
	NC	A2		
	VCCIO0	D5		
	VCCIO0	D12		
	VCCIO0	G8		
	VCCIO0	G9		
	VCCIO1	E13		
	VCCIO1	H10		
	VCCIO1	J10		
	VCCIO1	M13		
	VCCIO2	K8		
	VCCIO2	K9		
	VCCIO2	N5		
	VCCIO2	N12		
	VCCIO3	M4		
	VCCIO4	H7		
	VCCIO4	J7		
	VCCIO5	E4		

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
	VSS	B2		
	VSS	B15		
	VSS	C3		
	VSS	C14		
	VSS	D4		
	VSS	D13		
	VSS	E5		
	VSS	E12		
	VSS	F6		
	VSS	F11		
	VSS	H8		
	VSS	H9		
	VSS	J8		
	VSS	J9		
	VSS	L6		
	VSS	L11		
	VSS	M5		
	VSS	M12		
	VSS	N4		
	VSS	N13		
	VSS	P3		
	VSS	P14		
	VSS	R2		
	VSS	R15		

2.2.5 Thermal Resistance

Table 2-4 Thermal Resistance Data

θJA(℃/W) (Flow: 0m/s)	θJB (℃/W)	θJC (℃/W)	θJA(℃/W) (Flow: 1m/s)	θJA(℃/W) (Flow: 2m/s)
29.3	21.2	15.3	26.8	25.4

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