Logos2 Family FPGAs Device Datasheet

(DS04001, V2.1)

(13.07.2023)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V2.1	13.07.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
CLM	Configurable Logic Module
DRM	Dedicated RAM Module
APM	Arithmetic Process Module
DDR	Double Data Rate
ADC	Analog to Digital Converter
HSSTLP	High Speed Serial Transceiver Low Performance
CTC	Clock Tolerance Compensation
I_{DK}	I drain-knee
PCIe	Peripheral Component Interconnect Express
UID	Unique Identification
HSTL	High Speed Transceiver Logic
SSTL	Stub Series Terminated Logic
LVDS	Low-Voltage Differential Signaling
TMDS	Transition-minimized differential signaling
HDMI	High Definition Multimedia Interface
DVI	Digital Visual Interface
UI	Unit Interval
HR	High Range

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This document mainly includes an overview of the features, product model and resource scale list, AC and DC characteristics of the Logos2 Family FPGAs devices from Shenzhen Pango Microsystems Co., Ltd.. It enables users to understand the features of the Logos2 Family FPGAs devices, facilitating device selection.

Chapter 1 Overview

Logos2 Family programmable logic devices are manufactured using mainstream 28nm process technology, featuring high cost-effectiveness and low power consumption. The Logos2 Family FPGAs include Configurable Logic Modules (CLM), dedicated 36Kb storage unit (DRM), Arithmetic Processing Units (APM), multi function high-performance I/Os, extensive on-chip clock resources and other modules. It also integrates hard core resources such as Analog-to-Digital Converter (ADC) Module, supports various configuration modes, and security functions like Bitstream Encryption Authentication and Device ID (UID). Based on the above features, the Logos2 Family FPGAs are widely applicable to various areas such as video, industrial control, automotive electronics, communications, computers, medical treatment, LED display, security monitoring, instrumentation, and consumer and so on.

1.1 Features of Logos2 Family FPGAs

- **High Cost-Efficient, Low Power Consumption**
  - Mature 28nm CMOS process
  - Core voltage down to 1.0V[1]
- **Flexible IO, Supports Multiple Standards**
  - Up to 500 user I/Os, supporting 1.2V to 3.3V I/O standards
  - Supports HSTL, SSTL memory interface standards
  - Supports LVDS, MINI-LVDS and other differential standards
  - Programmable IO BUFFER, high-performance IO LOGIC
  - Grade 2 hot-swapping
- **Flexible Programmable Logic Module CLM**
  - LUT6 logic architecture
  - Each CLM contains 4 multi-functional LUT6s and 8 registers
  - Supports fast arithmetic carry logic
  - Supports distributed RAM
  - Supports cascade chains
- **DRM Supports Multiple Read/Write Modes**
  - A single DRM provides 36Kb of memory space, configurable as 2 independent 18Kb storage blocks

- Supports various working modes, including single-port (SP) RAM, dual-port (DP) RAM, simple dual-port (SDP) RAM, ROM, and FIFO mode
- Dual-port RAM and simple dual-port RAM support mixed data bit width for both ports
- Supports ECC
- Supports three write modes: Normal-Write, Transparent-Write, and Read-before-Write
- Supports Byte Write function
- Optional address latch, output registers

➢ **Efficient Arithmetic Processing Unit (APM)**

- Each APM supports one 25*18 operation or two 12*9 operations
- Supports Input Register and Output Register
- Supports 48-bit addition
- Supports signed data operations

➢ **Integrated ADC Hard Core**

- 12bit resolution, 1MSPS sampling rate
- Up to 17 input channels
- Integrated temperature sensors (Grade -5 does not support)

➢ **Extensive Clock Resources**

- Supports 3 types of clock networks: GLOBAL CLOCK, REGIONAL CLOCK, I/O CLOCK
- Integrates multiple PLLs, each PLL supports up to 5 clock outputs

➢ **Flexible Configuration Methods**

- Supports multiple programming modes
- JTAG mode, compliant with IEEE 1149.1 and IEEE 1149.6 standards
- Master SPI Mode Supports up to 8bit data width
- Supports Slave Serial and Slave Parallel modes.
- Supports AES256-GCM bitstream encryption, supports 96bit UID protection
- Supports digital signature verification of bitstream files
- Supports eFuse key storage
- Supports battery-backed RAM (BB-RAM) key storage and provides chip-level security protection
- Supports disabling bitstream readback
- Supports JTAG security management
- Supports protection against DPA attacks
- Supports SEU error detection and correction
- Supports multi-version bitstream fallback function
- Supports watchdog timeout detection
- Supports Fabric Configuration tool
- Supports the in-circuit Logic Analyzer: Fabric Debugger

- **High-speed Serial Transceiver**

  HSSTLP

  - Data Rate up to 6.6Gbps per Lane
  - Flexible PCS, supports protocols such as PCIe GEN1/GEN2, Gigabit Ethernet, XAUI, Gige, etc.

Notes: 1. The DR version supports VCC 0.9V

1.2 Logos2 Family FPGA Resource Scale and Packaging Information

The resource scale and packaging information of the Logos2 Family FPGA are as shown in Table 1-1 and Table 1-2.

Table 1-1 Logos2 FPGA Resource Count

Resource Name		**PG2L25H**	**PG2L50H**	**PG2L100H(X)**	**PG2L200H**
CLM	LUT6	17800	35800	66600	159800
	Equivalent LUT4	26700	53700	99900	239700
	FF	35600	71600	133200	319600
	Distributed RAM (Kb)	343.75	593.75	1243.75	2468.75
DRM (36Kbits per unit)		55	85	155	415
APM (units)		80	120	240	740
PLLs	GPLLs	3	5	6	10
	PPLLs	3	5	6	10
ADC (dual core)	Dedicated analogue channels (differential input pairs)	1	1	1	1
	Multiplexed analogue channels (differential input pairs)	11	16	16	16
SERDES LANE[1]		4	4	8	16
PCIE GEN2 ×4 CORE		1	1	1	1

Notes: 1. 4 LANEs form one HSSTLP

Table 1-2 Logos2 FPGA Package Information and User IO Count

Device / **Packaging Information**	**PG2L25H**		**PG2L50H**		**PG2L100H(X)**		**PG2L200H**	
	SERDES LANE	**I/O**	**SERDES LANE**	**I/O**	**SERDES LANE**	**I/O**	**SERDES LANE**	**I/O**
FBG676 (27mm ×27mm, 1.0mm)					8	300		
FBG484 (23mm ×23mm, 1.0mm)			4	250	4	285		
MBG325 (15mm ×15mm, 0.8mm)	4	150						
MBG324 (15mm ×15mm, 0.8mm)			0	210	0	210		
FBB484 (23mm ×23mm, 1.0mm)							4	285
FBB676 (27mm ×27mm, 1.0mm)							8	400
FFBG1156 (35mm ×35mm, 1.0mm)							16	500

1.3 Brief Description of Logos2 Family FPGAs

1.3.1 CLM

CLM (Configurable Logic Module) is the basic logic unit of Logos2 family products, mainly composed of multifunctional LUT6s, registers, and multiplexers. CLMs in Logos2 Family products come in two forms: CLMA and CLMS. Both CLMA and CLMS support logic, arithmetic, shift registers, and ROM functions, but only CLMS supports distributed RAM function. Key features of CLM are as follows:

- Featuring an innovative LUT6 logic architecture
- Each CLM contains 4 multifunctional LUT6s
- Each CLM contains 8 registers
- Arithmetic functional mode supported
- Supports fast arithmetic carry logic
- Supports multiplexer functions
- Supports ROM functions
- Supports distributed RAM mode
- Supports cascade chains

For detailed CLM features and usage, please refer to ***"UG040001_Logos2 Family FPGAs Configurable Logic Module (CLM) User Guide"***.

1.3.2 DRM

A single DRM provides 36Kb of memory space, supports various working modes and configurable bit widths, and supports dual-port mixed bit widths in DP RAM and SDP RAM modes. The main features of DRM are as follows:

- The DRM storage capacity can be independently configured as 2 x 18K or 1 x 36K.
- The data width of DP RAM goes up to 36bits, with its two ports being completely independent apart from sharing RAM content, and supporting different clock domains.
- The data width of SDPRAM goes up to 72bits, with its two ports also supporting different clock domains, but one port is limited to write operations and the other is limited to read operations.
- In ROM mode, the content of the DRM is typically initialized during the process of downloading configuration data. The same process applies in other modes. The data width of the ROM can be up to 72bits.

- In synchronous or asynchronous FIFO mode, one port is dedicated to data writing and the other port to data reading, with read and write ports using different clocks.
- Supports ECC when used as 64-bit 36K memory, allowing users-inserted errors.

For detailed DRM features and usage, please refer to the ***"UG040002_Logos2 Family FPGAs Dedicated RAM Module (DRM) User Guide"***.

1.3.3 APM

APM consists of I/O Unit, Preadder, Mult, and Postadder functional units, with each unit support register output. Each APM can implement one 25*18 multiplier or two 12*9 multipliers, supporting pre-addition functions; it supports signed data operations and one 48-bit or two 24-bit addition/subtraction/accumulation operations. The APMs of Logos2 FPGA support cascading, enabling applications such as filters and high-bit-width multipliers. The main features of APM are as follows:

- Signed multiplier 25*18; unsigned multiplication achieved by setting the highest bit to 0
- All calculations and output results are signed, including the sign bit
- One 48-bit addition/subtraction/accumulation operation or two 24-bit operations supported
- With Pre-add as 25 bits
- Independent optional CE and RST
- Input cascade chains supported
- Output cascade chains supported
- Control/data signal pipeline
- Dynamic mode switching supported
- Rounding function supported

For detailed APM features and usage, please refer to the "***UG040003_Logos2 Family FPGAs Arithmetic Processing Module (APM) User Guide***".

1.3.4 Input/Output

IOB

The IOs of Logos2 FPGA are organized by Bank, with each Bank powered by an independent IO power supply. IOs are flexibly configurable, supporting 1.2V to 3.3V power supply voltages and various single-ended and differential interface standards, to accommodate different applications. All user IOs are bidirectional, containing IBUF, OBUF, and tri-state control TBUF. IOB of Logos2 FPGA has flexible configuration options for interface standards, Output Drive, Slew Rate, Input

Hysteresis, etc. For detailed IO features and usage, please refer to the "***UG040006_Logos2 Family FPGAs Input/Output Interface (IO) User Guide***".

IOL

The IOL module is located between the IOB and the core, managing signals to be input to and output from the FPGA Core.

IOL supports various high-speed interfaces application, in addition to supporting direct data input/output and IO register input/output modes, it also supports the following features:

- ISERDES: For high-speed interfaces application, it supports the input Deserializers of 1:2; 1:4; 1:7; 1:8 etc..
- OSERDES: For high-speed interfaces application, it supports the output Serializers of 2:1; 4:1; 7:1; 8:1 etc..
- Built-in IO delay function, which can dynamically/statically adjust input/output delay.

Built-in input FIFO, mainly used for clock domain conversion from external non-continuous DQS (for DDR memory interface) to internal continuous clock and compensating for the phase difference between the sampling clock and internal clock in some special Generic DDR applications.

For detailed IO features and usage, please refer to "***UG040006_Logos2 Family FPGAs Input/Output Interface (IO) User Guide***".

1.3.5 ADC

Each Logos2 FPGA incorporates a Analog-to-digital converter (ADC) with 12-bit resolution and 1MSPS sampling rate. Each ADC has 17 pairs of differential input channels, 16 pairs of which are Analog Inputs multiplexed with GPIO, and the remaining one uses dedicated analog input pins. The scanning mode of the 17 pairs of differential channels is fully controlled by the FPGA, and users can determine the number of channel pairs that share the 1MSPS ADC sampling rate by User Logic. The ADC provides monitoring functions for on-chip voltage and temperature. It can detect VCC, VCCA, and VCC_DRM; For detailed characteristics parameters, refer to Table 6-1. The specific use of the ADC is detailed in the "***UG040009_Logos2 Family FPGA Analog-to-Digital Converter (ADC) User Guide***".

1.3.6 Clock

The Logos2 Family products includes three types of clocks: Global Clock, Region Clock, and I/O Clock. Global Clock provides the clock for synchronous logic units of the chip. Global Clock can serve as a synchronous clock for synchronous logic units in different clock regions. Region Clock

provides the clock for synchronous logic units in the single clock region it belongs to. It can drive the logical units in two adjacent clock regions in the vertical direction through a dedicated driver. I/O Clock provides the synchronous clock for high-speed I/O data.

To meet requirements of users for frequency changes and phase adjustments, the Logos2 Family products also offer abundant PLL resources. GPLL provides more functions compared to PPLL while PPLL can provide clocks for DDR and other applications.

The clock resources for the PG2L100H are as follows:

- The chip has 32 GLOBAL CLOCKs, with 16 in either upper and lower sides of the chip.
- The chip has 96 HORIZONTAL CLOCKs, with 12 in each REGION.

For detailed features and usage of the clocks, please refer to "***UG040004_Logos2 Family FPGAs Clock Resources (Clock) User Guide***".

1.3.7 Configuration

Configuration is the process of programming the FPGA. Logos2 FPGA uses SRAM cells to store configuration data, which must be reconfigured after every power up; the configuration data can be actively obtained by the chip from external flash or downloaded into the chip via an external processor or controller.

Logos2 FPGA supports multiple configuration modes, including JTAG mode, Master SPI mode, Slave Parallel mode, and Slave Serial mode. The configuration-related features of Logos2 FPGA are as follows:

- JTAG mode, compliant with IEEE 1149.1 and IEEE 1149.6 standards
- Master SPI mode, supporting 1/2/4/8-bit data width
- Slave Parallel mode, supporting 8/16/32-bit data width
- Slave Serial mode
- Supports configuration data compression, effectively reducing the size of the bitstream, saving memory space and programming time
- Configuration data encryption, which protects customers' design intellectual property against malicious copying
- Supports SHA-3 summary, RSA-2048 authentication, and AES256-GCM self-authentication for bitstream digital signature
- Supports eFuse and battery-powered RAM (BB-RAM) key storage, with BB-RAM providing chip-level security protection
- Security protection technology, which prevents bitstream reverse reading
- Supports JTAG security management and can disable JTAG function permanently

- Protection against DPA attacks, which prevents encrypted keys from being hacked
- Supports SEU 1-bit correction and 2-bit detection.
- Supports watchdog timeout detection function
- Supports configuration bitstream version fallback feature in Master SPI mode
- Supports UID function

For detailed features and usage of configuration, please refer to "***UG040005_Logos2 Family FPGAs Configuration User Guide***".

1.3.8 High-Speed Serial Transceiver HSSTLP

HSSTLP is a high-speed serial interface for the Logos2 Family products. HSSTLP consists of high-performance PMA and highly flexible PCS, which can be flexibly applied to various serial protocol standards. Each HSSTLP supports 1 to 4 full-duplex transmit and receive LANEs. The key features of HSSTLP include:

- Range of Data Rate: 0.6Gbps-6.6Gbps
- Flexible reference clock selection
- Transmit and receive channel data rates can be independently configured
- Programmable output swing and de-emphasis
- Adaptive equalizer at receiver side
- PMA Rx supports SSC
- The data channels support 8bit only, 10bit only, 8b10b, 16bit only, 20bit only, 32bit only, 40bit only, and 64b66b/64b67b modes
- The PCS is flexibly configurable and supports protocols such as PCI Express GEN1, PCI Express GEN2, XAUI, Gigabit Ethernet, CPRI, SRIO, etc.
- Flexible Word Alignment functions
- Supports RxClock Slip function to ensure a fixed Receive Latency
- Supports 8b10b encoding/decoding
- Supports 64B/66B and 64B/67B
- Flexible CTC scheme
- Supports x2 and x4 Channel Bonding
- Supports dynamically configurate HSSTLP
- Near-end loopback and far-end loopback
- Built-in PRBS Generator and Checker

For detailed features and usage of HSSTLP, please refer to the "***UG040008_Logos2 Family FPGA High-Speed Serial Transceiver (HSSTLP) User Guide***"

1.4 Logos2 Family FPGAs Reference Materials

Section 1.3 provides a brief description of the various Logos2 FPGA modules, as well as the clock and configuration system. For detailed information on the respective modules, please refer to the user guide documents related to Logos2 FPGA, as shown in the table below.

Table 1-3 Logos2 Family FPGAs User Guide Documents

Document Number	Document Name	Content of the Document
UG040001	Logos2 Family FPGAs Configurable Logic Module (CLM) User Guide	Functional description of Logos2 Family FPGAs Configurable Logic Module
UG040002	Logos2 Family FPGAs Dedicated RAM Module (DRM) User Guide	Functional description of Logos2 Family FPGAs Dedicated RAM Module
UG040003	Logos2 Family FPGAs Arithmetic Processing Module (APM) User Guide	Functional description of Logos2 Family FPGAs Arithmetic Processing Module
UG040004	Logos2 Family FPGAs Clock Resources (Clock) User Guide	Logos2 Family FPGAs Clock Resources, including the function and usage of PLL
UG040005	Logos2 Family FPGAs Configuration User Guide	Description of the configuration interface, configuration modes, and configuration process in Logos2 Family FPGA
UG040006	Logos2 Family FPGAs Input/Output Interface (IO) User Guide	Functional description of Logos2 Family FPGAs Input/Output Interface
UG040007	Logos2 Family Product GTP User Guide	Functional Description and user guide for Logos2 Family FPGAs GTPs
UG040008	Logos2 Family FPGAs High-Speed Serial Transceiver (HSSTLP) User Guide	Functional Description of Logos2 Family FPGAs High-Speed Serial Transceiver (HSSTLP)
UG040009	Logos2 Family FPGAs Analog-to-Digital Converter (ADC) Module User Guide	Functional description of Logos Family FPGAs Analog-to-Digital Converter
UG040012	Logos2 Family Hardware Design Guide	Logos2 Family FPGAs Hardware Design Guide

1.5 Logos2 Family FPGAs Ordering Information

Content and meaning of Logos2 Family FPGAs product model numbers are shown in Figure 1-1.

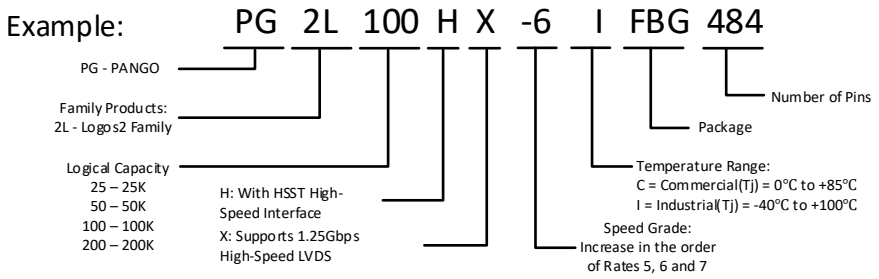

Figure 1-1 Content and Meaning of Logos2 Family FPGAs Product Model Numbers

Chapter 2 Operating Conditions

2.1 Absolute Voltage Limits of the Device

Table 2-1 Absolute Maximum Voltage of the Device

Item	Min.	Max.	Unit	Description
V_{REF}	-0.5	2.0	V	Input reference voltage
V_{CCB}	-0.5	2.0	V	Backup battery power voltage for key memory
V_{CC}	-0.5	1.1	V	Core logic power supply voltage
V_{CCA}	-0.5	2.0	V	Auxiliary power supply voltage
V_{CCIO}	-0.5	3.6	V	Output driver power supply voltage
V_{CC_DRM}	-0.5	1.1	V	DRM power supply voltage
V_{IN} [1]	-0.3	V_{CCIO}+0.45	V	I/O input voltage
	-0.3	2.525	V	When V_{CCIO} is 3.3V, it is the V_{REF} or the I/O input voltage of differential I/O standard
V_{CCADC}	-0.5	2.0	V	ADC power supply voltage
T_{STG}	-65	150	℃	Storage ambient temperature
T_{SOL} [2]		260	℃	Maximum soldering temperature
T_j		125	℃	Maximum junction temperature

Notes:

1. The maximum value of **V_{IN}** is applicable to DC signals. For allowed AC Maximum Overshoot and Undershoot Voltage, refer to Table 2-4;
2. For relevant descriptions of device soldering, refer to the device package guide;
3. Exceeding the above maximum ratings may cause permanent damage to the device. Operating within the rating limits will not damage the device, but does not guarantee normal operation at these limits. Long-term operation of the device at the limits will drastically impact its reliability.

2.2 Recommended Operating Conditions for the Device

Table 2-2 Recommended Device Operating Conditions

Item	Min.	Typ.	Max.	Unit	Description
V_{CCB}	1.0	--	1.89	V	Backup battery power voltage for key memory
V_{CC}	0.95	1.0	1.05	V	Core Power Supply Voltage
V_{CCA}	1.71	1.8	1.89	V	Auxiliary power supply voltage
V_{CCIO}	1.14	--	3.465	V	Output driver power supply voltage
V_{CC_DRM}	0.95	1.0	1.05	V	DRM power supply voltage
V_{IN}	-0.2	--	VCCIO+0.2	V	I/O input voltage
	-0.2	--	2.5	V	When VCCIO is 3.3V, it is the VREF or the I/O input voltage of differential

Item	Min.	Typ.	Max.	Unit	Description
					I/O standard
I_{IN}	--	--	10	mA	The maximum current allowed to flow through the forward-biased clamp diode of any pin in a powered-up or powered-down Bank
T_j	0		85	℃	Operating junction temperature of commercial devices
	-40		100	℃	Operating junction temperature of industrial devices

Notes: The V_{CCIO} voltage should be within a range of ±5% of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V.

2.3 DC Characteristics of the Device Under Recommended Operating Conditions

Table 2-3 DC Characteristics of the Device Under Recommended Operating Conditions

Identification	Min.	Typ.	Max.	Description
V_{DRVCC}	0.75V	--	--	Configuration data retention voltage of V_{CC}
V_{DRVCCA}	1.5V	--	--	Configuration data retention voltage of V_{CCA}
I_L	--	--	60uA	Leakage current of input or output pins
I_{REF}	--	--	60uA	Leakage current of the V_{REF} pin
I_{PU}	90uA	--	390uA	sPAD pull-up current (V_{IN}=0; V_{CCIO}=3.3V)
	68uA	--	370uA	PAD pull-up current (V_{IN}=0; V_{CCIO}=2.5V)
	34uA	--	300uA	PAD pull-up current (V_{IN}=0; V_{CCIO}=1.8V)
	23uA	--	190uA	PAD pull-up current (V_{IN}=0; V_{CCIO}=1.5V)
	12uA	--	150uA	PAD pull-up current (V_{IN}=0; V_{CCIO}=1.2V)
I_{PD}	50uA	--	350uA	PAD pull-down current (V_{IN}=3.3V)
	45uA	--	180uA	PAD pull-down current (V_{IN}=1.8V)
I_{CCADC}	--	--	25mA	Power-up state of the analogue circuit, current of the ADC analogue power supply
I_{VCCB}	--	--	150nA	Power current of V_{CCB}
R_{INTERM}	28Ω	40Ω	55Ω	The Thevenin equivalent resistance of the programmable input terminal at V_{CCIO}/2 voltage. (When set to 40Ω)
	35Ω	50Ω	65Ω	The Thevenin equivalent resistance of the programmable input terminal at V_{CCIO}/2 voltage. (When set to 50Ω)
	44Ω	60Ω	83Ω	The Thevenin equivalent resistance of the programmable input terminal at V_{CCIO}/2 voltage. (When set to 60Ω)
C_{IN}	--	--	TBD	Input capacitance at the PAD end of bare die
n	--	0.9988	--	Ideal factor of temperature diode
r	--	2.5Ω	--	Serial resistance of temperature diodes

Notes: Typical values refer to measurements at normal pressure and 25 ℃ junction temperature; maximum values refer to measurements at normal pressure and 100 ℃ junction temperature

2.4 Allowed Maximum Overshoot and Undershoot Voltage for VIN

Table 2-4 Allowed Maximum Overshoot and Undershoot Voltage for VIN

Overshoot Voltage (V)	%UI (-40℃~125℃)	Undershoot Voltage (V)	%UI (-40℃~125℃)
VCCIO + 0.45	100	-0.3	100
		-0.35	55.5
		-0.4	23.2
		-0.45	9.9
VCCIO + 0.5	42	-0.5	4.3
VCCIO + 0.55	19.08	-0.55	1.89
VCCIO + 0.6	8.77	-0.60	0.84
VCCIO + 0.65	4.1	-0.65	0.387
VCCIO + 0.7	1.9	-0.7	0.18
VCCIO + 0.75	0.918	-0.75	0.08
VCCIO + 0.80	0.44	-0.8	0.04
VCCIO + 0.85	0.21	-0.85	0.017

Notes:

1. The peak voltage of overshoot or undershoot, and the duration above VCCIO+0.20V or below GND-0.20V, should not exceed the values in this table
2. UI duration is less than 15us

2.5 Typical Quiescent Current

Table 2-5 Typical Quiescent Current

Identification	Device	Typ.	Unit	Description
I_{CCQ}	PG2L25H	150	mA	Quiescent Current of V_{CC}
	PG2L50H	275		
	PG2L100H(X)	500		
	PG2L200H	1065		
I_{CC_DRMQ}	PG2L25H	3.5	mA	Quiescent Current of V_{CC_DRM}
	PG2L50H	6.5		
	PG2L100H(X)	11		
	PG2L200H	30		
I_{CCIOQ}	PG2L25H	6.6	mA	Quiescent Current of V_{CCIO}
	PG2L50H	6.6		
	PG2L100H(X)	18		
	PG2L200H	30		
I_{CCAQ}	PG2L25H	30	mA	Quiescent Current of V_{CCA}
	PG2L50H	55		
	PG2L100H(X)	120		
	PG2L200H	380		

Notes:

1. Typical values refer to measurements at normal pressure and 85℃ junction temperature, and all single-ended I/Os; devices with blank configuration have no output current load or input pull-up resistor, and all I/Os are in tri-state and floating
2. For static power estimation under other specific conditions, use the power Evaluation Kit integrated into the PDS.

2.6 Power-up/Power-down Requirements

2.6.1 Power-up/Power-down Sequences

- During power-up and power-down, the duration where (VCCIO-VCCA) > 2V must be less than 100 milliseconds.
- Recommended power-up sequence: VCC, VCC_DRM, VCCA, VCCIO, as shown in Figure 2-1. Before reaching the typical voltage values, the following must be met: VCC ≥ VCC_DRM ≥ VCCA ≥ VCCIO, and at this time, the power-up current is minimum.
- The recommended power-down sequence is the reverse of the recommended power-up sequence, as shown in Figure 2-2. Before reaching zero voltage, the following must be met: VCCIO ≤ VCCA ≤ VCC_DRM ≤ VCC.

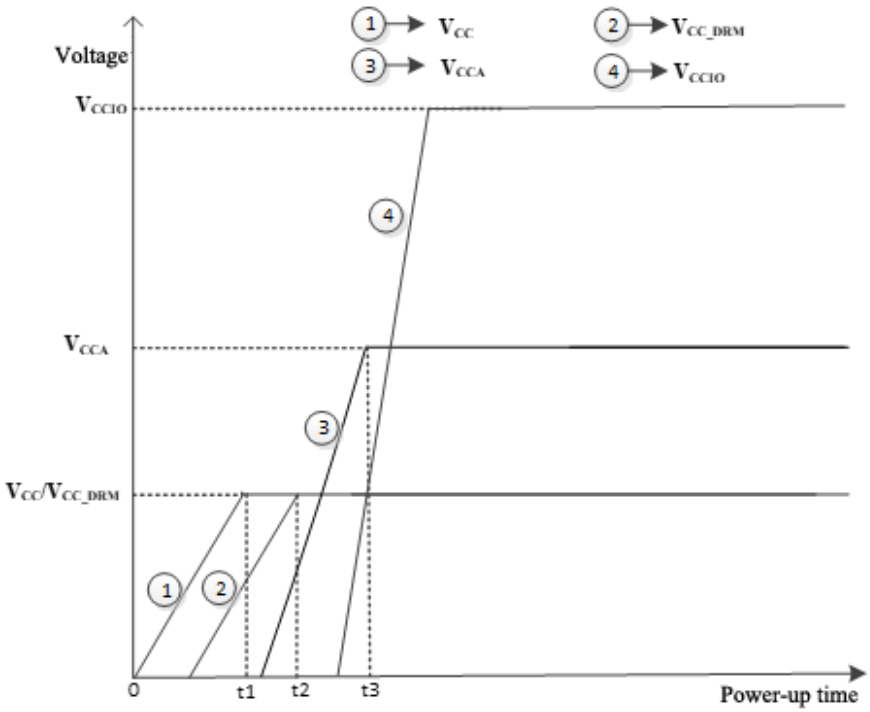

Figure 2-1 Power-up Timing Diagram

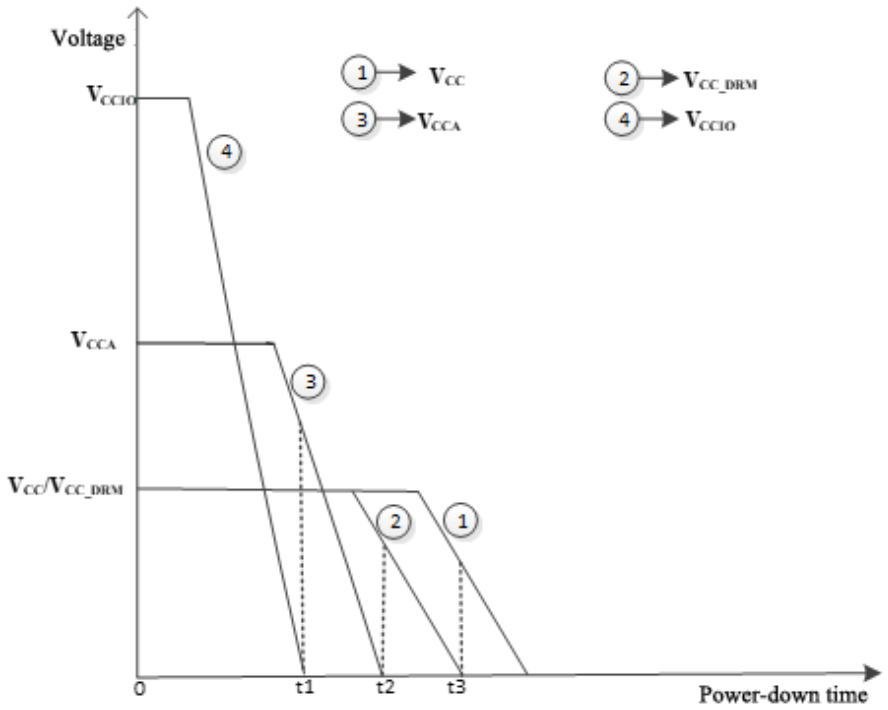

Figure 2-2 Power-down Timing Diagram

2.6.2 Power-up Ramp Time

Table 2-6 Power-up Ramp Time

Identification	Min.	Max.	Unit	Description
TVCC	0.2	50	ms	The time for VCC to rise from GND to 90% of VCC
TVCC_DRM	0.2	50	ms	The time for VCC_DRM to rise from GND to 90% of VCC_DRM
TVCCIO	0.2	50	ms	The time for VCCIO to rise from GND to 90% of VCCIO
TVCCA	0.2	50	ms	The time for VCCA to rise from GND to 90% of VCCA
TVCCIO2VCCA	-	100	ms	The time where VCCIO - VCCA > 2V

2.6.3 Minimum Current Required for Start-up

Table 2-7 Minimum Current Required for Start-up

Identification	Max.	Unit	Description
I_{CCMIN}	I_{CCQ}+150	mA	Minimum current for V_{CC} power-up and start-up
I_{CC_DRMMIN}	I_{CC_DRMQ}+70	mA	Minimum current for V_{CC_DRM} power-up and start-up
$I_{CCIOMIN}$	I_{CCIOQ}+50	mA	Minimum current for V_{CCIO} power-up and start-up (per bank)
I_{CCAMIN}	I_{CCAQ}+40	mA	Minimum current for V_{CCA} power-up and start-up

2.7 Hot-Swap

2.7.1 Hot-Swap Specification

For the hot plug leakage current specification for the device, please refer to Table 2-8.

Table 2-8 Hot Plug Leakage Current Specifications

Parameter Symbol	Paramater Description	Max.
I_{DK} (DC)[1]	DC Current, per I/O	1mA
I_{DK} (AC)[2]	AC Current, per I/O	1mA

Notes:

1. When the chip is not powered-up, DC Current apply voltage to the hot plug I/O and test the maximum current sinking into the chip from the I/O.
2. AC current is the maximum current sinking into the chip from the I/O during the recommended power-up and power-down sequence.
3. Dedicated configuration I/O does not support hot plug; configurable multiplexed I/Os and ADC multiplexed I/Os can meet the specification of IDK (DC) current but not that of IDK (AC) current. Other user I/Os meet the IDK current specification under the recommended power-up and power-down sequence; if the sequence is not followed, the maximum IDK (AC) current is 15mA.

2.7.2 Hot-Swap Application Restrictions

To fulfil hot-swapping requirement, the following conditions must be met:

1. Power-up/Power-down must be performed according to the chip's recommended sequence.
2. To ensure application requirements are met, the user must choose appropriate external circuitry (such as pull-up/pull-down resistors and series resistors) etc.

2.8 ESD (HBM, CDM), Latch-Up Specifications

Table 2-9 ESD, Latch-Up Specifications

Identification	Value	Unit	Description
HBM_IO	±1000	V	Human Body Model (HBM)
HBM_SERDES	±1000	V	HBM, Serdes
CDM_IO	±350	V	Charge Device Model (CDM), general IOs
CDM_SERDES	±300	V	CDM, Serdes, Logos2 100K and below devices
	±250	V	CDM, Serdes, Logos2 100K above devices
Latch-up	±100	mA	Current injection method

2.9 Efuse Programming Conditions

Table 2-10 Efuse Programming Conditions

Identification	Min.	Max.	Unit	Description

I_{eFUSE}		188	mA	Current provided by V_{CCA}
T_j	15	125	℃	

Chapter 3 DC Characteristics Under Typical Operating Conditions

3.1 I/O Input & Output DC Characteristics

The input and output voltage range of each single-ended IO level standard is shown in the table below

Table 3-1 Input and Output Voltage Range of Single-Ended IO Level Standard

Standard	VIL		VIH		V_{OL} Max (v)	VOH Min (v)	I_{OL} (mA)	I_{OH} (mA)
	Min(v)	Max(v)	Min(v)	Max(v)				
PCI33	-0.3	0.3VCCIO	0. 5VCCIO	VCCIO+0.5	0.1VCCIO	0.9VCCIO	1.5	-0.5
LVCMOS33	-0.3	0.8	2.0	3.465	0.4	VCCIO-0.4	4 8 12 16	-4 -8 -12 -16
LVTTL33	-0.3	0.8	2.0	3.465	0.4	2.4	4 8 12 16 24	-4 -8 -12 -16 -24
LVCMOS25	-0.3	0.7	1.7	VCCIO+0.3	0.4	VCCIO-0.4	4 8 12 16	-4 -8 -12 -16
LVCMOS18	-0.3	0.35VCCIO	0.65VCCIO	VCCIO+0.3	0.4	VCCIO-0.4	4 8 12 16 24	-4 -8 -12 -16 -24
LVCMOS15	-0.3	0.35VCCIO	0.65VCCIO	VCCIO+0.3	0.4	VCCIO-0.4	4 8 12 16	-4 -8 12 16
LVCMOS12	-0.3	0.35VCCIO	0.65VCCIO	VCCIO+0.3	0.4	VCCIO-0.4	4 8 12	-4 -8 -12
SSTL18_I	-0.3	Vref-0.125	Vref+0.125	VCCIO+0.3	0.5VCCIO-0.47	0.5VCCIO+0.47	8	-8
SSTL18_II	-0.3	Vref-0.125	Vref+0.125	VCCIO+0.3	0.5VCCIO-0.6	0.5VCCIO+0.6	13.4	-13.4
SSTL15_I	-0.3	Vref-0.10	Vref+0.10	VCCIO+0.3	0.5VCCIO-0.175	0.5VCCIO+0.175	8.9	-8.9
SSTL15_II	-0.3	Vref-0.10	Vref+0.10	VCCIO+0.3	0.5VCCIO-0.175	0.5VCCIO+0.175	13	-13
HSUL12	-0.3	Vref-0.13	Vref+0.13	VCCIO+0.3	0.2VCCIO	0.8VCCIO	0.1	-0.1
HSTL18_I	-0.3	Vref-0.1	Vref+0.1	VCCIO+0.3	0.40	VCCIO-0.40	8	-8
HSTL18_II	-0.3	Vref-0.1	Vref+0.1	VCCIO+0.3	0.40	VCCIO-0.40	16	-16
HSTL15_I	-0.3	Vref-0.1	Vref+0.1	VCCIO+0.3	0.40	VCCIO-0.40	8	-8
HSTL15_II	-0.3	Vref-0.1	Vref+0.1	VCCIO+0.3	0.40	VCCIO-0.40	16	-16
SSTL135_I	-0.3	Vref-0.1	Vref+0.1	VCCIO+0.3	0.5VCCIO-0.15	0.5VCCIO+0.15	8.9	-8.9
SSTL135_II	-0.3	Vref-0.1	Vref+0.1	VCCIO+0.3	0.5VCCIO-0.15	0.5VCCIO+0.15	13	-13
LPDDR	-0.3	0.2VCCIO	0.8VCCIO	VCCIO+0.3	0.1VCCIO	0.9VCCIO	0.1	-0.1

The input and output voltage ranges of the differential IO level standards are shown in Table 3-2

Table 3-2 Parameter Requirements for Differential Input/Output Standard

I/O Standard	Vicm(V)			Vid(V)			Vocm(V)			Vod(V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
LVDS	1	1.2	1.425	0.1	0.35	0.6	1	1.25	1.425	0.25	0.35	0.6
BLVDS	0.3	1.2	1.425	0.1	–	–	–	1.25	–	–		
MINI_LVDS	0.3	1.2	VCCA	0.2	0.4	0.6	1	1.2	1.4	0.3	0.40	0.6
PPDS	0.2	0.9	VCCA	0.1	0.25	0.4	0.5	1.0	1.4	0.1	0.3	0.45
RSDS	0.3	0.9	1.5	0.1	0.35	0.6	1	1.2	1.4	0.1	0.35	0.6
TMDS	2.7	2.965	3.23	0.15	0.675	1.2	VCCIO-0.405	VCCIO-0.3	VCCIO-0.19	0.4	0.6	0.8

Table 3-3 Parameter Requirements for Pseudo-differential Input/Output Standard

IO Standard	Vid(V)	Vicm (V)			Vol(V)	Voh(V)	IOL (mA)	IOH (mA)
	min	min	typ	max	max	min	max	min
HSUL12D	0.1	0.3	0.6	0.85	0.2VCCIO	0.8VCCIO	0.1	-0.1
SSTL135D_I	0.1	0.3	0.675	1	0.5VCCIO-0.15	0.5VCCIO+0.15	8.9	-8.9
SSTL135D_II	0.1	0.3	0.675	1	0.5VCCIO-0.15	0.5VCCIO+0.15	13	-13
HSTL15D_I	0.1	0.3	0.75	1.125	0.4	VCCIO-0.4	8	-8
HSTL15D_II	0.1	0.3	0.75	1.125	0.4	VCCIO-0.4	16	-16
HSTL18D_I	0.1	0.3	0.9	1.425	0.4	VCCIO-0.4	8	-8
HSTL18D_II	0.1	0.3	0.9	1.425	0.4	VCCIO-0.4	16	-16
LPDDRD	0.1	0.3	0.9	1.425	0.1VCCIO	0.9VCCIO	0.1	-0.1
SSTL15D_I	0.1	0.3	0.75	1.125	0.5VCCIO-0.175	0.5VCCIO+0.175	0.89	-0.89
SSTL15D_II	0.1	0.3	0.75	1.125	0.5VCCIO-0.175	0.5VCCIO+0.175	13	-13
SSTL18D_I	0.1	0.3	0.9	1.425	0.5VCCIO-0.47	0.5VCCIO+0.47	8	-8
SSTL18D_II	0.1	0.3	0.9	1.425	0.5VCCIO-0.6	0.5VCCIO+0.6	13.4	-13.4

Chapter 4 AC Characteristics Under Typical Operating Conditions

This chapter primarily lists the AC characteristics of each logic unit of the Logos2 Family FPGA under typical operating conditions.

4.1 AC Characteristic Parameters of Configurable Logic Module (CLM)

Table 4-1 CLM Module AC Characteristics

Delay Time			**Unit**	**Parameter Description**
-5	**-6**	**-7**		
Logic Delay				
0.24	0.196	TBD	ns,max	LUT6 input Ax/Bx/Cx/Dx to Y0/Y1/Y2/Y3 delay
0.452	0.353	TBD	ns,max	LUT6 input Ax/Bx/Cx/Dx to CR0/CR1 delay (LUT7)
0.445	0.395	TBD	ns,max	Delay from LUT6 input Ax/Bx/Cx/Dx to CR2 to Y1(LUT8)
0.449	0.357	TBD	ns,max	LUT input Ax to CYA(CR0) delay
0.446	0.371	TBD	ns,max	LUT input Bx to CYB(CR1) delay
0.452	0.358	TBD	ns,max	LUT input Cx to CYC(CR2) delay
0.434	0.353	TBD	ns,max	LUT input Dx to CYD(CR3) delay
0.105	0.065	TBD	ns,max	CIN input to COUT delay
Timing Parameter				
0.227	0.198	TBD	ns,max	CLK input with respect to TCO of Q0/Q1/Q2/Q3
0.27	0.218	TBD	ns,max	CLK input with respect to TCO of CR0/CR1/CR2/CR3
0.288/-0.08	0.22/-0.16	TBD	ns,min	Ax/Bx/Cx/Dx with respect to DFF setup/hold
0.16/-0.1	0.12/0.04	TBD	ns,min	M with respect to DFF setup/hold
0.224/-0.07	0.13/-0.04	TBD	ns,min	CE with respect to DFF setup/hold
0.224/-0.07	0.11/-0.05	TBD	ns,min	RS with respect to DFF setup/hold
Distributed RAM Timing Parameters				
0.455	0.63	TBD	ns,max	CLK -> Y0/Y1/Y2/Y3 mem read delay
0.56	0.71	TBD	ns,max	CLK -> CR0/CR1/CR2/CR3 mem read delay
-0.26/0.28	0.145/0.083	TBD	ns,min	CLK -> WE timing check, setup/hold
0.24/-0.07	0.048/0.193	TBD	ns,min	CLK -> An address timing check, setup/hold
-0.26/0.28	0.048/0.193	TBD	ns,min	CLK -> AD/BD/CD/DD data timing check, setup/hold

Notes: The parameters in the table are only applicable to PG2L100H; for parameters of other devices in the Logos2 Family, please refer to the PDS timing report.

4.2 AC Characteristic Parameters of DRM (Dedicated RAM Module)

Table 4-2 AC Characteristic Parameters of DRM Module

Categories	**Value**	**Unit**	**Description of AC Characteristic**

	-5	-6	-7		Parameters
T_{co_18K}	1.75	1.529	TBD	ns,max	CLKA/CLKB->QA/QB (Output register not enabled, in 18K mode)
$T_{co\_18K\_reg}$	0.718	0.625	TBD	ns,max	CLKA/CLKB->QA/QB (Output register enabled, in 18K mode)
T_{co_36K}	1.758	1.529	TBD	ns,max	CLKA/CLKB->QA/QB (Output register not enabled, in 36K mode)
$T_{co\_36K\_reg}$	0.718	0.625	TBD	ns,max	CLKA/CLKB->QA/QB (Output register enabled, in 36K mode)
T_{co_ecc}	1.758	1.529	TBD	ns,max	CLKB->QA/QB (Output register not enabled, in ECC mode)
$T_{co\_ecc\_reg}$	0.718	0.625	TBD	ns,max	CLKB->QA/QB (Output register enabled, in ECC mode)
$T_{co\_ecc\_err}$	0.718	0.625	TBD	ns,max	CLKB->ECC_S/DBITERR (Output register enabled, in ECC mode)
$T_{co\_flag\_full}$	1.11	0.966	TBD	ns,max	CLKA->FULL(ALMOST_FULL) (18K/36K FIFO modes)
$T_{co\_flag\_empty}$	0.652	0.567	TBD	ns,max	CLKB->EMPTY(ALMOST_EMPTY) (18K/36K FIFO modes)
$T_{co\_ecc\_parity}$	0.407	0.354	TBD	ns,max	CLKA->ECC_PARITY (ECC encoding mode)
$T_{co\_ecc\_rdaddr}$	0.834	0.726	TBD	ns,max	CLKA->ECC_RDADDR (Output register not enabled, in ECC mode)
$T_{co\_ecc\_rdaddr\_reg}$	0.834	0.726	TBD	ns,max	CLKA->ECC_RDADDR (Output register enabled, in ECC mode)
$T_{su\_18K\_ad}$/ $T_{hd\_18K\_ad}$	-0.077/0.097	-0.067/0.085	TBD	ns,min	Address Input Setup/Hold Time (18K mode)
$T_{su\_18K\_d}$/ $T_{hd\_18K\_d}$	-0.002/0.043	-0.002/0.038	TBD	ns,min	Data Input Setup/Hold Time (18K mode)
$T_{su\_18K\_ce}$/ $T_{hd\_18K\_ce}$	0.034/0.029	0.03/0.026	TBD	ns,min	CE Input Setup/Hold Time (18K mode)
$T_{su\_18K\_we}$/ $T_{hd\_18K\_we}$	-0.065/0.086	-0.057/0.075	TBD	ns,min	WE Input Setup/Hold Time (18K mode)
$T_{su\_18K\_be}$/ $T_{hd\_18K\_be}$	-0.010/0.029	-0.009/0.026	TBD	ns,min	BE Input Setup/Hold Time (18K mode)
$T_{su\_18K\_oe}$/ $T_{hd\_18K\_oe}$	-0.060/0.080	-0.053/0.070	TBD	ns,min	OCE Input Setup/Hold Time (18K mode)
$T_{su\_18K\_rst}$/ $T_{hd\_18K\_rst}$	0.001/0.017	0.001/0.015	TBD	ns,min	Synchronous Reset Input Setup/Hold Time (18K mode)
$T_{su\_36K\_ad}$/ $T_{hd\_36K\_ad}$	-0.077/0.097	-0.067/0.085	TBD	ns,min	Address Input Setup/Hold Time (36K mode)
$T_{su\_36K\_d}$/ $T_{hd\_36K\_d}$	-0.002/0.043	-0.002/0.038	TBD	ns,min	Data Input Setup/Hold Time (36K mode)
$T_{su\_36K\_ce}$/ $T_{hd\_36K\_ce}$	0.034/-0.014	0.03/-0.013	TBD	ns,min	CE Input Setup/Hold Time (36K mode)
$T_{su\_36K\_we}$/ $T_{hd\_36K\_we}$	-0.033/0.054	-0.029/0.047	TBD	ns,min	WE Input Setup/Hold Time (36K mode)
$T_{su\_36K\_be}$/ $T_{hd\_36K\_be}$	-0.01/0.029	-0.009/0.026	TBD	ns,min	BWE Input Setup/Hold Time (36K mode)
$T_{su\_36K\_oe}$/ $T_{hd\_36K\_oe}$	-0.027/0.047	-0.024/0.041	TBD	ns,min	OCE Input Setup/Hold Time (36K mode)
$T_{su\_36K\_rst}$/	0.001/0.017	0.001/0.015	TBD	ns,min	Synchronous Reset Input Setup/Hold

Categories	Value			Unit	Description of AC Characteristic Parameters
	-5	-6	-7		
$T_{hd\_36K\_rst}$					Time (36K mode)
$T_{su\_ecc\_d}$/ $T_{hd\_ecc\_d}$	0.021/0.018	0.019/0.016	TBD	ns,min	Data Input Setup/Hold Time (ECC mode)
$T_{su\_fifo\_wctl}$/ $T_{hd\_fifo\_wctl}$	-0.065/0.086	-0.057/0.075	TBD	ns,min	WREN Input (Setup/Hold Time) (18K/36K FIFO modes)
$T_{su\_fifo\_rctl}$/ $T_{hd\_fifo\_rctl}$	0.03/-0.014	0.03/-0.013	TBD	ns,min	RDEN Input (Setup/Hold Time (18K/36K FIFO modes)
$T_{su\_ecc\_injerr}$/ $T_{hd\_ecc\_injerr}$	0.021/0.018	0.019/0.016	TBD	ns,min	INJECT_S/DBITERR input Setup/Hold time(ECC mode)
T_{mpw_norm}	1.104	0.960	TBD	ns,min	CLKA/CLKB MPW(NW/TW mode)
T_{mpw_rbw}	1.546	1.345	TBD	ns,min	CLKA/CLKB MPW(RBW mode)
T_{mpw_fifo}	1.104	0.960	TBD	ns,min	CLKA/CLKB MPW (FIFO mode)
T_{mpw_ecc}	1.104	0.960	TBD	ns,min	CLKA/CLKB MPW (ECC mode)

Notes: The parameters in the table are only applicable to PG2L100H; for parameters of other devices in the Logos2 Family, please refer to the PDS timing report.

4.3 AC Characteristic Parameters of APM (Arithmetic Process Module)

Table 4-3 APM Module AC Characteristics

Description of AC Characteristic Parameters	Pre-dder	Multiplier	Post-adder	Value			Unit
				-5	-6	-7	
Data/Control Pin to Input Register CLK Setup and Hold Time							
H→preadd unit register CLK setup/hold	Yes	NA	NA	1.376/-0.1	1.197/-0.141	TBD	ns
X→preadd unit register CLK setup/hold	Yes	NA	NA	1.58/-0.16	1.376/-0.147	TBD	ns
X→input unit register CLK setup/hold	NA	NA	NA	0.38/-0.02	0.336/-0.020	TBD	ns
Y→input unit register CLK setup/hold	NA	NA	NA	0.22/-0.03	0.196/-0.028	TBD	ns
H→input unit register CLK setup/hold	NA	NA	NA	0.28/-0.04	0.248/-0.042	TBD	ns
Z→input unit register CLK setup/hold	NA	NA	NA	0.16/0.01	0.146/0.010	TBD	ns
INCTRL→input unit register CLK setup/hold	NA	NA	NA	0.16/0	0.144/0.000	TBD	ns
MODEY→input unit register CLK setup/hold	NA	NA	NA	0.16/-0.009	0.147/-0.008	TBD	ns
MODEZ→input unit register CLK setup/hold	NA	NA	NA	0.25/-0.01	0.220/-0.014	TBD	ns
Data Pin to Pipeline Register CLK Setup and Hold Time							
Y→Multiplier unit register CLK setup/hold	NA	Yes	No	1.47/-0.25	1.281/-0.226	TBD	ns
X→Multiplier unit register CLK setup/hold	Yes	Yes	No	2.76/-0.38	2.402/-0.333	TBD	ns
X→Multiplier unit register CLK setup/hold	No	Yes	No	1.57/-0.26	1.373/-0.233	TBD	ns

Description of AC Characteristic Parameters	Pre-dder	Multiplier	Post-adder	Value			Unit
				-5	-6	-7	
H-> Multiplier unit register CLK setup/hold	Yes	Yes	No	2.55/-0.36	2.224/-0.316	TBD	ns
Data/Control Pin to Output Register CLK Setup and Hold Time							
Y→postadd unit register CLK setup/hold	NA	Yes	Yes	2.51/-0.512	2.190/-0.446	TBD	ns
X→postadd unit register CLK setup/hold	No	Yes	Yes	2.636/-0.52	2.293/-0.454	TBD	ns
X→postadd unit register CLK setup/hold	Yes	Yes	Yes	3.82/-0.63	3.322/-0.554	TBD	ns
H→postadd unit register CLK setup/hold	Yes	Yes	Yes	3.61/-0.617	3.144/-0.537	TBD	ns
Z→postadd unit register CLK setup/hold	NA	NA	Yes	1.411/-0.23	1.227/-0.208	TBD	ns
Y→postadd unit register CLK setup/hold	NA	No	Yes	1.447/-0.27	1.259/-0.242	TBD	ns
X→postadd unit register CLK setup/hold	No	No	Yes	1.342/-0.28	1.167/-0.247	TBD	ns
PI→postadd unit register CLK setup/hold	NA	NA	Yes	1.314/-0.04	1.143/-0.035	TBD	ns
From Each Stage of Register CLK to APM Output Pin Time							
postadd unit register CLK→P output	NA	NA	NA	0.380	0.331	TBD	ns
Multiplier unit register CLK→P output	NA	NA	Yes	1.703	1.481	TBD	ns
Multiplier unit register CLK→Poutput	NA	NA	No	0.488	0.425	TBD	ns
pretadd unit register CLK→DPO output	Yes	Yes	Yes	2.58	2.248	TBD	ns
Z input unit register CLK→DPO output	NA	NA	Yes	1.59	1.390	TBD	ns
From Data/Control Pin to APM Output Pin Combinational Logic Delay							
Y→Poutput	NA	Yes	No	1.86	1.619	TBD	ns
Y→Poutput	NA	Yes	Yes	2.75	2.399	TBD	ns
Y→Poutput	NA	No	Yes	1.66	1.444	TBD	ns
X→Poutput	No	Yes	No	1.93	1.680	TBD	ns
X→Poutput	Yes	Yes	No	2.94	2.564	TBD	ns
X→Poutput	Yes	Yes	Yes	4.03	3.512	TBD	ns
X→Poutput	No	No	Yes	1.50	1.308	TBD	ns
H→Poutput	Yes	Yes	No	2.95	2.568	TBD	ns
H→Poutput	Yes	Yes	Yes	3.84	3.347	TBD	ns
Z→Poutput	NA	NA	Yes	1.62	1.410	TBD	ns
PI→Poutput	NA	NA	Yes	1.53	1.339	TBD	ns

Notes: The parameters in the table are only applicable to PG2L100H; for parameters of other devices in the Logos2 Family, please refer to the PDS timing report.

4.4 GPLL AC Characteristics Parameters

Table 4-4 GPLL AC Characteristics

Specification	Min.	Max.	Unit	Description
F_{IN}	10	800	MHz	Input Clock Frequency
F_{INJIT}	300		ps	Input clock jitter (F_{IN} < 200MHz)
	0.06		UI	Input clock jitter (F_{IN} ≥ 200MHz)
F_{INDT}	10-49MHz: 25% 50-199MHz: 30% 200-399MHz: 35% 400-499MHz: 40% 500-800MHz: 45%			Input clock duty cycle
F_{PFD}	10	450	MHz	PFD operating frequency range
F_{VCO}	600	1200	MHz	VCO operating frequency range
F_{OUT}	4.69	800	MHz	Output clock frequency range
F_{OUTCAS}	0.0366	800	MHz	Output cascade frequency range
T_{PHO}	0.12		ns	Static phase offset
T_{OUTJIT}	180		ps	Output clock jitter (F_{OUT} ≥ 100MHz)
	0.018		UI	Output clock jitter (F_{OUT} < 100MHz)
$T_{OUTDUTY}$	50%±5%			Output clock duty cycle precision (50%)
F_{BW}	1	4	MHz	Loop bandwidth
T_{LOCK}	---	200	us	Lock time
F_{DPS_CLK}	0.01	450	MHz	Dynamic phase shift clock frequency
T_{RST}	10	---	ns	Reset signal width

4.5 PPLL AC Characteristics Parameters

Table 4-5 PPLL AC Characteristics

Specification	Min.	Max.	Unit	Description
FIN	19	800	MHz	Input Clock Frequency
FINJIT	200		ps	Input clock jitter (F_{IN} < 200MHz)
	0.04		UI	Input clock jitter (F_{IN} ≥ 200MHz)
FINDT	10-49MHz: 25% 50-199MHz: 30% 200-399MHz: 35% 400-499MHz: 40% 500-800MHz: 45%			Input clock duty cycle
FPFD	19	450	MHz	PFD operating frequency range
FVCO	1330	2133	MHz	VCO operating frequency range
FOUT	10.39	2133	MHz	Output clock frequency range
TPHO	0.12		ns	Static phase offset

TOUTJTT	180		ps	Output clock jitter ($F_{OUT} \geq 100MHz$)
	0.018		UI	Output clock jitter ($F_{OUT} < 100MHz$)
TOUTDT	50%±5%			Output clock duty cycle precision (50%)
FBW	1	4	MHz	Bandwidth
TLOCK	---	120	us	Lock time
TRST	10	---	ns	Reset signal width

4.6 DQS AC Characteristics Parameters

Single-step phase offset values of DQS phase adjustment are shown in Table 4-6.

Table 4-6 DQS AC Characteristics

Categories	**Speed Grade**	**AC Characteristics Parameters Description**			**Unit**
		Min.	**Typ.**	**Max.**	
DQS	-5, -6	4	7	10	ps

4.7 Global Clock Network AC Characteristics Parameters

Table 4-7 Global Clock Network AC Characteristics

Item	**Maximum Frequency**	**Unit**	**Description**
	-5, -6		
GLOBAL CLK	600	MHz	Global Clock Network

4.8 Regional Clock Network AC Characteristics Parameters

Table 4-8 Regional Clock Network AC Characteristics

Item	**Maximum Frequency**	**Unit**	**Description**
	-5, -6		
REGIONAL CLK	350	MHz	Regional Clock Network

Notes: Maximum input frequency 650 MHz

4.9 IO Clock Network AC Characteristics Parameters

Table 4-9 IO Clock Network AC Characteristics

Item	**Maximum Frequency**	**Unit**	**Description**
	-5, -6		
IO CLK	680	MHz	IO Clock Network

4.10 Configuration and Programming AC Characteristics Parameters

4.10.1 Power-up Timing Characteristics

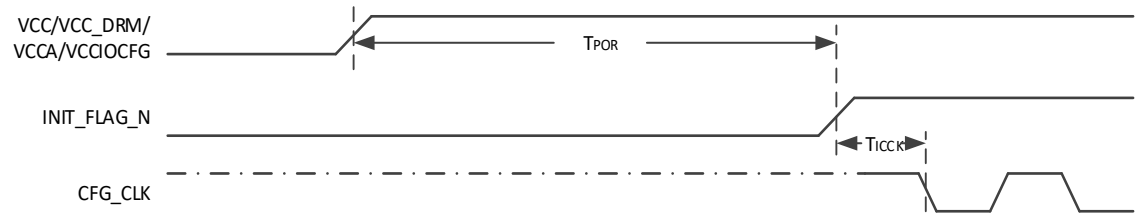

Figure 4-1 Device Power-up Timing Characteristics

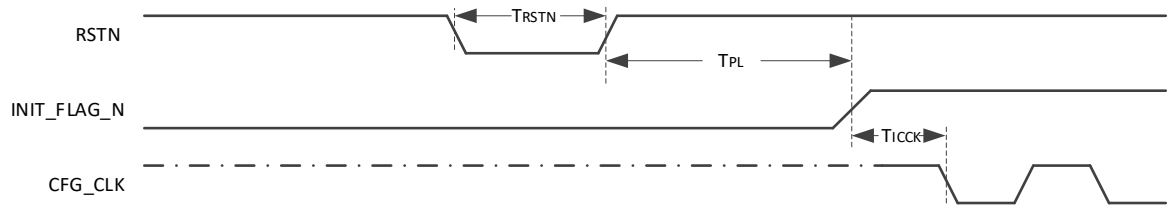

Figure 4-2 Device Reset and Reconfiguration Timing Characteristics

Table 4-10 Power-up Timing Characteristics Parameters

Item	Device	Value	Unit	Description
T_{PL}	PG2L25H	3.6	ms, Max	Program Latency
	PG2L50H	6		
	PG2L100H(X)	11		
	PG2L200H	26		
T_{POR}	PG2L25H	63.6	ms, Max	Power-on-Reset
	PG2L50H	66		
	PG2L100H(X)	71		
	PG2L200H	86		
T_{ICCK}	Logos2	400	ns,Min	CFG_CLK Output Delay
T_{RSTN}		384	ns,Min	RSTN Low Pulse Width

4.10.2 AC Characteristics of Each Download Mode

Table 4-11 AC Characteristics of Download Modes Supported by Logos2 Family FPGA

Interface	Item	Description	Value		Property
			-5	-6	
JTAG	F_{TCK}	TCK Frequency	50M	50M	Max
	F_{TCKD}	TCK Duty Cycle	45%/55%	45%/55%	Min/Max
	T_{TCKH}	TCK High Pulse Width	10ns	10ns	Min
	T_{TCKL}	TCK Low Pulse Width	10ns	10ns	Min
	T_{TMSSU}/T_{TDISU}	TMS/TDI Setup Time (TCK Rising Edge)	3.5ns	3.5ns	Min
	T_{TMSH}/T_{TDIH}	TMS/TDI Hold Time (TCK Rising Edge)	1.5ns	1.5ns	Min
	$T_{TCK2TDO}$	TCK Falling Edge to TDO Output Valid	6ns	6ns	Max
Master SPI Mode	F_{MCLK}	CFG_CLK Frequency	40M	40M	Max
		CFG_CLK Frequency (Low Speed)	15.38M	15.38M	Max
		CFG_CLK Frequency (Daisy Chain)	25M	25M	Max
	F_{MCLKS}	CFG_CLK Frequency Initial Value	2.99M	2.99M	Typ.
	F_{MCLKD}	CFG_CLK Duty Cycle	45%/55%	45%/55%	Min/Max
	$F_{MCLKTOL}$	CFG_CLK Frequency Deviation	50%	50%	Max
	F_{EMCLK}	ECCLKIN Frequency	40M	40M	Max
		ECCLKIN Frequency (Low Speed)	15.38M	15.38M	Max
	F_{EMCLKD}	ECCLKIN Duty Cycle	45%/55%	45%/55%	Min/Max
	T_{MDSU}	D[7:0] Setup Time (CFG_CLK Rising Edge)	9.5ns	9.5ns	Min
	T_{MDH}	D[7:0] Hold Time (CFG_CLK Rising Edge)	0ns	0ns	Min
	T_{MDSUF}	D[7:0] Setup Time (CFG_CLK Falling Edge)	9.5ns	9.5ns	Min
	T_{MDHF}	D[7:0] Hold Time (CFG_CLK Falling Edge)	0ns	0ns	Min
	T_{MCLK2D}	CFG_CLK Falling Edge to D[0]/D[4] Output Valid	3.5ns	3.5ns	Max
	$T_{MCLK2CS}$	CFG_CLK Falling Edge to FCS_N/FCS2_N Output Valid	4ns	4ns	Max
	$T_{MCLK2DOUT}$	CFG_CLK Falling Edge to CSO_DOUT Output Valid	3.5ns	3.5ns	Max
Slave Serial	F_{SSCLK}	CFG_CLK Frequency	50M	50M	Max
		CFG_CLK Frequency (Daisy Chain)	50M	50M	Max
	T_{SSCLKL}	CFG_CLK Low Pulse Width	6ns	6ns	Min
	T_{SSCLKH}	CFG_CLK High Pulse Width	6ns	6ns	Min
	T_{SSDSU}	DI Setup Time (CFG_CLK Rising Edge)	3.5ns	3.5ns	Min
	T_{SSDH}	DI Hold Time (CFG_CLK Rising Edge)	0ns	0ns	Min
	T_{SSDSUF}	DI Setup Time (CFG_CLK Falling Edge)	3.5ns	3.5ns	Min
	T_{SSDHF}	DI Hold Time (CFG_CLK Falling Edge)	0ns	0ns	Min
	$T_{SSCLK2DOUT}$	CFG_CLK Falling Edge to CSO_DOUT Output Valid	2ns/7ns	2ns/7ns	Min/Max
Slave	F_{SPCLK}	CFG_CLK Frequency	20M	50M	Max

Interface	Item	Description	Value		Property
			-5	-6	
Parallel	T_{SPCLKL}	CFG_CLK Low Pulse Width	6ns	6ns	Min
	T_{SPCLKH}	CFG_CLK High Pulse Width	6ns	6ns	Min
	T_{SPDSU}	D[31:0] Setup Time (CFG_CLK Rising Edge)	5.5ns	5.5ns	Min
	T_{SPDH}	D[31:0] Hold Time (CFG_CLK Rising Edge)	0.5ns	0.5ns	Min
	T_{SPCRSU}	CS_N/RWSEL Setup Time (CFG_CLK Rising Edge)	4.5ns	4.5ns	Min
	T_{SPCRH}	CS_N/RWSEL Hold Time (CFG_CLK Rising Edge)	0.5ns	0.5ns	Min
	$T_{SPCLK2D}$	CFG_CLK Rising Edge to D[31:0] Output Valid	9ns	9ns	Max
	$T_{SPCS2CSO}$	CS_N to CSO_DOUT Output Delay	8.5ns	8.5ns	Max
Internal slave parallel interface	F_{IPCLK}	CLK Frequency	20M	50M	Max
	T_{IPCLKL}	CLK Low Pulse Width	2.5ns	2.5ns	Min
	T_{IPCLKH}	CLK High Pulse Width	2.5ns	2.5ns	Min
	T_{IPDSU}	CS_N/RW_SEL/DI[31:0] Setup Time (CLK Rising Edge)	2ns	2ns	Min
	T_{IPDH}	CS_N/RW_SEL/DI[31:0] Hold Time (CLK Rising Edge)	1ns	1ns	Min
	$T_{IPCLK2D}$	CLK Rising Edge to DO[31:0] Output Valid	4ns	4ns	Max
	$T_{IPCLK2D1}$	CLK Rising Edge to RBCRC_VALID/ECC_VALID/DRCFG_OVER/PRCFG_OVER Valid	2ns	2ns	Max
	$T_{IPCLK2D2}$	CLK Rising Edge to RBCRC_ERR/ ECC_INDEX/SERROR/DERROR/ SEU_FRAME_ADDR/SEU_FRAME_NADDR SEU_COLUMN_ADDR/SEU_COLUMN_NADDR SEU_REGION_ADDR/SEU_REGION_NADDR DRCFG_ERR/PRCFG_ERR Output Valid	0	0	Max

4.11 IOB High Range (HR) AC Characteristics Parameters

IOB High Range (HR) AC characteristics parameters are as shown in Table 4-12, where DO=>PAD is the delay from IOB port DO through OBUF to PAD; PAD=>DIN is the delay from PAD through IBUF to IOB port DIN.

Table 4-12 IOB High Range (HR) AC Characteristics Parameters

I/O Std	Delay(DO=>PAD)/ns	Delay(PAD=>DIN)/ns
LVCMOS33 STRENGTH"4" MODE"F"	1.705	0.8347
LVCMOS33	2.376	0.8347

I/O Std	Delay(DO=>PAD)/ns	Delay(PAD=>DIN)/ns
STRENGTH "4" MODE"S"		
LVCMOS33 STRENGTH"8" MODE"F"	1.688	0.8347
LVCMOS33 STRENGTH"8" MODE"S"	2.369	0.8347
LVCMOS33 STRENGTH"12" MODE"F"	1.466	0.8347
LVCMOS33 STRENGTH"12" MODE"S"	2.172	0.8347
LVCMOS33 STRENGTH"16" MODE"F"	1.266	0.8347
LVCMOS33 STRENGTH"16" MODE"S"	1.913	0.8347
LVTTL33 STRENGTH"4" MODE"F"	1.705	0.8347
LVTTL33 STRENGTH"4" MODE"S"	2.376	0.8347
LVTTL33 STRENGTH"8" MODE"F"	1.688	0.8347
LVTTL33 STRENGTH"8" MODE"S"	2.369	0.8347
LVTTL33 STRENGTH"12" MODE"F"	1.466	0.8347
LVTTL33 STRENGTH"12" MODE"S"	2.172	0.8347
LVTTL33 STRENGTH"16" MODE"F"	1.266	0.8347
LVTTL33 STRENGTH"16" MODE"S"	1.913	0.8347
LVTTL33 STRENGTH"24" MODE"F"	1.266	0.8347
LVTTL33 STRENGTH"24" MODE"S"	1.913	0.8347
LVCMOS25 STRENGTH"4" MODE"F"	1.49	0.8982
LVCMOS25 STRENGTH"4" MODE"S"	2.084	0.8982

I/O Std	Delay(DO=>PAD)/ns	Delay(PAD=>DIN)/ns
LVCMOS25 STRENGTH"8" MODE"F"	1.525	0.8982
LVCMOS25 STRENGTH"8" MODE"S"	2.325	0.8982
LVCMOS25 STRENGTH"12" MODE"F"	1.354	0.8982
LVCMOS25 STRENGTH"12" MODE"S"	2.115	0.8982
LVCMOS25 STRENGTH"16" MODE"F"	1.23	0.8982
LVCMOS25 STRENGTH"16" MODE"S"	1.903	0.8982
LVCMOS18 STRENGTH"4" MODE"F"	1.068	0.996
LVCMOS18 STRENGTH"4" MODE"S"	1.274	0.996
LVCMOS18 STRENGTH"8" MODE"F"	0.9271	0.996
LVCMOS18 STRENGTH"8" MODE"S"	1.151	0.996
LVCMOS18 STRENGTH"12" MODE"F"	0.8111	0.996
LVCMOS18 STRENGTH"12" MODE"S"	0.9624	0.996
LVCMOS18 STRENGTH"16" MODE"F"	0.8024	0.996
LVCMOS18 STRENGTH"16" MODE"S"	0.9805	0.996
LVCMOS18 STRENGTH"24" MODE"F"	0.8218	0.996
LVCMOS18 STRENGTH"24" MODE"S"	0.9408	0.996
LVCMOS15 STRENGTH"4" MODE"F"	1.003	1.091
LVCMOS15 STRENGTH"4" MODE"S"	1.214	1.091
LVCMOS15 STRENGTH"8"	1.003	1.091

I/O Std	Delay(DO=>PAD)/ns	Delay(PAD=>DIN)/ns
MODE"F"		
LVCMOS15 STRENGTH"8" MODE"S"	1.214	1.091
LVCMOS15 STRENGTH"12" MODE"F"	0.7844	1.091
LVCMOS15 STRENGTH"12" MODE"S"	0.9222	1.091
LVCMOS15 STRENGTH"16" MODE"F"	0.8026	1.091
LVCMOS15 STRENGTH"16" MODE"S"	0.9151	1.091
LVCMOS12 STRENGTH"4" MODE"F"	0.9499	1.238
LVCMOS12 STRENGTH"4" MODE"S"	1.156	1.238
LVCMOS12 STRENGTH"8" MODE"F"	0.9499	1.238
LVCMOS12 STRENGTH"8" MODE"S"	1.156	1.238
LVCMOS12 STRENGTH"12" MODE"F"	0.9118	1.238
LVCMOS12 STRENGTH"12" MODE"S"	1.034	1.238
SSTL18_I STRENGTH"8" MODE"F"	0.7247	0.871
SSTL18_I STRENGTH"8" MODE"S"	0.8676	0.871
SSTL18_II STRENGTH"13.4" MODE"F"	0.6479	0.871
SSTL18_II STRENGTH"13.4" MODE"S"	0.7475	0.871
SSTL18D_I STRENGTH"8" MODE"F"	0.7247	0.871
SSTL18D_I STRENGTH"8" MODE"S"	0.8676	0.871
SSTL18D_II STRENGTH"13.4" MODE"F"	0.6479	0.871

I/O Std	Delay(DO=>PAD)/ns	Delay(PAD=>DIN)/ns
SSTL18D_II STRENGTH"13.4" MODE"S"	0.7475	0.871
HSTL18_I STRENGTH"8" MODE"F"	0.7247	0.871
HSTL18_I STRENGTH"8" MODE"S"	0.8676	0.871
HSTL18_II STRENGTH"16" MODE"F"	0.6479	0.871
HSTL18_II STRENGTH"16" MODE"S"	0.7475	0.871
HSTL18D_I STRENGTH"8" MODE"F"	0.7247	0.871
HSTL18D_I STRENGTH"8" MODE"S"	0.8676	0.871
HSTL18D_II STRENGTH"16" MODE"F"	0.6479	0.871
HSTL18D_II STRENGTH"16" MODE"S"	0.7475	0.871
SSTL15_I STRENGTH"8.9" MODE"F"	0.7278	0.9481
SSTL15_I STRENGTH"8.9" MODE"S"	0.8599	0.9481
SSTL15_II STRENGTH"13" MODE"F"	0.7295	0.9481
SSTL15_II STRENGTH"13" MODE"S"	0.8726	0.9481
SSTL15D_I STRENGTH"8.9" MODE"F"	0.7278	0.9481
SSTL15D_I STRENGTH"8.9" MODE"S"	0.8599	0.9481
SSTL15D_II STRENGTH"13" MODE"F"	0.7295	0.9481
SSTL15D_II STRENGTH"13" MODE"S"	0.8726	0.9481
HSTL15_I STRENGTH"8" MODE"F"	0.7278	0.9481
HSTL15_I STRENGTH"8"	0.8599	0.9481

I/O Std	Delay(DO=>PAD)/ns	Delay(PAD=>DIN)/ns
MODE"S"		
HSTL15_II STRENGTH"16" MODE"F"	0.7295	0.9481
HSTL15_II STRENGTH"16" MODE"S"	0.8726	0.9481
HSTL15D_I STRENGTH"8" MODE"F"	0.7278	0.9481
HSTL15D_I STRENGTH"8" MODE"S"	0.8599	0.9481
HSTL15D_II STRENGTH"16" MODE"F"	0.7295	0.9481
HSTL15D_II STRENGTH"16" MODE"S"	0.8726	0.9481
SSTL135_I STRENGTH"8.9" MODE"F"	0.7459	1.071
SSTL135_I STRENGTH"8.9" MODE"S"	0.8795	1.071
SSTL135_II STRENGTH"13" MODE"F"	0.7036	1.071
SSTL135_II STRENGTH"13" MODE"S"	0.8431	1.071
SSTL135D_I STRENGTH"8.9" MODE"F"	0.7459	1.071
SSTL135D_I STRENGTH"8.9" MODE"S"	0.8795	1.071
SSTL135D_II STRENGTH"13" MODE"F"	0.7036	1.071
SSTL135D_II STRENGTH"13" MODE"S"	0.8431	1.071
LPDDR MODE"F"	0.9499	1.238
LPDDR MODE"S"	1.156	1.238
HSUL12 MODE"F"	0.9499	1.238
HSUL12 MODE"S"	1.156	1.238
TMDS	0.9883	0.9481
LVDS25	0.9883	0.9481
MINI-LVDS	0.9883	0.9481
RSDS	0.9883	0.9481
PPDS	0.9883	0.9481

Chapter 5 Performance Parameters Under Typical Operating Conditions (Fabric Performance)

This chapter lists the performance characteristics of common applications for Logos2 Family FPGAs.

5.1 LVDS Performance Parameters

Table 5-1 LVDS Performance

Description		Maximum Rate		Unit	IO Resources
		-5	-6		
SDR LVDS Transmitter	PG2L100H	400	450	Mbps	OSERDES (DATA _WIDTH =4 TO 8)
	PG2L25H, PG2L50H, PG2L100HX, PG2L200H	TBD	625	Mbps	
DDR LVDS Transmitter	PG2L100H	800	900	Mbps	OSERDES (DATA _WIDTH =4 TO 8)
	PG2L25H, PG2L50H, PG2L100HX, PG2L200H	TBD	1250	Mbps	
SDR LVDS Receiver	PG2L100H	400	450	Mbps	ISERDES (DATA _WIDTH =4 TO 8)
	PG2L25H, PG2L50H, PG2L100HX, PG2L200H	TBD	625	Mbps	
DDR LVDS Receiver	PG2L100H	800	900	Mbps	ISERDES (DATA _WIDTH =4 TO 8)
	PG2L25H, PG2L50H, PG2L100HX, PG2L200H	TBD	1250	Mbps	

5.2 Memory Interface Performance Parameters

Table 5-2 Memory Interface Performance

Item	Maximum Rate		Unit
	-5	-6	
DDR3	800	1066	Mbps
DDR3L	667	667	Mbps
DDR2	667	667	Mbps
LPDDR2	667	667	Mbps
LPDDR	400	400	Mbps
QDR2	500	500	Mbps

5.3 DRM (Dedicated RAM Module) Performance Parameters

Table 5-3 DRM Performance

Mode	Maximum Rate (MHz)

	-5	**-6**
DRM (NW mode & read register enabled) @ 18K memory mode	300	400
DRM (TW mode & read register enabled) @ 18K memory mode	300	400
DRM (RBW mode & read register enabled) @ 18K memory mode	250	350
DRM (synchronous FIFO mode & read register enabled)	300	400
DRM (ECC Mode)	200	300

5.4 APM (Arithmetic Process Module) Performance Parameters

Table 5-4 APM Performance

Condition	**Maximum Rate (MHz)**	
	-5	**-6**
All registers used (using registers at every stage of APM)	350	460
Only use INREG and PREG (only use APM's input and output registers)	160	190

Chapter 6 ADC (Analog to Digital Converter) Characteristics

This chapter mainly introduces the characteristic parameters of the ADC Hard Core for Logos2 Family FPGAs, as shown in Table 6-1.

Table 6-1 ADC Hard Core Characteristics

Parameter	**Min.**	**Typ.**	**Max.**	**Unit**	**Description/Condition**	
VCCADC = 1.8V ±5%, VREFADC_P = 1.255V, VREFADC_N = 0V, ADC_CLK_OUT = 26 MHz, Tj: –40 ℃ ~100 ℃, dedicated channel; Typical values at Tj=+40 ℃ Vinp-p=-0.45dB Full Scale;						
VCCADC	1.71	1.8	1.89	V	Analog Supply Voltage	
Resolution	12	--	--	Bits	Resolution	
Sample Rate	--	--	1	MSPS	Sampling rate	
Channel	--	--	17		Channel	
Voltage Reference[1]	1.205	1.255	1.305	V	External reference voltage	
	1.230	1.255	1.280	V	Internal reference voltage	Ground VREFP pin to AGND, –40°C≤ Tj ≤100°C
Offset Error	--	--	±4	LSB	Bipolar	–40°C≤ Tj <100°C
	--	--	±12	LSB	Unipolar	–40°C≤ Tj ≤100°C
Gain Error	--	±1	--	%FS	Gain error after gain error calibration	
DNL	--	--	-1<DNL<5	LSB	Differential Nonlinear; No missing codes	
INL	--	--	±4	LSB	Integeral Nonlinear	–40°C≤ T_j ≤100°C
SNR_1		58	--	dB	Signal to Noise Ratio	F_{SAMPLE} = 500KS/s,F_{IN} = 20 kHz Dedicated channel
SNR_2		58		dB	Signal to Noise Ratio	F_{SAMPLE} = 500KS/s,F_{IN} = 20 kHz Auxiliary channel
THD_1	--	64		dB	2^{nd} to 7^{th} total harmonic distortion	F_{SAMPLE} = 500KS/s,F_{IN} = 20 kHz Dedicated channel
THD_2	--	62		dB	2^{nd} to 7^{th} total harmonic distortion	F_{SAMPLE} = 500KS/s,F_{IN} = 20 kHz Auxiliary channel
Temperature Sensor Accuracy[1]	--	--	±4	℃	Temperature sensing accuracy	–40°C≤ Tj ≤100°C
Voltage Sensor Accuracy[1]			±5	%	On-chip power supply voltage detection accuracy	Voltage measurement range: V_{CC}/V_{CC_DRM}:1V ±3% V_{CCA}:1.8V ±5% Temperature range: –40°C ≤Tj ≤100°C
DCLK	8		100	MHz	APB interface clock	
DCLK Duty Cycle	40		60	%		

Notes:

1. The on-chip temperature detection accuracy and on-chip power supply voltage detection accuracy are the test results after enabling the calibration of Offset Error and Gain Error, with ADC sampling clock frequency between 1MHz and 5MHz; any changes in the

reference voltages VREFADC_P=1.255V and VREFADC_N=0V will affect the accuracy of the measured temperature and power supply voltage.

2. For ADC sampling auxiliary IO channels, the auxiliary IO must be constrained within a 1.8V power domain;
3. Grade -5 does not support temperature sensors

Chapter 7 High-Speed Serial Transceiver (HSSTLP) Characteristics

This chapter mainly introduces the characteristics of the HSSTLP Hard Core for Logos2 Family FPGAs, including absolute voltage/current rating limits, recommended operating conditions, AC/DC characteristics, and features under typical protocol working modes.

7.1 HSSTLP Hard Core Absolute Voltage Limits and Current Rating

Table 7-1 HSSTLP Absolute Voltage Limits and Current Rating

Item	Min.	Max.	Unit	Description
HSSTAVCC	–0.5	1.21	V	HSST analogue power supply 1.0V voltage
HSSTAVCCPLL	–0.5	1.32	V	HSST PLL analog power supply 1.2V voltage

Note: Exceeding the above ratings limits may cause permanent damage to the device.

7.2 Recommended Operating Conditions for HSSTLP Hard Core

The following table shows the recommended operating voltages for the HSSTLP Hard Core of Logos2 Family FPGAs.

Table 7-2 Recommended Operating Conditions for HSSTLP Hard Core

Item	Min.	Typ.	Max.	Unit	Description
Voltage Values					
HSSTAVCC	0.97	1.0	1.03	V	HSST analogue power supply 1.0V voltage
HSSTAVCCPLL	1.17	1.2	1.23	V	HSST PLL analog power supply 1.2V voltage

7.3 HSSTLP Hard Core DC Characteristics Parameters

Table 7-3 HSSTLP Hard Core DC Characteristics

Item	Min	Typ.	Max	Unit	Condition	Description
Input and Output Signals DC Characteristics						
HSST_V_{DINPP}	150	-	1000	mV	External AC coupled	Differential input peak-to-peak voltage
HSST_V_{DIN}	0	-	HSSTAVCC	mV	DC coupled, HSSTAVCC=1V	Input absolute voltage values
HSST_V_{INCM}	-	3/4 HSSTAVCC	-	mV	DC coupled, HSSTAVCC=1V	Common mode input voltage value
HSST_V_{DOUTPP}	900	-	-	mV	Swing set to maximum	Differential output peak-to-peak

Item	Min	Typ.	Max	Unit	Condition	Description
						voltage
HSST_$V_{OUTCMDC}$	HSSTAVCC– DV_{OUTPP}/4			mV	DC common mode output voltage, when the transmitter side is floating	
HSST_$V_{OUTCMAC}$	1/2 HSSTAVCC			mV	Common mode output voltage: External AC coupled	
HSST_R_{DIN}	-	100	-	Ω	Differential input resistance	
HSST_R_{DOUT}	-	100	-	Ω	Differential output resistance	
HSST_TX_{SKEW}	-	-	14	ps	Skew between P and N sides of TX output	
HSST_C_{DEXT}	-	100	-	nF	Recommended external AC coupling capacitor value	
Reference Clock Input DC Characteristics						
HSST_V_{RCLKPP}	400	-	2000	mV	Differential input peak-to-peak voltage	
HSST_R_{RCLK}	-	100	-	Ω	Differential input resistance	
HSST_$C_{RCLKEXT}$	-	100	-	nF	Recommended external AC coupling capacitor value	

7.4 High-Speed Serial Transceiver (HSSTLP) AC Characteristics

The AC characteristics of the HSSTLP Hard Core are shown in Table 7-4 to Table 7-9.

Table 7-4 HSST Hard Core Performance Parameters

Item	Value			Unit	Description
	-5	-6	-7		
HSST_Fmax	5	6.6	TBD	Gbps	Maximum data rate of HSST
HSST_Fmin	0.6	0.6	TBD	Gbps	Minimum data rate of HSST
HSST_Fpllmax	5	6.6	TBD	GHz	Maximum frequency of HSST PLL
HSST_Fpllmin	1.6	1.6	TBD	GHz	Minimum frequency of HSST PLL

The HSSTLP reference clock switching characteristics are shown in Table 7-5.

Table 7-5 HSSTLP Hard Core Reference Clock Switching Characteristics

Item	Value			Unit	Condition	Description
	Min	Typ.	Max			
HSST_F_{REFCLK}	60	-	330	MHz	Reference clock frequency range	
HSST_T_{RCLK}	-	225	-	ps	20%-80%	Reference clock rise time
HSST_T_{FCLK}	-	225	-	ps	80%-20%	Reference clock fall time
HSST_T_{RATIO}	45	50	55	%	PLL	Reference clock duty cycle

Table 7-6 HSSTLP Hard Core PLL/Lock Time Characteristics

Item	Value			Unit	Condition	Description
	Min	Typ.	Max			
HSST_$T_{PLLLOCK}$	-	-	1.5	ms		PLL lock time, the time from reset release to lock
HSST_$T_{CDRLOCK}$	-	60,000	2,500,000	UI	The time it takes for the CDR to lock after the PLL has locked onto a reference clock and before switching to receiving external input data	CDR lock time

The HSST Hard Core user clock switching characteristics are shown in Table 7-7.

Table 7-7 HSSTLP Hard Core User Clock Switching Characteristics

Item	Frequency		Unit	Description
Data Interface Clock Switching Characteristics				
HSST_FT2C	206.25	MHz	Maximum frequency of P_CLK2CORE_TX	
HSST_FR2C	206.25	MHz	Maximum frequency of P_CLK2CORE_RX	
HSST_FTFC	206.25	MHz	Maximum frequency of P_TX_CLK_FR_CORE	
HSST_FRFC	206.25	MHz	Maximum frequency of P_RX_CLK_FR_CORE	
APB Dynamic Configuration Interface Clock Switching Characteristics				
HSST_FAPB	100	MHz	Maximum frequency of APB CLK	

The HSST Hard Core Transmitter side switching characteristics are shown in Table 7-8.

Table 7-8 HSSTLP Hard Core Transmitter Side Switching Characteristics

Item	Min	Typ.	Max	Unit	Condition	Description
HSST_T_{TXR}	-	100	-	ps	20%-80%	TX Rising Time
HSST_T_{TXF}	-	100	-	ps	80%-20%	TX Falling Time
HSST_T_{CHSKEW}	-	-	500	ps	-	TX channel-to-channel skew
HSST_$V_{TXIDLEAMP}$	-	-	30	mV	-	Electrical idle amplitude
HSST_$V_{TXIDLETIME}$	-	-	150	ns	-	Electrical idle transition time
HSST_$TJ_{0.6G}$	-	-	0.1	UI	0.6Gbps	Total Jitter
HSST_$DJ_{0.6G}$	-	-	0.05	UI		Deterministic Jitter
HSST_$TJ_{1.25G}$	-	-	0.1	UI	1.25Gbps	Total Jitter
HSST_$DJ_{1.25G}$	-	-	0.05	UI		Deterministic Jitter
HSST_$TJ_{2.5G}$	-	-	0.2	UI	2.5Gbps	Total Jitter
HSST_$DJ_{2.5G}$	-	-	0.08	UI		Deterministic Jitter
HSST_$TJ_{3.125G}$	-	-	0.2	UI	3.125Gbps	Total Jitter
HSST_$DJ_{3.125G}$	-	-	0.08	UI		Deterministic Jitter
HSST_$TJ_{5.0G}$	-	-	0.3	UI	5.0Gbps	Total Jitter
HSST_$DJ_{5.0G}$	-	-	0.1	UI		Deterministic Jitter

Item	Min	Typ.	Max	Unit	Condition	Description
HSST_TJ$_{6.6G}$	-	-	0.3	UI	6.6Gbps	Total Jitter
HSST_DJ$_{6.6G}$	-	-	0.1	UI		Deterministic Jitter

The HSST Hard Core Receiver side switching characteristics are shown in Table 7-9.

Table 7-9 HSSTLP Hard Core Receiver Side Switching Characteristics

Item	Min	Typ.	Max	Unit	Description
HSST_TRXIDLETIME	-		34	ns	Time from RXELECIDLE state to LOS signal response
HSST_RXVPPOOB	72	-	210	mV	OOB detection threshold peak-to-peak value
HSST_RXTRACK	-5000	-	5000	ppm	Receiver spread spectrum following, 33kHz modulation frequency
HSST_RXLENGTH	-	-	512	UI	Support for the length of RX continuous long 0 or long 1
HSST_RXTOLERANCE	-1250	-	1250	ppm	Frequency deviation tolerance of data/reference clock
Sinusoidal jitter tolerance					
HSST_SJ_0.6	TBD	-	-	UI	Sinusoidal jitter[1], 0.6Gbps
HSST_SJ_1.25	0.42	-	-	UI	Sinusoidal jitter[1], 1.25Gbps
HSST_SJ_2.5	0.42	-	-	UI	Sinusoidal jitter[1], 2.5Gbps
HSST_SJ_3.125	0.4	-	-	UI	Sinusoidal jitter[1], 3.125Gbps
HSST_SJ_5.0	0.4	-	-	UI	Sinusoidal jitter[1], 5.0Gbps
HSST_SJ_6.6	0.4	-	-	UI	Sinusoidal jitter[1], 6.6Gbps

Notes:

1. The frequency of the injected sinusoidal jitter is 10MHz

Chapter 8 PCIe Hard Core Features

Table 8-1 PCIe Performance Parameters

Item	Value	Unit	Description
Fpclk	250	MHz	Maximum Clock Frequency of PCIe Core
Fpclk_div2	125	MHz	Maximum Clock Frequency of User Interface

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