Compa Family CPLDs Embedded Hard Core User Guide

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.3	22.05.2023	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
SPI	Serial Peripheral Interface
I2C	Inter-Integrated Circuit bus
PWM	Pulse-Width Modulation

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Chapter 1 **General Introduction**

CPLD Family products feature a rich set of high-performance, low-power embedded hard cores, including one SPI hard core, two I^2C hard cores, andone timer hard core, among others. The embedded hard cores are configured with an 8-bit slave APB interface (as shown in Figure 2-1), compatible with the AMBA APB3 protocol, with a maximum clock frequency of 100MHz. The hard cores also have interrupt function (as shown in Figure 2-2) and can be configured into interrupt mode.

Embedded hard cores simplify the design implementation process, saving resources such as LUTs, registers, clocks, and routes, thus providing designers with more options. Moreover, the hard cores feature low power consumption, low latency, and high rates, which can replace external dedicated chips, saving more space for hardware placement and routing. CPLDs are widely used in consumer electronics, communications, automotive electronics, digital television, and other fields, with abundant embedded hard core resources increasingly favoured by engineers.

Chapter 2 APB Bus

2.1 Schematics

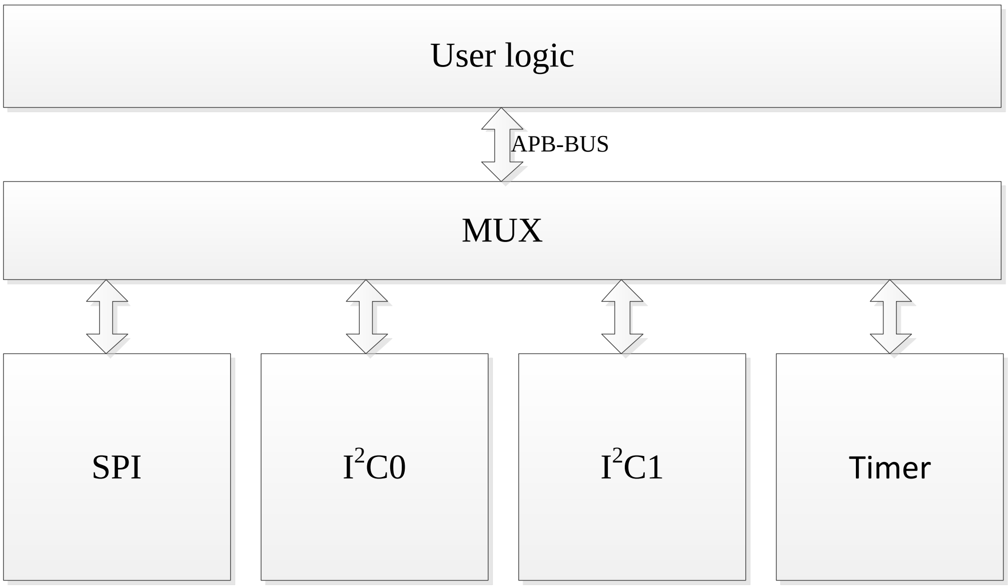

Figure 2-1 Embedded Hard Core Module Connection Diagram

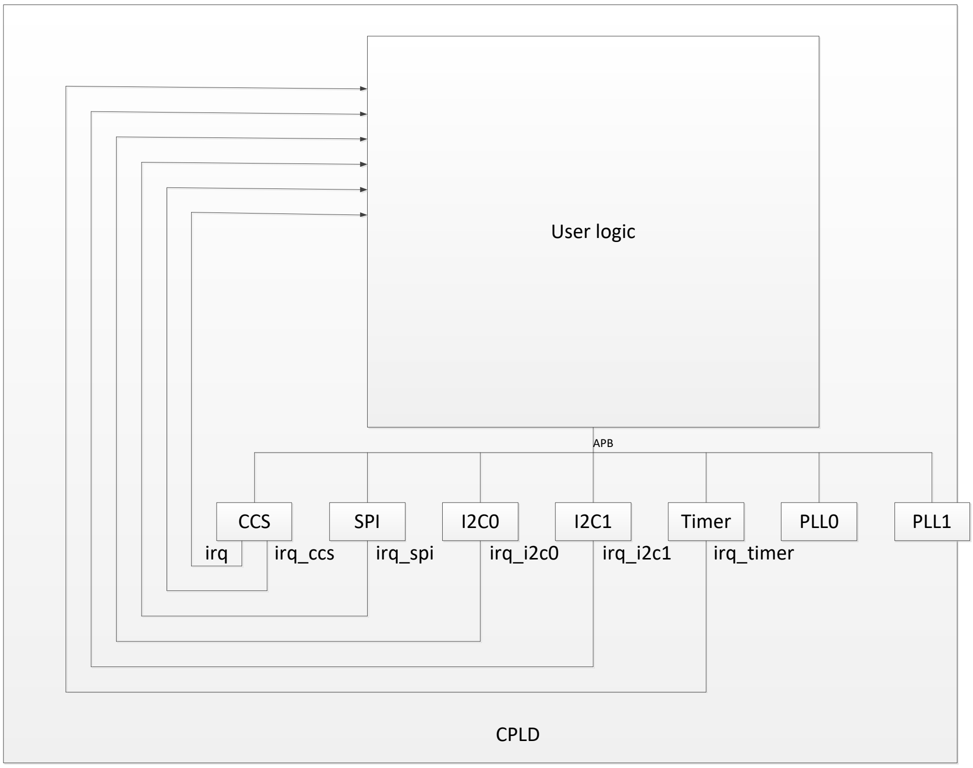

Figure 2-2 CPLD Embedded Hard Core Interrupt Connection Diagram

2.2 APB Primitive

When using embedded hard cores, the user must instantiate the corresponding GTP primitive, which needs to be used in conjunction with GTP_APB, to control the hard core operating mode through operations on GTP_APB. The relevant information for GTP_APB is described as below.

```
GTP_APB    U_GTP_APB
(
            .CLK            (clk            ),
            .RST_N          (rst_sys_n      ),
            .ADDR           (addr           ),
            .SEL_CCS        (sel_ccs        ),
            .SEL_SPI        (sel_spi        ),
            .SEL_I2C0       (sel_i2c0       ),
            .SEL_I2C1       (sel_i2c1       ),
            .SEL_TIMER      (sel_timer      ),
            .SEL_PLL0       (sel_pll0       ),
            .SEL_PLL1       (sel_pll1       ),
            .EN             (en             ),
            .WR             (wr             ),
            .WDATA          (wdata          ),
            .RDATA          (rdata          ),
            .RDY            (rdy            ),
            .IRQ            (irq            ),
            .IRQ_CCS        (irq_ccs        )
);
```

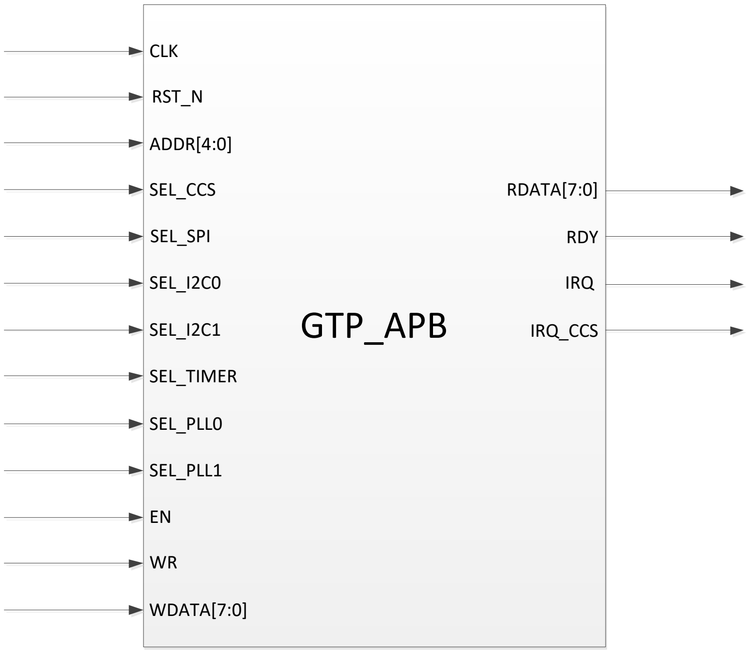

Figure 2-3 GTP_APB Signal Input/Output Diagram

Table 2-1 GTP_APB Port Description List

Port Name	**Direction**	**Function Description**
CLK	Input	Clock, sampling on the rising edge, with a maximum frequency of 100M
RST_N	Input	Asynchronous reset, active low
ADDR[4:0]	Input	Address Bus
SEL_CCS	Input	Select CCS, active high
SEL_SPI	Input	Select SPI, active high
SEL_I2C0	Input	Select I2C0, active high
SEL_I2C1	Input	Select I2C1, active high
SEL_TIMER	Input	Select timer, active high
SEL_PLL0	Input	Select PLL0, active high
SEL_PLL1	Input	Select PLL1, active high
EN	Input	Enable, active high, indicating the second and subsequent cycles of transmission
WR	Input	Read/Write selection. 0: Read; 1: Write
WDATA[7:0]	Input	Data bus input
RDATA[7:0]	Output	Data bus output
RDY	Output	Ready, indicating the end of a normal bus cycle
IRQ	Output	General interrupt
IRQ_CCS	Output	CCS interrupt

2.3 APB Interface Timing

2.3.1 Write Operation

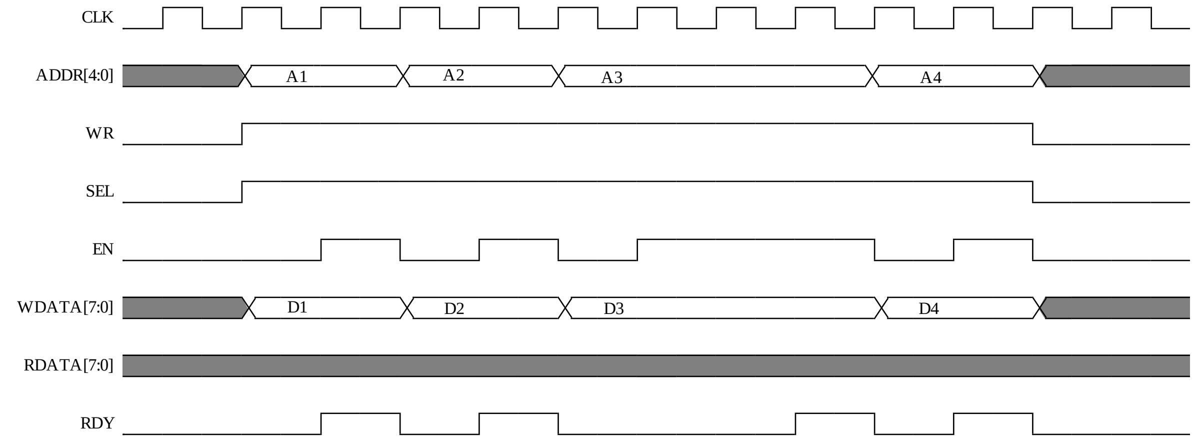

Figure 2-4 APB Interface Continuous Write Timing Diagram

2.3.2 Read Operation

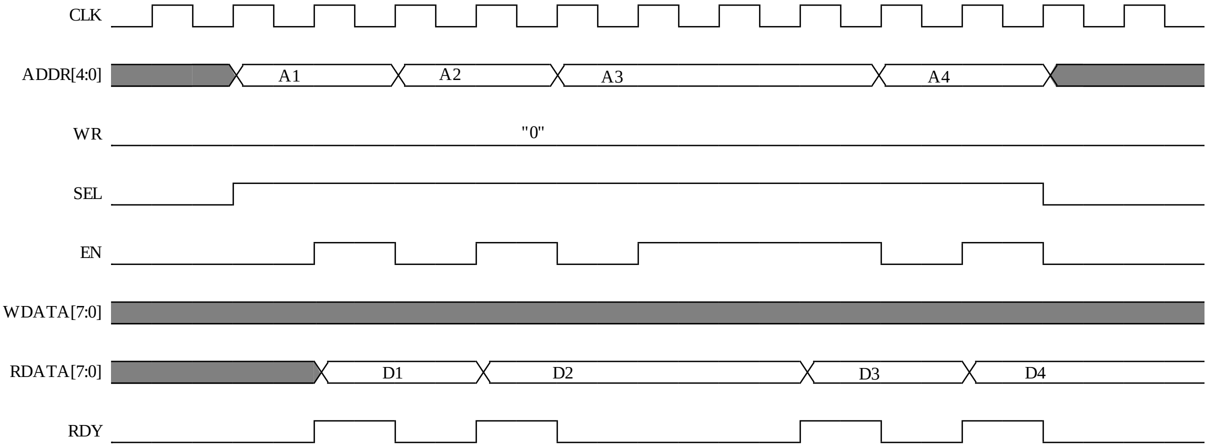

Figure 2-5 APB Interface Continuous Read Timing Diagram

2.3.3 Back-to-Back

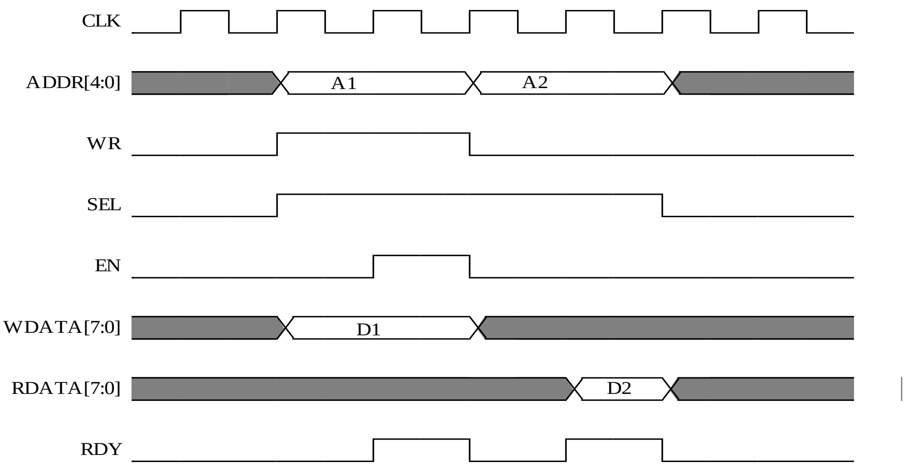

Figure 2-6 APB Interface Write Before Read Timing Diagram

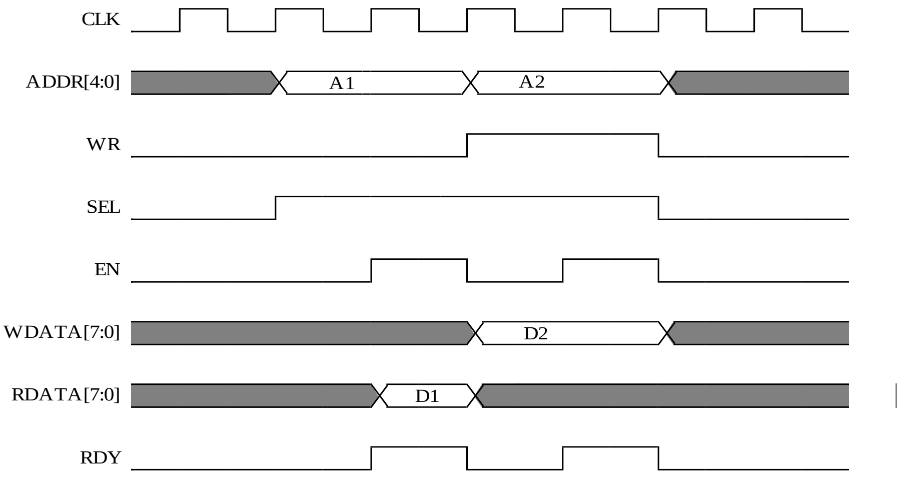

Figure 2-7 APB Interface Read Before Write Timing Diagram

Chapter 3 **SPI Hard IP**

The CPLD Family products include an SPI hard core that can be configured into master/slave SPI mode; when the SPI hard core is configured into master mode, it can control other devices through the connected slave SPI interface on the SPI bus. When the SPI hard core is configured as a slave, it can be directly connected to an external SPI master device interface.

3.1 Features

- 8-bit slave APB interface, compatible with AMBA APB3 protocol, with 1K/2K/4K/7K clock frequency up to 100MHz, and 10K clock frequency up to 76MHz
- SPI master/slave operation, with 1K/2K/4K/7K master operation frequency up to 25MHz, and slave operation frequency up to 100MHz; 10K chip master operation frequency up to 19MHz, and slave operation frequency up to 76MHz
- Controls up to 8 slave devices
- Double-buffered data registers
- Clock programmable polarity and phase
- Data transfer LSB/MSB order selection
- Interrupt

3.2 SPI Primitive

When using SPI hard cores, the user must instantiate the corresponding GTP_SPI primitive, which needs to be used in conjunction with GTP_APB. The relevant information for GTP_SPI is described as below.

```
GTP_SPI   U_GTP_SPI
(
.SCK_OE_N      (SCK_OE_N      ),
.SCK_I         (SCK_I          ),
.SCK_O      (SCK_O          ),
.SS_O_N        (SS_O_N          ),
.SS_I_N        (SS_I_N          ),
.MISO_OE_N   (MISO_OE_N    ),
.MISO_I       (MISO_I        ),
.MISO_O       (MISO_O        ),
.MOSI_OE_N   (MOSI_OE_N    ),
.MOSI_I       (MOSI_I        ),
.MOSI_O       (MOSI_O       ),
.IRQ          (IRQ          )
);
```

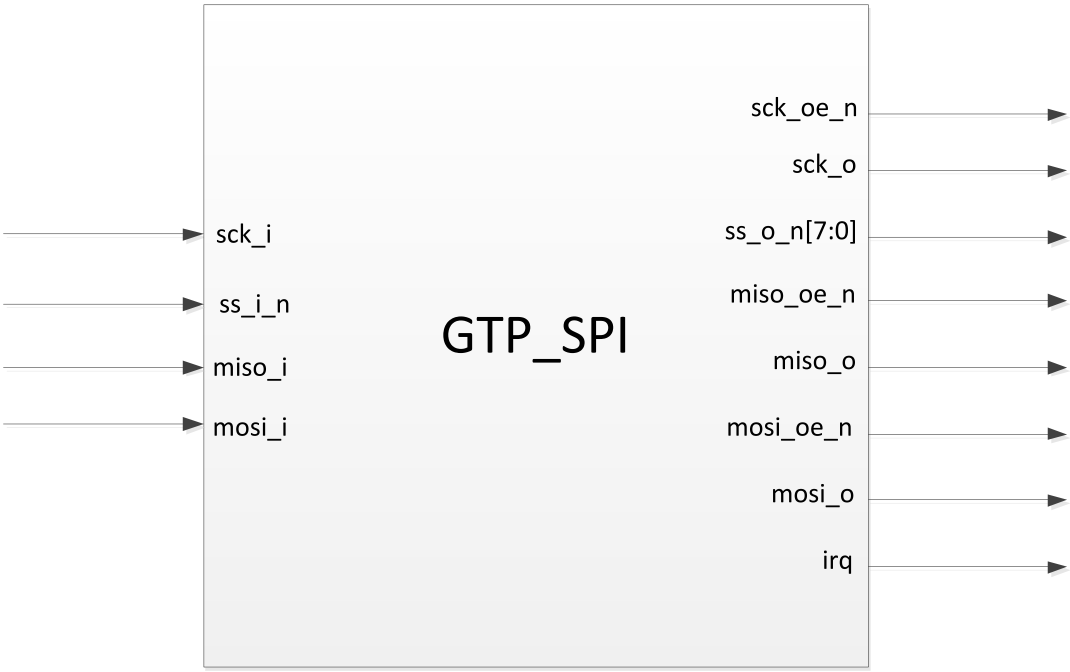

Figure 3-1 GTP_SPI Module Input/Output Diagram

Table 3-1 GTP_SPI Port Description List

Item	Direction	Description
sck_oe_n	Output	Serial clock output enable, active low
sck_i	Input	Serial clock input The maximum frequency ratio between slave mode sck and pclk: Write: 45:100 Write Before Read: 2.5:100 Write Before Fast Read: 15:100 The maximum frequency ratio between slave mode sck and pclk in 10K slave mode: Write: 34.2:76 Write Before Read: 1.9:76 Write Before Fast Read: 11.4:76
sck_o	Output	Serial clock output, with a maximum frequency of 50M
ss_o_n[7:0]	Output	Chip select output, active low

Item	Direction	Description
ss_i_n	Input	Chip select input, active low
miso_oe_n	Output	Master In Slave Out enable, active low
miso_i	Input	When signal miso_oe_n active low, miso_i in Master device used as input pin, and in Slave device used as output pin
miso_o	Output	When signal miso_oe_n active low, miso_o in Master device used as output pin, and in Slave device used as input pin
mosi_oe_n	Output	Master Out Slave In enable, active low
mosi_i	Input	When signal mosi_oe_n active low, mosi_i in Master device used as input pin, and in Slave device used as output pin
mosi_o	Output	When signal mosi_oe_n active low, mosi_i in Master device used as output pin, and in Slave device used as input pin
irq	Output	Interrupt request

Note: pclk is the APB interface clock CLK

3.3 Register

The SPI hard core communicates with the user interface through a set of control, command, status, and data registers, with the register names and their functions listed below.

Table 3-2 SPI Register List

Item	R/W	Address	Description
CTLR	R/W	00000	Control Register
IRQCTLR	R/W	00001	Interrupt Control Register
CMDR	R/W	00010	Command register
DATATR	R/W	00011	Data Transmit Registers
DATARR	R	00100	Data Receive Registers
DIVR	R/W	00101	Division register
STARTR	R/W	00110	Start register
STOPR	R/W	00111	Stop register
CSR	R/W	01000	Chip selection register
STATUSR	R	01001	Status register
IRQSTATUSR	R	01010	Interrupt Status Registers

3.3.1 Control Register

Table 3-3 SPI Control Register List

Bit	Item	Initial Value	Description
[7]	Reserved		
[6]	wakeup_en	1’b0	Wakeup enable Whether to send a wakeup request to the power controller when the control function module is selected as a slave device (chip select input is valid) 1: Yes 0: No

Bit	Item	Initial Value	Description
[5]	fastread	1’b0	Fast read enable 0: Normal Read 1: Fast read In the Write Before Read operation, for fast read, there is a padding byte between write and read
[4]	lsb_en	1’b0	Data transfer LSB enable 1: LSB 0: MSB
[3]	cpha	1’b0	Clock phase select 1: Send on the rising edge and receive on the falling edge 0: Send on the falling edge and receive on the rising edge
[2]	cpol	1’b0	Clock polarity select 1: Idle is 1 0: Idle is 0
[1]	mode	1’b0	Master/Slave select 1: Master device 0: Slave device
[0]	spi_en	1’b0	SPI interface enable 1: Enable 0: Disable

3.3.2 Interrupt Control Register

Table 3-4 SPI Interrupt Control Register List

Bit	Item	Initial Value	Description
[7:4]	Reserved		
[3]	over_en	1’b0	Operation completion interrupt enable 1: Enable 0: Disable
[2]	rdy_en	1’b0	Interface data valid interrupt enable 1: Enable 0: Disable
[1]	overrun_en	1’b0	Overflow interrupt enable 1: Enable 0: Disable
[0]	mode_en	1’b0	Mode interrupt enable 1: Enable 0: Disable

3.3.3 Command register

Table 3-5 SPI Command Register List

Bit	Item	Initial Value	Description
[7:3]	Reserved		
[2]	rw	1’b0	Read/Write control 0: Write 1: Read
[1]	m_eop	1’b0	Stop
[0]	m_sop	1’b0	Starting

3.3.4 Data Transmit Registers

Table 3-6 SPI Data Transmit Register List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	datat[7:0]	8’d0	Data transferred from the APB interface to the SPI interface

3.3.5 Data Receive Registers

Table 3-7 SPI Data Receive Register List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	datar[7:0]	8’d0	Data transferred from the SPI interface to the APB interface

3.3.6 Division register

Table 3-8 SPI Division Register List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	divr[7:0]	8’d24	Clock division factor, default to division by 50, sck_o is equal to pclk divided by 2(divr+1), with the minimum of division by 4, cannot configured to 2 (when divr[7:0] configured as 8’d0). 8’d1: Divide by 4 8’d2: Divide by 6 8’d3: Divide by 8 8’d4: Divide by 10 8’dn: Divide by 2(n+1)

3.3.7 Start register

Table 3-9 SPI Start Register List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	startr[7:0]	8’d0	Start delay

3.3.8 Stop register

Table 3-10 SPI Stop Register List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	stopr[7:0]	8’d0	Stop delay

3.3.9 Chip selection register

Table 3-11 SPI Chip Selection Register List

Bit	**Item**	**Initial Value**	**Description**
[7]	ss7_en	1’b0	Slave device 7 select 1: Select 0: Not select
[6]	ss6_en	1’b0	Slave device 6 select 1: Select 0: Not select
[5]	ss5_en	1’b0	Slave device 5 select 1: Select 0: Not select
[4]	ss4_en	1’b0	Slave device 4 select 1: Select 0: Not select
[3]	ss3_en	1’b0	Slave device 3 select 1: Select 0: Not select
[2]	ss2_en	1’b0	Slave device 2 select 1: Select 0: Not select
[1]	ss1_en	1’b0	Slave device 1 select 1: Select 0: Not select
[0]	ss0_en	1’b0	Slave device 0 select 1: Select 0: Not select

3.3.10 Status register

Table 3-12 SPI Status Register List

Bit	**Item**	**Description**
[7:2]	Reserved	
[1]	over	End of operation flag
[0]	rdy	Interface data valid flag

3.3.11 Interrupt Status Registers

Table 3-13 SPI Interrupt Status Register List

Bit	**Item**	**Description**
[7:4]	Reserved	
[3]	irq_over	Operation completion interrupt
[2]	irq_rdy	Interface data valid interrupt
[1]	irq_overrun	Overflow interrupt
[0]	irq_mode_err	Mode error interrupt

3.4 Interface timing

There are four modes for SPI. CPOL=0 indicates that the clock is low when at idle status, and high otherwise; CPHA=0 indicates the first edge of the clock signal is the sampling edge, otherwise the 2nd edge is the sampling edge.

3.4.1 CPOL=0 CPHA=0

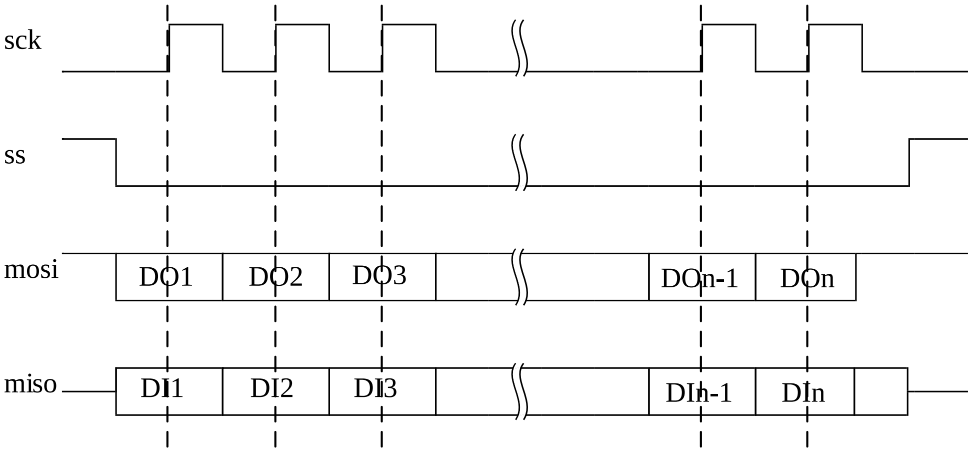

Figure 3-2 SPI Control Timing Diagram (CPOL=0, CPHA=0)

3.4.2 CPOL=0 CPHA=1

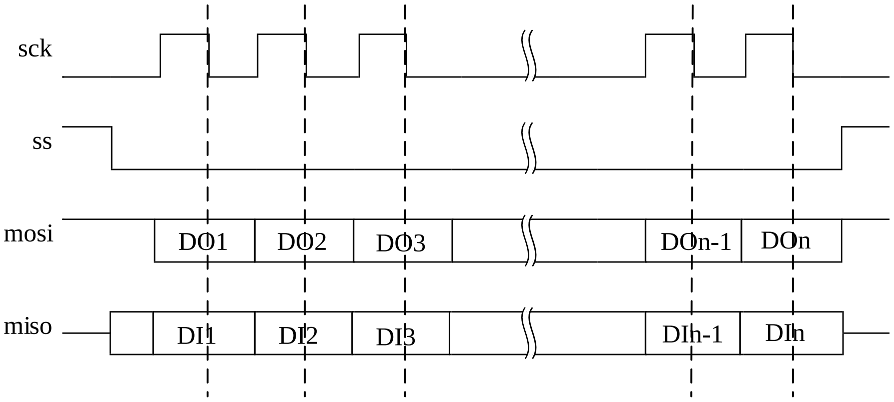

Figure 3-3 SPI Control Timing Diagram (CPOL=0, CPHA=1)

3.4.3 CPOL=1 CPHA=0

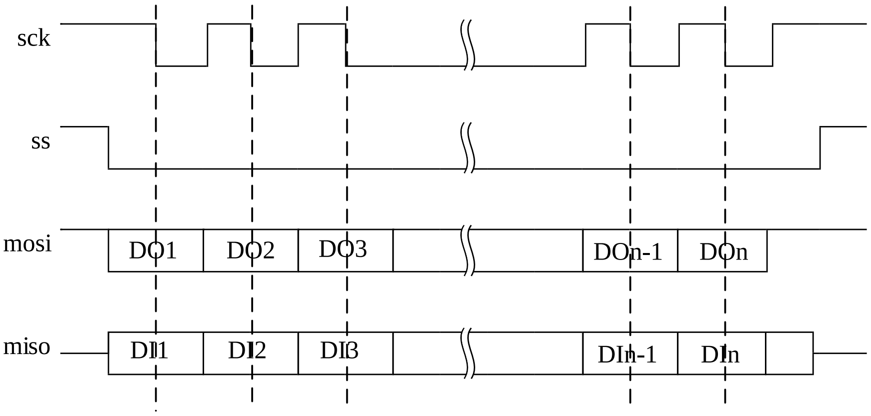

Figure 3-4 SPI Control Timing Diagram (CPOL=1, CPHA=0)

3.4.4 CPOL=1 CPHA=1

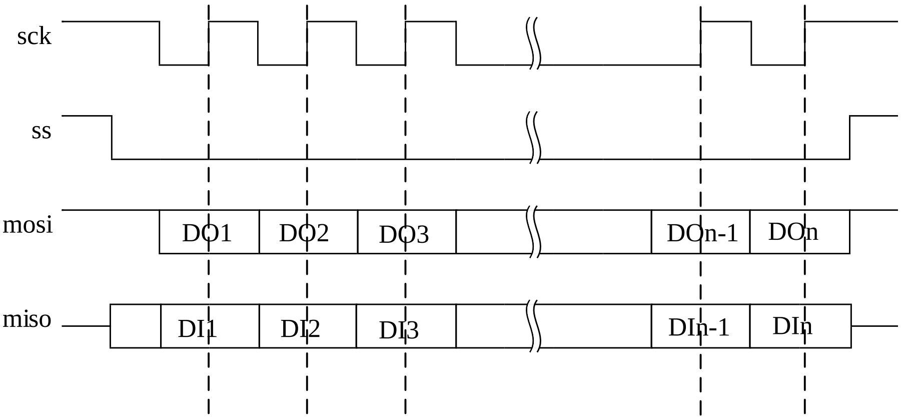

Figure 3-5 SPI Control Timing Diagram (CPOL=1, CPHA=1)

3.5 Operation Flow

During the operation, the status register can be continuously read for checking, or it can be checked again after receiving the interrupt signal irq.

3.5.1 Peer to Peer Mode

3.5.1.1 Master Device

Single Byte Write

Table 3-14 SPI Master Device Single-Byte Write Operation Process

Steps	**Operation Flow**
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, and start write operation
8	Write to data transmit register, and write byte
9	Write to command register, and clear start operation and stop operation
10	Read from status register to end detection
11	Write to command register, and clear stop operation

Multibyte Write

Table 3-15 SPI Master Device Multi-Byte Write Operation Process

Steps	**Operation Flow**
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, and start write operation
8	Write to data transmit register, and write byte 0
9	Write to command register, and clear start operation
10	Write to data transmit register, and write 1st byte
11	Write to data transmit register, and write 2nd byte
12	Write to data transmit register, and write 3rd byte
13	……
14	Write to data transmit register, and write nth byte
15	Write to command register, and stop operation
16	Read from status register to end detection
17	Write to command register, and clear stop operation

Single Byte Read

Table 3-16 SPI Master Device Single Byte Read Operation Process

Steps	Operation Flow
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, simultaneously start/stop read operation
8	Read bytes from data receive register
9	Write to command register, and clear start operation
10	Read from status register to end detection
11	Write to command register, and clear stop read operation

Multibyte Read

Table 3-17 SPI Master Device Multi-Byte Read Operation Process

Steps	Operation Flow
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, and start read operation
8	Read byte 0 from data receive register
9	Write to command register, and clear start operation
10	Read byte 1 from data receive register
11	Read byte 2 from data receive register
12	……
13	Read byte n-2 from data receive register
14	Read byte n-1 from data receive register
15	Write to command register, and stop operation
16	Read byte n from data receive register
17	Read from status register to end detection
18	Write to command register, and clear stop read operation

Single Byte Write before Read

Table 3-18 SPI Master Device Single Byte Write Before Read Operation Process

Steps	Operation Flow
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, start operation
8	Write to data transmit register, and write byte
9	Write to command register, and clear start operation
10	Read from status register, checking if the interface is ready
11	Once the interface is ready, write to command register to stop read operation
12	Read bytes from data receive register
13	Read from status register to end detection
14	Write to command register, and clear stop read operation

Single Byte Write and Multibyte Read

Table 3-19 SPI Master Device Single Byte Write and Multi-Byte Read Operation Process

Steps	Operation Flow
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, start operation
8	Write to data transmit register, and write byte
9	Write to command register, and clear start operation
10	Read from status register, checking if the interface is ready
11	Once the interface is ready, write to command register to read
12	Read byte 0 from data receive register
13	Read byte 1 from data receive register
14	Read byte 2 from data receive register
15	……
16	Read byte n-2 from data receive register
17	Read byte n-1 from data receive register
18	Write to command register, and stop operation
19	Read byte n from data receive register

Steps	Operation Flow
20	Read from status register to end detection
21	Write to command register, and clear stop read operation

Multibyte Write and Single Byte Read

Table 3-20 SPI Master Device Multi-Byte Write and Single-Byte Read Operation Process

Steps	Operation Flow
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, start operation
8	Write to data transmit register, and write byte 0
9	Write to command register, and clear start operation
10	Write to data transmit register, and write byte 1
11	Write to data transmit register, and write byte 2
12	Write to data transmit register, and write byte 3
13	……
14	Write to data transmit register, and write byte m
15	Read from status register, checking if the interface is ready
16	Once the interface is ready, write to command register to stop read operation
17	Read bytes from data receive register
18	Read from status register to end detection
19	Write to command register, and clear stop read operation

Multibyte Write Before Read

Table 3-21 SPI Master Device Multi-Byte Write Before Read Operation Process

Steps	Operation Flow
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, start operation
8	Write to data transmit register, and write byte 0
9	Write to command register, and clear start operation
10	Write to data transmit register, and write byte 1

Steps	**Operation Flow**
11	Write to data transmit register, and write byte 2
12	Write to data transmit register, and write byte 3
13	……
14	Write to data transmit register, and write byte m
15	Read from status register, checking if the interface is ready
16	Once the interface is ready, write to command register to read
17	Read byte 0 from data receive register
18	Read byte 1 from data receive register
19	Read byte 2 from data receive register
20	……
21	Read byte n-2 from data receive register
22	Read byte n-1 from data receive register
23	Write to command register, and stop operation
24	Read byte n from data receive register
25	Read from status register to end detection
26	Write to command register, and clear stop read operation

3.5.1.2 Slave Device

Write Operation

Table 3-22 SPI Slave Device Multi-Byte Write Operation Process

Steps	**Operation Flow**
1	Write to interrupt control register
2	Write to command register, and start write operation
3	Write to control register
4	Read from status register, checking if the interface is ready
5	Once the interface is ready, read byte 0 from the data receive register
6	Read from status register, checking if the interface is ready
7	Once the interface is ready, read byte 1 from the data receive register
8	……
9	Read from status register, checking if the interface is ready
10	Once the interface is ready, read byte n-1 from the data receive register
11	Read from status register, checking if the interface is ready
12	Once the interface is ready, read byte n from the data receive register
13	Read from status register to detect whether the operation ends

Read Operation

Table 3-23 SPI Slave Device Multi-Byte Read Operation Process

Steps	**Operation Flow**
1	Write to interrupt control register
2	Write to command register, and start write operation
3	Write to control register
4	Read from status register, checking if the interface is ready
5	Once the interface is ready, read byte 0 from the data receive register
6	Read from status register, checking if the interface is ready
7	Once the interface is ready, read byte 1 from the data receive register
8	……
9	Read from status register, checking if the interface is ready
10	Once the interface is ready, read byte m-1 from the data receive register
11	Read from status register, checking if the interface is ready
12	Once the interface is ready, read byte m from the data receive register
13	Write to command register, and start read operation
14	Write to data transmit register, and write byte 0
15	Read from status register, checking if the interface is ready
16	Once the interface is ready, write byte 1 to the data transmit register
17	Read from status register, checking if the interface is ready
18	Once the interface is ready, write byte 2 to the data transmit register
19	……
20	Read from status register, checking if the interface is ready
21	Once the interface is ready, write to the data transmit register, and write byte n-1
22	Read from status register, checking if the interface is ready
23	Once the interface is ready, write byte n to the data transmit register
24	Read from status register, checking if the interface is ready
25	Once the interface is ready, write byte n+1 to the data transmit register
26	Read from status register to detect whether the operation ends
27	Write 0 to control register

If there is data quantity information in the read operation, an additional padding byte must be sent at the end. If there is no data quantity information in the read operation, the last one or two bytes sent to the data transmit register will not be read.

3.5.2 Interrupt Mode

3.5.2.1 Master Device

Single Byte Write

Table 3-24 SPI Master Device Interrupt Mode Single-Byte Write Operation Process

Steps	**Operation Flow**
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, and start write operation
8	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
9	Write to data transmit register, and write byte
10	Write to the interrupt status register to clear the interface data valid interrupt
11	Write to command register, and clear start operation and stop operation
12	Upon receiving an interrupt, read from the interrupt status register to detect the operation completion interrupt
13	Write to the interrupt status register to clear the operation completion interrupt
14	Write to command register, and clear stop operation

Multibyte Write

Table 3-25 SPI Master Device Interrupt Mode Multi-Byte Write Operation Process

Steps	**Operation Flow**
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, and start write operation
8	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
9	Write to data transmit register, and write byte 1
10	Write to the interrupt status register to clear the interface data valid interrupt
11	Write to command register, and clear start operation
12	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
13	Write to data transmit register, and write byte 2
14	Write to the interrupt status register to clear the interface data valid interrupt

Steps	Operation Flow
15	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
16	Write to data transmit register, and write byte 3
17	Write to the interrupt status register to clear the interface data valid interrupt
18	……
19	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
20	Write to data transmit register, and write byte n-1
21	Write to the interrupt status register to clear the interface data valid interrupt
22	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
23	Write to data transmit register, and write byte n
24	Write to the interrupt status register to clear the interface data valid interrupt
25	Write to command register, and stop operation
26	Upon receiving an interrupt, read from the interrupt status register to detect the operation completion interrupt
27	Write to the interrupt status register to clear the operation completion interrupt
28	Write to command register, and clear stop operation

Single Byte Read

Table 3-26 SPI Master Device Interrupt Mode Single-Byte Read Operation Process

Steps	Operation Flow
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, simultaneously start/stop read operation
8	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
9	Read bytes from data receive register
10	Write to the interrupt status register to clear the interface data valid interrupt
11	Write to command register, and clear start operation
12	Upon receiving an interrupt, read from the interrupt status register to detect the operation completion interrupt
13	Write to the interrupt status register to clear the operation completion interrupt
14	Write to command register, and clear stop read operation

Multibyte Read

Table 3-27 SPI Master Device Interrupt Mode Multi-Byte Read Operation Process

Steps	Operation Flow
1	Write to start register

Steps	Operation Flow
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, and start read operation
8	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
9	Read byte 1 from data receive register
10	Write to the interrupt status register to clear the interface data valid interrupt
11	Write to command register, and clear start operation
12	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
13	Read byte 2 from data receive register
14	Write to the interrupt status register to clear the interface data valid interrupt
15	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
16	Read byte 3 from data receive register
17	Write to the interrupt status register to clear the interface data valid interrupt
18	……
19	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
20	Read byte n-2 from data receive register
21	Write to the interrupt status register to clear the interface data valid interrupt
22	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
23	Read byte n-1 from data receive register
24	Write to the interrupt status register to clear the interface data valid interrupt
25	Write to command register, and stop operation
26	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
27	Read byte n from data receive register
28	Write to the interrupt status register to clear the interface data valid interrupt
29	Upon receiving an interrupt, read from the interrupt status register to detect the operation completion interrupt
30	Write to the interrupt status register to clear the operation completion interrupt
31	Write to command register, and clear stop read operation

Single Byte Write Before Read

Table 3-28 SPI Master Device Interrupt Mode Single-Byte Write Before Read Operation Process

Steps	Operation Flow
1	Write to start register
2	Write to stop register
3	Write to division register

Steps	Operation Flow
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, and start write operation
8	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
9	Write to data transmit register, and write byte
10	Write to the interrupt status register to clear the interface data valid interrupt
11	Write to command register, and clear start operation
12	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
13	Write to the command register to stop the read operation
14	Write to the interrupt status register to clear the interface data valid interrupt
15	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
16	Read bytes from data receive register
17	Write to the interrupt status register to clear the interface data valid interrupt
18	Upon receiving an interrupt, read from the interrupt status register to detect the operation completion interrupt
19	Write to the interrupt status register to clear the operation completion interrupt
20	Write to command register, and clear stop read operation

Single Byte Write and Multibyte Read

Table 3-29 SPI Master Device Interrupt Mode Single Byte Write and Multi-Byte Read Operation Process

Steps	Operation Flow
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, and start write operation
8	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
9	Write to data transmit register, and write byte
10	Write to the interrupt status register to clear the interface data valid interrupt
11	Write to command register, and clear start operation
12	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
13	Write to command register, and start read operation
14	Write to the interrupt status register to clear the interface data valid interrupt
15	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
16	Read byte 1 from data receive register

Steps	Operation Flow
17	Write to the interrupt status register to clear the interface data valid interrupt
18	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
19	Read byte 2 from data receive register
20	Write to the interrupt status register to clear the interface data valid interrupt
21	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
22	Read byte 3 from data receive register
23	Write to the interrupt status register to clear the interface data valid interrupt
24	……
25	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
26	Read byte n-2 from data receive register
27	Write to the interrupt status register to clear the interface data valid interrupt
28	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
29	Read byte n-1 from data receive register
30	Write to the interrupt status register to clear the interface data valid interrupt
31	Write to command register, and stop operation
32	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
33	Read byte n from data receive register
34	Write to the interrupt status register to clear the interface data valid interrupt
35	Upon receiving an interrupt, read from the interrupt status register to detect the operation completion interrupt
36	Write to the interrupt status register to clear the operation completion interrupt
37	Write to command register, and clear stop read operation

Multibyte Write and Single Byte Read

Table 3-30 SPI Master Device Interrupt Mode Multi-Byte Write and Single Byte Read Operation Process

Steps	Operation Flow
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register
7	Write to command register, and start write operation
8	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
9	Write to data transmit register, and write byte 1
10	Write to the interrupt status register to clear the interface data valid interrupt

Steps	Operation Flow
11	Write to command register, and clear start operation
12	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
13	Write to data transmit register, and write byte 2
14	Write to the interrupt status register to clear the interface data valid interrupt
15	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
16	Write to data transmit register, and write byte 3
17	Write to the interrupt status register to clear the interface data valid interrupt
18	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
19	Write to data transmit register, and write byte 4
20	Write to the interrupt status register to clear the interface data valid interrupt
21	……
22	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
23	Write to data transmit register, and write byte m-1
24	Write to the interrupt status register to clear the interface data valid interrupt
25	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
26	Write to data transmit register, and write byte m
27	Write to the interrupt status register to clear the interface data valid interrupt
28	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
29	Write to the command register to stop the read operation
30	Write to the interrupt status register to clear the interface data valid interrupt
31	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
32	Read bytes from data receive register
33	Write to the interrupt status register to clear the interface data valid interrupt
34	Upon receiving an interrupt, read from the interrupt status register to detect the operation completion interrupt
35	Write to the interrupt status register to clear the operation completion interrupt
36	Write to command register, and clear stop read operation

Multibyte Write Before Read

Table 3-31 SPI Master Device Interrupt Mode Multi-Byte Write Before Read Operation Process

Steps	Operation Flow
1	Write to start register
2	Write to stop register
3	Write to division register
4	Write to chip selection register
5	Write to interrupt control register
6	Write to control register

Steps	Operation Flow
7	Write to command register, and start write operation
8	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
9	Write to data transmit register, and write byte 1
10	Write to the interrupt status register to clear the interface data valid interrupt
11	Write to command register, and clear start operation
12	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
13	Write to data transmit register, and write byte 2
14	Write to the interrupt status register to clear the interface data valid interrupt
15	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
16	Write to data transmit register, and write byte 3
17	Write to the interrupt status register to clear the interface data valid interrupt
18	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
19	Write to data transmit register, and write byte 4
20	Write to the interrupt status register to clear the interface data valid interrupt
21	……
22	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
23	Write to data transmit register, and write byte m-1
24	Write to the interrupt status register to clear the interface data valid interrupt
25	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
26	Write to data transmit register, and write byte m
27	Write to the interrupt status register to clear the interface data valid interrupt
28	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
29	Write to command register, and start read operation
30	Write to the interrupt status register to clear the interface data valid interrupt
31	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
32	Read byte 1 from data receive register
33	Write to the interrupt status register to clear the interface data valid interrupt
34	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
35	Read byte 2 from data receive register
36	Write to the interrupt status register to clear the interface data valid interrupt
37	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
38	Read byte 3 from data receive register
39	Write to the interrupt status register to clear the interface data valid interrupt
40	……
41	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
42	Read byte n-2 from data receive register

Steps	Operation Flow
43	Write to the interrupt status register to clear the interface data valid interrupt
44	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
45	Read byte n-1 from data receive register
46	Write to the interrupt status register to clear the interface data valid interrupt
47	Write to command register, and stop operation
48	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
49	Read byte n from data receive register
50	Write to the interrupt status register to clear the interface data valid interrupt
51	Upon receiving an interrupt, read from the interrupt status register to detect the operation completion interrupt
52	Write to the interrupt status register to clear the operation completion interrupt
53	Write to command register, and clear stop read operation

3.5.2.2 Slave Device

Write Operation

Table 3-32 SPI Slave Device Interrupt Mode Write Operation Process

Steps	Operation Flow
1	Write to interrupt control register
2	Write to command register, and start write operation
3	Write to control register
4	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
5	Write to the interrupt status register to clear the interface data valid interrupt
6	Read byte 1 from data receive register
7	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
8	Write to the interrupt status register to clear the interface data valid interrupt
9	Read byte 2 from data receive register
10	……
11	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
12	Write to the interrupt status register to clear the interface data valid interrupt
13	Read byte n-1 from data receive register
14	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
15	Write to the interrupt status register to clear the interface data valid interrupt
16	Read byte n from data receive register
17	Upon receiving an interrupt, read from the interrupt status register to detect the operation completion interrupt
18	Write to the interrupt status register to clear the operation completion interrupt

Read Operation

Table 3-33 SPI Slave Device Interrupt Mode Multi-Byte Read Operation Process

Steps	Operation Flow
1	Write to interrupt control register
2	Write to command register, and start write operation
3	Write to control register
4	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
5	Write to the interrupt status register to clear the interface data valid interrupt
6	Read byte 1 from data receive register
7	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
8	Write to the interrupt status register to clear the interface data valid interrupt
9	Read byte 2 from data receive register
10	……
11	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
12	Write to the interrupt status register to clear the interface data valid interrupt
13	Read byte m-1 from data receive register
14	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
15	Write to the interrupt status register to clear the interface data valid interrupt
16	Read byte m from data receive register
17	Write to command register, and start read operation
18	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
19	Write to the interrupt status register to clear the interface data valid interrupt
20	Write to data transmit register, and write byte 1
21	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
22	Write to the interrupt status register to clear the interface data valid interrupt
23	Write to data transmit register, and write byte 2
24	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
25	Write to the interrupt status register to clear the interface data valid interrupt
26	Write to data transmit register, and write byte 3
27	……
28	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
29	Write to the interrupt status register to clear the interface data valid interrupt
30	Write to data transmit register, and write byte n-1
31	Upon receiving an interrupt, read from the interrupt status register to detect the interface data valid interrupt
32	Write to the interrupt status register to clear the interface data valid interrupt
33	Write to data transmit register, and write byte n
34	Upon receiving an interrupt, read from the interrupt status register to detect the operation completion interrupt

Steps	Operation Flow
35	Write to the interrupt status register to clear the operation completion interrupt
36	Write 0 to control register

If there is data quantity information in the read operation, an additional padding byte must be sent at the end. If there is no data quantity information in the read operation, the last one or two bytes sent to the data transmit register will not be read.

Chapter 4 **I^{2}C Hard Core**

I^{2}C is a widely used two-wire serial bus, commonly used for communication between devices on the same board. Each CPLD device includes two identical I^{2}C hard cores. Either of these hard cores can operate as an I^{2}C master or I^{2}C slave, and neither has pre-assigned I/O pins, but needs to be allocated to general I/Os.

4.1 Features

- 8-bit slave APB interface, compatible with AMBA APB3 protocol, with 1K/2K/4K/7K clock frequency up to 100MHz, and 10K clock frequency up to 76MHz
- Fast/Standard Mode I^{2}C bus protocol, with up to 400kHz data transfer rate for 1K/2K/4K/7K, and up to 300kHz data transfer rate for 10K
- Configurable as master or slave device
- Synchronization
- Arbitration
- Clock stretch
- 7-bit/10-bit addressing
- All call addressing
- Soft reset
- Start Byte
- Device ID
- Interrupt

4.2 I^{2}C Primitive

When using I^{2}C hard cores, the user must instantiate the corresponding GTP_I2C primitive, which needs to be used in conjunction with GTP_APB. The relevant information for GTP_I2C is described as below.

```
GTP_I2C #(
    .I2C_NUM      (0              )     // 0    1 available
) U_GTP_I2C (
.SCL_I              (SCL_I      ),
.SCL_O              (SCL_O      ),
.SDA_I              (SDA_I      ),
.SDA_O              (SDA_O      ),
.IRQ                (IRQ       )
);
```

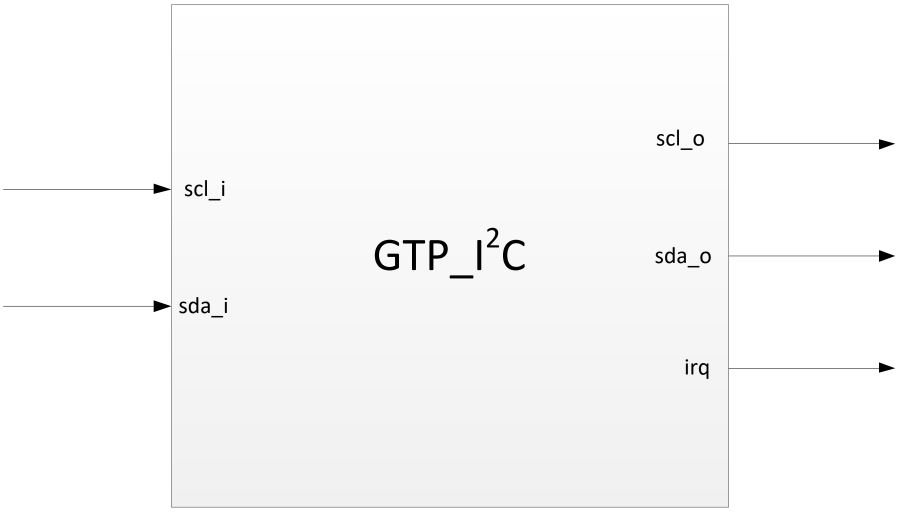

Figure 4-1 GTP_I2C Module Signal Input/Output Diagram

Table 4-1 GTP_I2C Module Signal List

Item	**Direction**	**Description**
scl_i	Input	Serial clock input, with a maximum frequency of 400K In slave mode, the minimum frequency ratio of pclk to scl is 25:1. For an scl of 400K, the minimum pclk frequency is 10M.
scl_o	Output	Serial clock output, with a maximum frequency of 400K
sda_i	Input	Serial data input
sda_o	Output	Serial data output
irq	Output	Interrupt request

Table 4-2 GTP_I2C Module Parameter List

Parameter Name	**Parameter Type**	**Valid Values**	**Defaults**	**Function Description**
I2C_NUM	Integer	0, 1	0	I2C hard core number, including two cores

4.3 Register Description

Table 4-3 I^{2}C Module Register Description List

Item	Read/write	Address	Description
CTLR	R/W	00000	Control Register
IRQCTLR	R/W	00001	Interrupt Control Register
CMDR	R/W	00010	Command register
ADR	R/W	00011	Address register
ADR10	R/W	00100	10-bit addressing address register
DATATR	R/W	00101	Data Transmit Registers
DATARR	R/W	00110	Data Receive Registers
STATUSR	R	00111	Status register
SCLLR0	R/W	01000	Clock low-level register 0
SCLLR1	R/W	01001	Clock low-level register 1
SCLHR0	R/W	01010	Clock high-level register 0
SCLHR1	R/W	01011	Clock high-level register 1
STARTR	R/W	01100	Start register
RSTARTR	R/W	01101	Restart register
STOPR	R/W	01110	Stop register
IRQSTATUSR	R	10000	Interrupt Status Registers
STR0	R/W	10001	Clock stretch register 0
STR1	R/W	10010	Clock stretch register 1
DLYR0	R/W	10011	Delay register 0
DLYR1	R/W	10100	Delay register 1

4.3.1 Control Register

Table 4-4 I^{2}C Control Register List

Bit	Item	Initial Value	Description
[7:5]	Reserved		
[4]	wakeup_en	1’b0	Wakeup enable Whether to send a wakeup request to the power controller when the control function module is selected as a slave device (when slave device address matched) 1: Yes 0: No
[3]	scl_str	1’b0	Clock stretch enable 1: Enabled 0: Disabled
[2]	s_gc	1’b0	All call enable 1: Enabled 0: Disabled
[1]	m_i2c	1’b0	Master device interface enable 1: Enabled 0: Disabled

Bit	Item	Initial Value	Description
[0]	s_i2c	1'b0	Slave device interface enable 1: Enabled 0: Disabled

4.3.2 Interrupt Control Register

Table 4-5 I^{2}C Interrupt Control Register List

Bit	Item	Initial Value	Description
[7:4]	Reserved		
[3]	rdy_en	1'b0	Bus idle interrupt enable 1: Enabled 0: Disabled
[2]	arb_lost_en	1'b0	Lost arbitration interrupt enable 1: Enabled 0: Disabled
[1]	overrun_en	1'b0	Overflow interrupt enable 1: Enabled 0: Disabled
[0]	m_wack_en	1'b0	No acknowledge interrupt enable 1: Enabled 0: Disabled

4.3.3 Command register

Table 4-6 I^{2}C Command Register List

Bit	Item	Initial Value	Description
[7:3]	Reserved		
[2]	m_ack	1'b0	Acknowledge 0: Acknowledge 1: No Acknowledge
[1]	m_eop	1'b0	Stop
[0]	m_sop	1'b0	Start

4.3.4 Address register

Table 4-7 I^{2}C Address Register List

Bit	Item	Initial Value	Description
[7]	Reserved		
[6:0]	addr[6:0]	7'd0	Slave device 7-bit address

4.3.5 10-bit addressing address register

Table 4-8 I^2C 10-Bit Addressing Address Register

Bit	**Item**	**Initial Value**	**Description**
[7:3]	Reserved		
[2:0]	addr[9:7]	3’d0	The highest three bits of slave device 10-bit addressing address

4.3.6 Data Transmit Registers

Table 4-9 I^2C Data Transmit Register List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	DATATR		Data transferred from the APB bus to the I^2C bus

4.3.7 Data Receive Registers

Table 4-10 I^2C Data Receive Register List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	DATARR		Data transferred from the I^2C bus to the APB bus

4.3.8 Status register

Table 4-11 I^2C Status Register List

Bit	**Item**	**Description**
[7:5]	Reserved	
[4]	id	Read device identification operation indicator
[3]	gc	All call operation indicator
[2]	m_wack	Master device write operation acknowledge indicator 0: Acknowledge 1: No Acknowledge
[1]	rdy	Bus idle indicator 0: Busy 1: Idle
[0]	rw	Read/Write operation indicator 0: Current operation is write 1: Current operation is read

4.3.9 Clock Low-Level Register 0

Table 4-12 I^{2}C Clock Low-Level Register 0 List

Bit	Item	Initial Value	Description
[7:0]		8‘d130	Low 8 bits of the clock low-level register, Control the number of pclk cycles for scl low-level duration, Clock low-level register cannot be configured to 0, Number of pclk cycles for scl low-level duration = clock low-level register value + 4

4.3.10 Clock low-level register 1

Table 4-13 I^{2}C Clock Low-Level Register 1 List

Bit	Item	Initial Value	Description
[7:0]		8‘d0	High 8 bits of the clock low-level register, Control the number of pclk cycles for scl low-level duration, Clock low-level register cannot be configured to 0, Number of pclk cycles for scl low-level duration = clock low-level register value + 4

4.3.11 Clock High-Level Register 0

Table 4-14 I^{2}C Clock High-Level Register 0 List

Bit	Item	Initial Value	Description
[7:0]		8‘d60	Low 8 bits of the clock high-level register, Control the number of pclk cycles for scl high-level duration, Clock high-level register cannot be configured to 0, Number of pclk cycles for scl high-level duration = clock high-level register value + 4

4.3.12 Clock High-Level Register 1

Table 4-15 I^{2}C Clock High-Level Register 1 List

Bit	Item	Initial Value	Description
[7:0]		8‘d0	High 8 bits of the clock high-level register, Control the number of pclk cycles for scl high-level duration, Clock high-level register cannot be configured to 0, Number of pclk cycles for scl high-level duration = clock high-level register value + 4

4.3.13 Clock Stretch Register 0

Table 4-16 I^{2}C Clock Stretch Register 0 List

Bit	Item	Initial Value	Description
[7:0]		8‘d130	Low 8 bits of the clock stretch register, Control the number of pclk cycles for scl low-level duration after transfer can continuation, During clock stretch, the setup time of sda_o relative to scl_i rising edge is approximately (clock stretch registers - delay registers) pclk cycles

4.3.14 Clock stretch register 1

Table 4-17 I^{2}C Clock Stretch Register 1 List

Bit	Item	Initial Value	Description
[7:0]		8‘d0	High 8 bits of the clock stretch register, Control the number of pclk cycles for scl low-level duration after transfer continuation, During clock stretch, the setup time of sda_o relative to scl_i rising edge is approximately (clock stretch registers - delay registers) pclk cycles

4.3.15 Delay register 0

Table 4-18 I^{2}C Delay Register 0 List

Bit	Item	Initial Value	Description
[7:0]		8‘d40	Low 8 bits of the delay register, Control the number of pclk cycles for sdo_o delay relative to scl_i/scl_o, When the Function Block acts as a master device, sda_o delays by dly[8:0] pclk cycles relative to the scl_o falling edge, Function block acts as a slave device: When sda_o is for address acknowledge, it delays by dly[8:0]+4 or dly[8:0]+5 pclk cycles relative to scl_i falling edge, When sda_o is for data acknowledge, it delays by dly[8:0]+9 pclk cycles relative to scl_i falling edge, When sda_o is for data, it delays by dly[8:0]+4 pclk cycles relative to scl_i falling edge

4.3.16 Delay register 1

Table 4-19 List of I2C Delay Register 0

Bit	Item	Initial Value	Description
[7:1]	Reserved		
[0]	dly[8]	1‘b0	highest bit of the delay register, Control the number of pclk cycles for sdo_o delay relative to scl_i/scl_o, When the Function Block acts as a master device, sda_o delays

Bit	Item	Initial Value	Description
			by dly[8:0] pclk cycles relative to the scl_o falling edge, Function block acts as a slave device: When sda_o is for address acknowledge, it delays by dly[8:0]+4 or dly[8:0]+5 pclk cycles relative to scl_i falling edge, When sda_o is for data acknowledge, it delays by dly[8:0]+9 pclk cycles relative to scl_i falling edge, When sda_o is for data, it delays by dly[8:0]+4 pclk cycles relative to scl_i falling edge

4.3.17 Start register

Table 4-20 I^{2}C Start Register List

Bit	Item	Initial Value	Description
[7:0]	num_start	8‘d0	Control the number of pclk cycles from sda falling edge to scl falling edge upon start: num_start * 64

4.3.18 Restart register

Table 4-21 I^{2}C Re-Start Register List

Bit	Item	Initial Value	Description
[7:0]	num_rstart	8‘d0	Control the number of pclk cycles from sda falling edge to scl falling edge upon restart: num_rstart * 64

4.3.19 Stop register

Table 4-22 I^{2}C Stop Register List

Bit	Item	Initial Value	Description
[7:0]	num_stop	8‘d0	Control the number of pclk cycles from scl rising edge to sda rising edge upon stop: num_stop * 64

4.3.20 Interrupt Status Registers

Table 4-23 I2C Interrupt Status Register List

Bit	Item	Description
[7:5]	Reserved	
[4]	irq_m_wack	No acknowledge interrupt
[3]	irq_overw	Write full interrupt
[2]	irq_overr	Read empty interrupt
[1]	irq_arb_lost	Lost arbitration interrupt
[0]	irq_rdy	Bus idle interrupt

4.4 Interface timing

I^{2}C interface write and read timing diagrams are shown as below, with the I^{2}C write timing diagram on the left and the I^{2}C read timing diagram on the right.

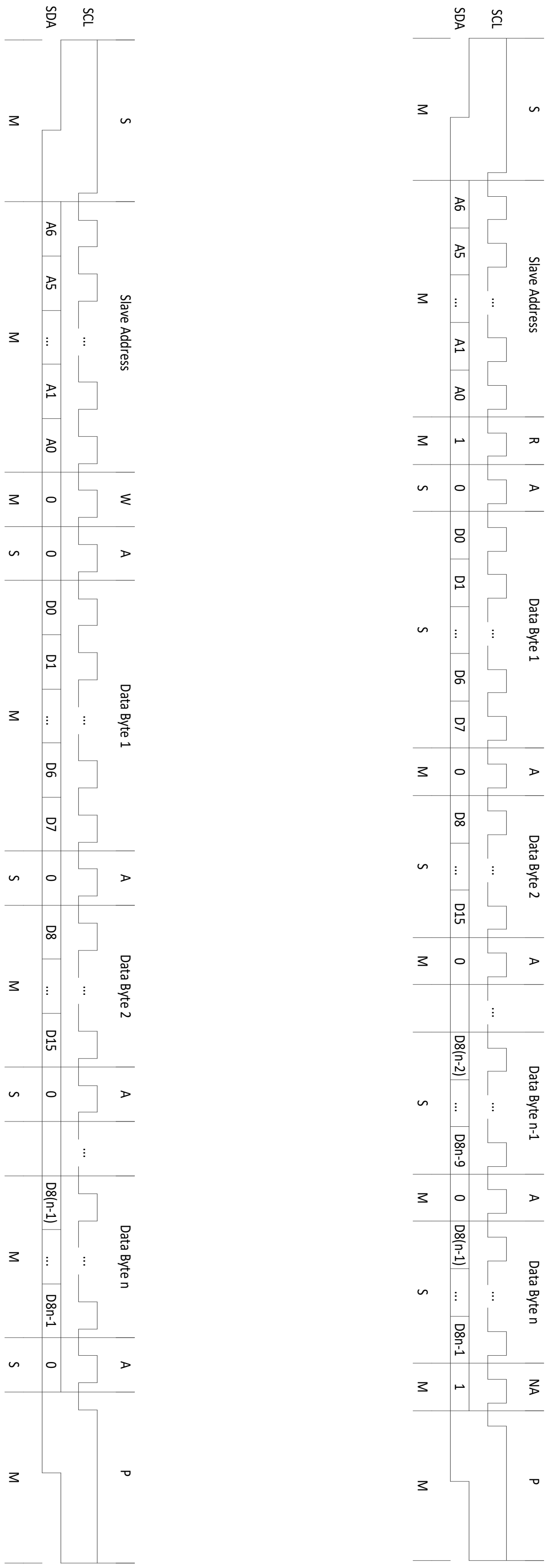

Figure 4-2 I^{2}C Write/Read Operation Timing Diagram

4.5 Operation Flow

4.5.1 Peer to Peer Mode

4.5.1.1 Master Device

Write

Table 4-24 I^2C Point-to-Point Mode Master Device Write Operation Process

Steps	**Operation Flow**
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending address and write flag
13	Write to command register, and clear start
14	Write to data transmit register, for sending the 1st byte of data
15	Write to data transmit register for sending the 2nd byte of data
16	……
17	Write to data transmit register for sending the nth byte of data
18	Read from status register to detect bus idleness
19	Write to command register, and stop
20	Read from status register to detect bus idleness
21	Write to command register, and clear stop

Read

Table 4-25 I^2C Point-to-Point Mode Master Device Read Operation Process

Steps	**Operation Flow**
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register

Steps	Operation Flow
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending address and read flag
13	Write to command register, and clear start
14	Read the 1st byte from the data receive register
15	Read the 2nd byte from the data receive register
16	Read the 3rd byte from the data receive register
17	……
18	Read the (0-2)th byte from the data receive register
19	Read the (0-1)th byte from the data receive register
20	Write to command register, no acknowledge
21	Read the nth byte from the data receive register
22	Write to the command register, to stop and clear no acknowledge
23	Read from status register to detect bus idleness
24	Write to command register, and clear stop

Repeat Write

Table 4-26 I^{2}C Point-to-Point Mode Master Device Repeat Write Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending address and write flag
13	Write to command register, and clear start
14	Write to data transmit register, for sending the 1st byte of data
15	Write to data transmit register for sending the 2nd byte of data
16	……
17	Write to data transmit register for sending the n1th byte of data
18	Read from status register to detect bus idleness

Steps	Operation Flow
19	Write to command register, start
20	Write to data transmit register for sending address and write flag
21	Write to command register, and clear start
22	Write to data transmit register, for sending the 1st byte of data
23	Write to data transmit register for sending the 2nd byte of data
24	……
25	Write to data transmit register for sending the n2th byte of data
26	……
27	Read from status register to detect bus idleness
28	Write to command register, start
29	Write to data transmit register for sending address and write flag
30	Write to command register, and clear start
31	Write to data transmit register, for sending the 1st byte of data
32	Write to data transmit register for sending the 2nd byte of data
33	……
34	Write to data transmit register for sending the nkth byte of data
35	Read from status register to detect bus idleness
36	Write to command register, and stop
37	Read from status register to detect bus idleness
38	Write to command register, and clear stop

Repeat Read

Table 4-27 I^2C Point-to-Point Mode Master Device Repeat Read Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending address and read flag
13	Write to command register, and clear start
14	Read the 1st byte from the data receive register
15	Read the 2nd byte from the data receive register

Steps	Operation Flow
16	Read the 3rd byte from the data receive register
17	……
18	Read the (n1-2)th byte of data from the data receive register
19	Read the (n1-1)th byte of data from the data receive register
20	Write to command register, no acknowledge
21	Read the n1th byte of data from the data receive register
22	Write to the command register, to start and clear no acknowledge
23	Write to data transmit register for sending address and read flag
24	Write to command register, and clear start
25	Read the 1st byte from the data receive register
26	Read the 2nd byte from the data receive register
27	Read the 3rd byte from the data receive register
28	……
29	Read the (n2-2)th byte of data from the data receive register
30	Read the (n2-1)th byte of data from the data receive register
31	Write to command register, no acknowledge
32	Read the n2th byte of data from the data receive register
33	……
34	Write to the command register, to start and clear no acknowledge
35	Write to data transmit register for sending address and read flag
36	Write to command register, and clear start
37	Read the 1st byte from the data receive register
38	Read the 2nd byte from the data receive register
39	Read the 3rd byte from the data receive register
40	……
41	Read the (nk-2)th byte of data from the data receive register
42	Read the (nk-1)th byte of data from the data receive register
43	Write to command register, no acknowledge
44	Read the nkth byte of data from the data receive register
45	Write to the command register, to stop and clear no acknowledge
46	Read from status register to detect bus idleness
47	Write to command register, and clear stop

Write before read

Table 4-28 I^{2}C Point-to-Point Mode Master Device Write-Before-Read Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0

Steps	Operation Flow
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending address and write flag
13	Write to command register, and clear start
14	Write to data transmit register, for sending the 1st byte of data
15	Write to data transmit register for sending the 2nd byte of data
16	Write to data transmit register for sending the 3rd byte of data
17	……
18	Write to data transmit register for sending the mth byte of data
19	Read from status register to detect bus idleness
20	Write to command register, start
21	Write to data transmit register for sending address and read flag
22	Write to command register, and clear start
23	Read the 1st byte from the data receive register
24	Read the 2nd byte from the data receive register
25	Read the 3rd byte from the data receive register
26	……
27	Read the (0-2)th byte from the data receive register
28	Read the (0-1)th byte from the data receive register
29	Write to command register, no acknowledge
30	Read the nth byte from the data receive register
31	Write to the command register, to stop and clear no acknowledge
32	Read from status register to detect bus idleness
33	Write to command register, and clear stop

Read before write

Table 4-29 I^{2}C Point-to-Point Mode Master Device Read-Before-Write Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register

Steps	Operation Flow
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending address and read flag
13	Write to command register, and clear start
14	Read the 1st byte from the data receive register
15	Read the 2nd byte from the data receive register
16	Read the 3rd byte from the data receive register
17	……
18	Read the (m-2)th byte of data from the data receive register
19	Read the (m-1)th byte of data from the data receive register
20	Write to command register, no acknowledge
21	Read the mth byte of data from the data receive register
22	Write to the command register, to start and clear no acknowledge
23	Write to data transmit register for sending address and write flag
24	Write to command register, and clear start
25	Write to data transmit register, for sending the 1st byte of data
26	Write to data transmit register for sending the 2nd byte of data
27	……
28	Write to data transmit register for sending the nth byte of data
29	Read from status register to detect bus idleness
30	Write to command register, and stop
31	Read from status register to detect bus idleness
32	Write to command register, and clear stop

Soft Reset

Table 4-30 I^2C Point-to-Point Mode Master Device Soft Reset Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0

9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending all-call address and write flag
13	Write to command register, and clear start
14	Write to data transmit register for sending byte 0x06
15	Read from status register to detect bus idleness
16	Write to command register, and stop
17	Read from status register to detect bus idleness
18	Write to command register, and clear stop

Hardware Programming

Table 4-31 I^2C Point-to-Point Mode Master Device Hardware Programming Operation Process

Steps	**Operation Flow**
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending all-call address and write flag
13	Write to command register, and clear start
14	Write to data transmit register for sending byte 0x04
15	Read from status register to detect bus idleness
16	Write to command register, and stop
17	Read from status register to detect bus idleness
18	Write to command register, and clear stop

Hardware All Call

Table 4-32 I^2C Point-to-Point Mode Master Device Hardware All Call Operation Process

Steps	**Operation Flow**
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1

Steps	Operation Flow
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending all-call address and write flag
13	Write to command register, and clear start
14	Write to data transmit register, for sending the master address and bit 1
15	Write to data transmit register, for sending the 1st byte of data
16	Write to data transmit register for sending the 2nd byte of data
17	……
18	Write to data transmit register for sending the nth byte of data
19	Read from status register to detect bus idleness
20	Write to command register, and stop
21	Read from status register to detect bus idleness
22	Write to command register, and clear stop

Start Byte

Table 4-33 I^2C Point-to-Point Mode Master Device Start Byte Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to the data transmit register, for sending the start byte
13	Write to command register, and clear start
14	Read from status register to detect no acknowledge
15	Write to command register, start
16	Write to data transmit register for sending address and write/read flag
17	Write to command register, and clear start

Read device identification

Table 4-34 I^2C Point-to-Point Mode Master Device Read Device Identification Operation Process

Steps	**Operation Flow**
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending the device identification address and write flag
13	Write to command register, and clear start
14	Write to data transmit register, for sending address and a padding bit
15	Read from status register to detect bus idleness
16	Write to command register, start
17	Write to data transmit register for sending device identification address and read flag
18	Write to command register, and clear start
19	Read the 1st byte of device identification from the data receive register
20	Read the 2nd byte of device identification from the data receive register
21	Write to command register, no acknowledge
22	Read the 3rd byte of device identification from the data receive register
23	Write to the command register, to stop and clear no acknowledge
24	Read from status register to detect bus idleness
25	Write to command register, and clear stop

10-Bit Addressing Write

Table 4-35 I^2C Point-to-Point Mode Master Device 10-Bit Addressing Write Operation Process

Steps	**Operation Flow**
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0

Steps	Operation Flow
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to the data transmit register for sending the first 7 bits of the address and the write flag
13	Write to command register, and clear start
14	Write to the data transmit register for sending the 2nd byte of the address
15	Write to data transmit register, for sending the 1st byte of data
16	Write to data transmit register for sending the 2nd byte of data
17	……
18	Write to data transmit register for sending the nth byte of data
19	Read from status register to detect bus idleness
20	Write to command register, and stop
21	Read from status register to detect bus idleness
22	Write to command register, and clear stop

10-Bit Addressing Read

Table 4-36 I^{2}C Point-to-Point Mode Master Device 10-Bit Addressing Read Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to the data transmit register for sending the first 7 bits of the address and the write flag
13	Write to command register, and clear start
14	Write to the data transmit register for sending the 2nd byte of the address
15	Read from status register to detect bus idleness
16	Write to command register, start
17	Write to the data transmit register for sending the first 7 bits of the address and the read flag
18	Write to command register, and clear start
19	Read the 1st byte from the data receive register
20	Read the 2nd byte from the data receive register
21	Read the 3rd byte from the data receive register

Steps	Operation Flow
22	……
23	Read the (0-2)th byte from the data receive register
24	Read the (0-1)th byte from the data receive register
25	Write to command register, no acknowledge
26	Read the nth byte from the data receive register
27	Write to the command register, to stop and clear no acknowledge
28	Read from status register to detect bus idleness
29	Write to command register, and clear stop

10-Bit Addressing Repeat Write

Table 4-37 I^{2}C Point-to-Point Mode Master Device 10-Bit Addressing Repeat Write Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to the data transmit register for sending the first 7 bits of the address and the write flag
13	Write to command register, and clear start
14	Write to the data transmit register for sending the 2nd byte of the address
15	Write to data transmit register, for sending the 1st byte of data
16	Write to data transmit register for sending the 2nd byte of data
17	……
18	Write to data transmit register for sending the n1th byte of data
19	Read from status register to detect bus idleness
20	Write to command register, start
21	Write to the data transmit register for sending the first 7 bits of the address and the write flag
22	Write to command register, and clear start
23	Write to the data transmit register for sending the 2nd byte of the address
24	Write to data transmit register, for sending the 1st byte of data
25	Write to data transmit register for sending the 2nd byte of data
26	……
27	Write to data transmit register for sending the n2th byte of data

Steps	Operation Flow
28	……
29	Read from status register to detect bus idleness
30	Write to command register, start
31	Write to the data transmit register for sending the first 7 bits of the address and the write flag
32	Write to command register, and clear start
33	Write to the data transmit register for sending the 2nd byte of the address
34	Write to data transmit register, for sending the 1st byte of data
35	Write to data transmit register for sending the 2nd byte of data
36	……
37	Write to data transmit register for sending the nkth byte of data
38	Read from status register to detect bus idleness
39	Write to command register, and stop
40	Read from status register to detect bus idleness
41	Write to command register, and clear stop

10-Bit Addressing Repeat Read

Table 4-38 I^{2}C Point-to-Point Mode Master Device 10-Bit Addressing Repeat Read Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to the data transmit register for sending the first 7 bits of the address and the write flag
13	Write to command register, and clear start
14	Write to the data transmit register for sending the 2nd byte of the address
15	Read from status register to detect bus idleness
16	Write to command register, start
17	Write to the data transmit register for sending the first 7 bits of the address and the read flag
18	Write to command register, and clear start
19	Read the 1st byte from the data receive register
20	Read the 2nd byte from the data receive register
21	Read the 3rd byte from the data receive register

Steps	**Operation Flow**
22	……
23	Read the (n1-2)th byte of data from the data receive register
24	Read the (n1-1)th byte of data from the data receive register
25	Write to command register, no acknowledge
26	Read the n1th byte of data from the data receive register
27	Write to the command register, to start and clear no acknowledge
28	Write to the data transmit register for sending the first 7 bits of the address and the write flag
29	Write to command register, and clear start
30	Write to the data transmit register for sending the 2nd byte of the address
31	Read from status register to detect bus idleness
32	Write to command register, start
33	Write to the data transmit register for sending the first 7 bits of the address and the read flag
34	Write to command register, and clear start
35	Read the 1st byte from the data receive register
36	Read the 2nd byte from the data receive register
37	Read the 3rd byte from the data receive register
38	……
39	Read the (n2-2)th byte of data from the data receive register
40	Read the (n2-1)th byte of data from the data receive register
41	Write to command register, no acknowledge
42	Read the n2th byte of data from the data receive register
43	……
44	Write to the command register, to start and clear no acknowledge
45	Write to the data transmit register for sending the first 7 bits of the address and the write flag
46	Write to command register, and clear start
47	Write to the data transmit register for sending the 2nd byte of the address
48	Read from status register to detect bus idleness
49	Write to command register, start
50	Write to the data transmit register for sending the first 7 bits of the address and the read flag
51	Write to command register, and clear start
52	Read the 1st byte from the data receive register
53	Read the 2nd byte from the data receive register
54	Read the 3rd byte from the data receive register
55	……
56	Read the (nk-2)th byte of data from the data receive register
57	Read the (nk-1)th byte of data from the data receive register
58	Write to command register, no acknowledge
59	Read the nkth byte of data from the data receive register
60	Write to the command register, to stop and clear no acknowledge

Steps	Operation Flow
61	Read from status register to detect bus idleness
62	Write to command register, and clear stop

10-Bit Addressing Write Before Read

Table 4-39 I^2C Point-to-Point Mode Master Device 10-Bit Addressing Write Before Read Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to the data transmit register for sending the first 7 bits of the address and the write flag
13	Write to command register, and clear start
14	Write to the data transmit register for sending the 2nd byte of the address
15	Write to data transmit register, for sending the 1st byte of data
16	Write to data transmit register for sending the 2nd byte of data
17	……
18	Write to data transmit register for sending the mth byte of data
19	Read from status register to detect bus idleness
20	Write to command register, start
21	Write to the data transmit register for sending the first 7 bits of the address and the write flag
22	Write to command register, and clear start
23	Write to the data transmit register for sending the 2nd byte of the address
24	Read from status register to detect bus idleness
25	Write to command register, start
26	Write to the data transmit register for sending the first 7 bits of the address and the read flag
27	Write to command register, and clear start
28	Read the 1st byte from the data receive register
29	Read the 2nd byte from the data receive register
30	Read the 3rd byte from the data receive register
31	……
32	Read the (0-2)th byte from the data receive register
33	Read the (0-1)th byte from the data receive register

Steps	Operation Flow
34	Write to command register, no acknowledge
35	Read the nth byte from the data receive register
36	Write to command register, and stop
37	Read from status register to detect bus idleness
38	Write to command register, and clear stop

10-Bit Addressing Read Before Write

Table 4-40 I^{2}C Point-to-Point Mode Master Device 10-Bit Addressing Read Before Write Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to the data transmit register for sending the first 7 bits of the address and the write flag
13	Write to command register, and clear start
14	Write to the data transmit register for sending the 2nd byte of the address
15	Read from status register to detect bus idleness
16	Write to command register, start
17	Write to the data transmit register for sending the first 7 bits of the address and the read flag
18	Write to command register, and clear start
19	Read the 1st byte from the data receive register
20	Read the 2nd byte from the data receive register
21	Read the 3rd byte from the data receive register
22	……
23	Read the (m-2)th byte of data from the data receive register
24	Read the (m-1)th byte of data from the data receive register
25	Write to command register, no acknowledge
26	Read the mth byte of data from the data receive register
27	Write to the command register, to start and clear no acknowledge
28	Write to the data transmit register for sending the first 7 bits of the address and the write flag
29	Write to command register, and clear start
30	Write to the data transmit register for sending the 2nd byte of the address

Steps	Operation Flow
31	Write to data transmit register, for sending the 1st byte of data
32	Write to data transmit register for sending the 2nd byte of data
33	……
34	Write to data transmit register for sending the nth byte of data
35	Read from status register to detect bus idleness
36	Write to command register, and stop
37	Read from status register to detect bus idleness
38	Write to command register, and clear stop

10-Bit Addressing Hardware All Call

Table 4-41 I^{2}C Point-to-Point Mode Master Device 10-Bit Addressing Hardware All Call Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending all-call address and write flag
13	Write to command register, and clear start
14	Write to the data transmit register, for sending the first 7 bits of master address and bit 1
15	Write to the data transmit register for sending the 2nd byte of master address
16	Write to data transmit register, for sending the 1st byte of data
17	Write to data transmit register for sending the 2nd byte of data
18	……
19	Write to data transmit register for sending the nth byte of data
20	Read from status register to detect bus idleness
21	Write to command register, and stop
22	Read from status register to detect bus idleness
23	Write to command register, and clear stop

10-Bit Addressing Read Device Identification

Table 4-42 I^{2}C Point-to-Point Mode Master Device 10-Bit Addressing Read Device Identification Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to control register
11	Write to command register, start
12	Write to data transmit register for sending the device identification address and write flag
13	Write to command register, and clear start
14	Write to the data transmit register for sending the first 7 bits of the address and the write flag
15	Write to the data transmit register for sending the 2nd byte of the address
16	Read from status register to detect bus idleness
17	Write to command register, start
18	Write to data transmit register for sending device identification address and read flag
19	Write to command register, and clear start
20	Read the 1st byte of device identification from the data receive register
21	Read the 2nd byte of device identification from the data receive register
22	Write to command register, no acknowledge
23	Read the 3rd byte of device identification from the data receive register
24	Write to the command register, to stop and clear no acknowledge
25	Read from status register to detect bus idleness
26	Write to command register, and clear stop

4.5.1.2 Slave Device

7-Bit Addressing Write/Repeat Write

Table 4-43 I^{2}C Point-to-Point Mode Slave Device 7-Bit Addressing Write/Repeat Write Operation Process

Steps	Operation Flow
1	Write to address register
2	Write to delay register 0
3	Write to delay register 1
4	Write to clock stretch register 0

Steps	**Operation Flow**
5	Write to clock stretch register 1
6	Write to control register
7	Read from the status register to detect ongoing operations and bus status
8	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
9	Read from the status register to detect ongoing operations and bus status
10	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
11	……
12	Read from the status register to detect ongoing operations and bus status
13	When the write operation bus is detected idle, read the nth byte of data from the data receive register

7-Bit Addressing Read/Repeat Read

Table 4-44 I^{2}C Point-to-Point Mode Slave Device 7-Bit Addressing Read/Repeat Read Operation Process

Steps	**Operation Flow**
1	Write to address register
2	Write to delay register 0
3	Write to delay register 1
4	Write to clock stretch register 0
5	Write to clock stretch register 1
6	Write to control register
7	Read from the status register to detect ongoing operations and bus status
8	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
9	Read from the status register to detect ongoing operations and bus status
10	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
11	……
12	Read from the status register to detect ongoing operations and bus status
13	When the read operation bus is detected idle, write the nth byte of data to the data transmit register

7-Bit Addressing Write Before Read

Table 4-45 I^{2}C Point-to-Point Mode Slave Device 7-Bit Addressing Write Before Read Operation Process

Steps	**Operation Flow**
1	Write to address register
2	Write to delay register 0
3	Write to delay register 1
4	Write to clock stretch register 0
5	Write to clock stretch register 1
6	Write to control register
7	Read from the status register to detect ongoing operations and bus status
8	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
9	Read from the status register to detect ongoing operations and bus status

Steps	Operation Flow
10	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
11	……
12	Read from the status register to detect ongoing operations and bus status
13	When the write operation bus is detected idle, read the mth byte of data from the data receive register
14	Read from the status register to detect ongoing operations and bus status
15	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
16	Read from the status register to detect ongoing operations and bus status
17	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
18	……
19	Read from the status register to detect ongoing operations and bus status
20	When the read operation bus is detected idle, write the nth byte of data to the data transmit register

7-Bit Addressing Read Before Write

Table 4-46 I^{2}C Point-to-Point Mode Slave Device 7-Bit Addressing Read Before Write Operation Process

Steps	Operation Flow
1	Write to address register
2	Write to delay register 0
3	Write to delay register 1
4	Write to clock stretch register 0
5	Write to clock stretch register 1
6	Write to control register
7	Read from the status register to detect ongoing operations and bus status
8	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
9	Read from the status register to detect ongoing operations and bus status
10	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
11	……
12	Read from the status register to detect ongoing operations and bus status
13	When the read operation bus is detected idle, write the mth byte of data to the data transmit register
14	Read from the status register to detect ongoing operations and bus status
15	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
16	Read from the status register to detect ongoing operations and bus status
17	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
18	……
19	Read from the status register to detect ongoing operations and bus status
20	When the write operation bus is detected idle, read the nth byte of data from the data receive register

10-Bit Addressing Write/Repeat Write

Table 4-47 I^2C Point-to-Point Mode Slave Device 10-Bit Addressing Write/Repeat Write Operation Process

Steps	Operation Flow
1	Write to address register
2	Write to 10-bit addressing address register
3	Write to delay register 0
4	Write to delay register 1
5	Write to clock stretch register 0
6	Write to clock stretch register 1
7	Write to control register
8	Read from the status register to detect ongoing operations and bus status
9	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
10	Read from the status register to detect ongoing operations and bus status
11	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
12	……
13	Read from the status register to detect ongoing operations and bus status
14	When the write operation bus is detected idle, read the nth byte of data from the data receive register

10-Bit Addressing Read/Repeat Read

Table 4-48 I^2C Point-to-Point Mode Slave Device 10-Bit Addressing Read/Repeat Read Operation Process

Steps	Operation Flow
1	Write to address register
2	Write to 10-bit addressing address register
3	Write to delay register 0
4	Write to delay register 1
5	Write to clock stretch register 0
6	Write to clock stretch register 1
7	Write to control register
8	Read from the status register to detect ongoing operations and bus status
9	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
10	Read from the status register to detect ongoing operations and bus status
11	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
12	……
13	Read from the status register to detect ongoing operations and bus status
14	When the read operation bus is detected idle, write the nth byte of data to the data transmit register

10-Bit Addressing Write Before Read

Table 4-49 I^2C Point-to-Point Mode Slave Device 10-Bit Addressing Write Before Read Operation Process

Steps	Operation Flow
1	Write to address register

Steps	Operation Flow
2	Write to 10-bit addressing address register
3	Write to delay register 0
4	Write to delay register 1
5	Write to clock stretch register 0
6	Write to clock stretch register 1
7	Write to control register
8	Read from the status register to detect ongoing operations and bus status
9	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
10	Read from the status register to detect ongoing operations and bus status
11	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
12	……
13	Read from the status register to detect ongoing operations and bus status
14	When the write operation bus is detected idle, read the mth byte of data from the data receive register
15	Read from the status register to detect ongoing operations and bus status
16	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
17	Read from the status register to detect ongoing operations and bus status
18	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
19	……
20	Read from the status register to detect ongoing operations and bus status
21	When the read operation bus is detected idle, write the nth byte of data to the data transmit register

10-Bit Addressing Read Before Write

Table 4-50 I^{2}C Point-to-Point Mode Slave Device 10-Bit Addressing Read Before Write Operation Process

Steps	Operation Flow
1	Write to address register
2	Write to 10-bit addressing address register
3	Write to delay register 0
4	Write to delay register 1
5	Write to clock stretch register 0
6	Write to clock stretch register 1
7	Write to control register
8	Read from the status register to detect ongoing operations and bus status
9	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
10	Read from the status register to detect ongoing operations and bus status
11	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
12	……
13	Read from the status register to detect ongoing operations and bus status
14	When the read operation bus is detected idle, write the mth byte of data to the data transmit register
15	Read from the status register to detect ongoing operations and bus status

Steps	Operation Flow
16	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
17	Read from the status register to detect ongoing operations and bus status
18	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
19	……
20	Read from the status register to detect ongoing operations and bus status
21	When the write operation bus is detected idle, read the nth byte of data from the data receive register

4.5.2 Interrupt Mode

4.5.2.1 Master Device

Write

Table 4-51 I^{2}C Interrupt Mode Master Device Write Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to data transmit register for sending address and write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to data transmit register, for sending the 1st byte of data
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to data transmit register for sending the 2nd byte of data
22	Write to the interrupt status register to clear the bus idle interrupt
23	……
24	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
25	Write to data transmit register for sending the nth byte of data

Steps	Operation Flow
26	Write to the interrupt status register to clear the bus idle interrupt
27	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
28	Write to the interrupt status register to clear the bus idle interrupt
29	Write to command register, and stop
30	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
31	Write to the interrupt status register to clear the bus idle interrupt
32	Write to command register, and clear stop

Read

Table 4-52 I^{2}C Interrupt Mode Master Device Read Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to data transmit register for sending address and read flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Read the 1st byte from the data receive register
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Read the 2nd byte from the data receive register
22	Write to the interrupt status register to clear the bus idle interrupt
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Read the 3rd byte from the data receive register
25	Write to the interrupt status register to clear the bus idle interrupt
26	……
27	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
28	Read the (0-2)th byte from the data receive register

Steps	Operation Flow
29	Write to the interrupt status register to clear the bus idle interrupt
30	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
31	Read the (0-1)th byte from the data receive register
32	Write to the interrupt status register to clear the bus idle interrupt
33	Write to command register, no acknowledge
34	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
35	Read the nth byte from the data receive register
36	Write to the interrupt status register to clear the bus idle interrupt
37	Write to the command register, to stop and clear no acknowledge
38	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
39	Write to the interrupt status register to clear the bus idle interrupt
40	Write to command register, and clear stop

Repeat Write

Table 4-53 I^{2}C Interrupt Mode Master Device Repeat Write Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to data transmit register for sending address and write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to data transmit register, for sending the 1st byte of data
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to data transmit register for sending the 2nd byte of data
22	Write to the interrupt status register to clear the bus idle interrupt
	……

Steps	Operation Flow
23	Write to data transmit register for sending the n1th byte of data
24	Write to the interrupt status register to clear the bus idle interrupt
25	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
26	Write to the interrupt status register to clear the bus idle interrupt
27	Write to command register, start
28	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
29	Write to data transmit register for sending address and write flag
30	Write to the interrupt status register to clear the bus idle interrupt
31	Write to command register, and clear start
32	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
33	Write to data transmit register, for sending the 1st byte of data
34	Write to the interrupt status register to clear the bus idle interrupt
35	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
36	Write to data transmit register for sending the 2nd byte of data
37	Write to the interrupt status register to clear the bus idle interrupt
	……
38	Write to data transmit register for sending the n2th byte of data
39	Write to the interrupt status register to clear the bus idle interrupt
	……
40	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
41	Write to the interrupt status register to clear the bus idle interrupt
42	Write to command register, start
43	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
44	Write to data transmit register for sending address and write flag
45	Write to the interrupt status register to clear the bus idle interrupt
46	Write to command register, and clear start
47	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
48	Write to data transmit register, for sending the 1st byte of data
49	Write to the interrupt status register to clear the bus idle interrupt
50	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
51	Write to data transmit register for sending the 2nd byte of data
52	Write to the interrupt status register to clear the bus idle interrupt
	……
53	When the write operation bus is detected idle, write to the data transmit register to send the nkth byte of data
54	Write to the interrupt status register to clear the bus idle interrupt
55	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
56	Write to the interrupt status register to clear the bus idle interrupt
57	Write to command register, and stop
58	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness

Steps	Operation Flow
59	Write to the interrupt status register to clear the bus idle interrupt
60	Write to command register, and clear stop

Repeat Read

Table 4-54 I^2C Interrupt Mode Master Device Repeat Read Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to data transmit register for sending address and read flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Read the 1st byte from the data receive register
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Read the 2nd byte from the data receive register
22	Write to the interrupt status register to clear the bus idle interrupt
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Read the 3rd byte from the data receive register
25	Write to the interrupt status register to clear the bus idle interrupt
	……
26	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
27	Read the (n1-2)th byte of data from the data receive register
28	Write to the interrupt status register to clear the bus idle interrupt
29	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
30	Read the (n1-1)th byte of data from the data receive register
31	Write to the interrupt status register to clear the bus idle interrupt
32	Write to command register, no acknowledge

Steps	Operation Flow
33	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
34	Read the n1th byte of data from the data receive register
35	Write to the interrupt status register to clear the bus idle interrupt
36	Write to the command register, to start and clear no acknowledge
37	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
38	Write to data transmit register for sending address and read flag
39	Write to the interrupt status register to clear the bus idle interrupt
40	Write to command register, and clear start
41	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
42	Read the 1st byte from the data receive register
43	Write to the interrupt status register to clear the bus idle interrupt
44	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
45	Read the 2nd byte from the data receive register
46	Write to the interrupt status register to clear the bus idle interrupt
47	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
48	Read the 3rd byte from the data receive register
49	Write to the interrupt status register to clear the bus idle interrupt
	……
50	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
51	Read the (n2-2)th byte of data from the data receive register
52	Write to the interrupt status register to clear the bus idle interrupt
53	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
54	Read the (n2-1)th byte of data from the data receive register
55	Write to the interrupt status register to clear the bus idle interrupt
56	Write to command register, no acknowledge
57	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
58	Read the n2th byte of data from the data receive register
59	Write to the interrupt status register to clear the bus idle interrupt
	……
60	Write to command register, start
61	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
62	Write to data transmit register for sending address and read flag
63	Write to the interrupt status register to clear the bus idle interrupt
64	Write to command register, and clear start
65	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
66	Read the 1st byte from the data receive register
67	Write to the interrupt status register to clear the bus idle interrupt
68	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
69	Read the 2nd byte from the data receive register

Steps	Operation Flow
70	Write to the interrupt status register to clear the bus idle interrupt
71	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
72	Read the 3rd byte from the data receive register
73	Write to the interrupt status register to clear the bus idle interrupt
	……
74	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
75	Read the (nk-2)th byte of data from the data receive register
76	Write to the interrupt status register to clear the bus idle interrupt
77	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
78	Read the (nk-1)th byte of data from the data receive register
79	Write to the interrupt status register to clear the bus idle interrupt
80	Write to command register, no acknowledge
81	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
82	Read the nkth byte of data from the data receive register
83	Write to the interrupt status register to clear the bus idle interrupt
84	Write to command register, and stop
85	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
86	Write to the interrupt status register to clear the bus idle interrupt
87	Write to command register, and clear stop

Write before read

Table 4-55 I^{2}C Interrupt Mode Master Device Write Before Read Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to data transmit register for sending address and write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start

Steps	**Operation Flow**
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to data transmit register, for sending the 1st byte of data
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to data transmit register for sending the 2nd byte of data
22	Write to the interrupt status register to clear the bus idle interrupt
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to data transmit register for sending the 3rd byte of data
25	Write to the interrupt status register to clear the bus idle interrupt
	……
26	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
27	Write to data transmit register for sending the mth byte of data
28	Write to the interrupt status register to clear the bus idle interrupt
29	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
30	Write to the interrupt status register to clear the bus idle interrupt
31	Write to command register, start
32	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
33	Write to data transmit register for sending address and write flag
34	Write to the interrupt status register to clear the bus idle interrupt
35	Write to command register, and clear start
36	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
37	Read the 1st byte from the data receive register
38	Write to the interrupt status register to clear the bus idle interrupt
39	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
40	Read the 2nd byte from the data receive register
41	Write to the interrupt status register to clear the bus idle interrupt
	……
42	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
43	Read the (0-2)th byte from the data receive register
44	Write to the interrupt status register to clear the bus idle interrupt
45	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
46	Read the (0-1)th byte from the data receive register
47	Write to the interrupt status register to clear the bus idle interrupt
48	Write to command register, no acknowledge
49	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
50	Read the nth byte from the data receive register
51	Write to the interrupt status register to clear the bus idle interrupt
52	Write to command register, and stop
53	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness

Steps	Operation Flow
54	Write to the interrupt status register to clear the bus idle interrupt
55	Write to command register, and clear stop

Read before write

Table 4-56 I^{2}C Interrupt Mode Master Device Read Before Write Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to data transmit register for sending address and read flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Read the 1st byte from the data receive register
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Read the 2nd byte from the data receive register
22	Write to the interrupt status register to clear the bus idle interrupt
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Read the 3rd byte from the data receive register
25	Write to the interrupt status register to clear the bus idle interrupt
	……
26	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
27	Read the (m-2)th byte of data from the data receive register
28	Write to the interrupt status register to clear the bus idle interrupt
29	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
30	Read the (m-1)th byte of data from the data receive register
31	Write to the interrupt status register to clear the bus idle interrupt
32	Write to command register, no acknowledge

Steps	Operation Flow
33	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
34	Read the mth byte of data from the data receive register
35	Write to the interrupt status register to clear the bus idle interrupt
36	Write to the command register, to start and clear no acknowledge
37	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
38	Write to data transmit register for sending address and write flag
39	Write to the interrupt status register to clear the bus idle interrupt
40	Write to command register, and clear start
41	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
42	Write to data transmit register for sending address and write flag
43	Write to the interrupt status register to clear the bus idle interrupt
44	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
45	Write to data transmit register, for sending the 1st byte of data
46	Write to the interrupt status register to clear the bus idle interrupt
47	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
48	Write to data transmit register for sending the 2nd byte of data
49	Write to the interrupt status register to clear the bus idle interrupt
	……
50	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
51	Write to data transmit register for sending the nth byte of data
52	Write to the interrupt status register to clear the bus idle interrupt
53	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
54	Write to the interrupt status register to clear the bus idle interrupt
55	Write to command register, and stop
56	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
57	Write to the interrupt status register to clear the bus idle interrupt
58	Write to command register, and clear stop

Soft Reset

Table 4-57 I^{2}C Interrupt Mode Master Device Soft Reset Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0

Steps	Operation Flow
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to data transmit register for sending all-call address and write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to data transmit register for sending byte 0x06
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to the interrupt status register to clear the bus idle interrupt
22	Write to command register, and stop
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to the interrupt status register to clear the bus idle interrupt
25	Write to command register, and clear stop

Hardware Programming

Table 4-58 I^{2}C Interrupt Mode Master Device Hardware Programming Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to data transmit register for sending all-call address and write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to data transmit register for sending byte 0x04

Steps	Operation Flow
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to the interrupt status register to clear the bus idle interrupt
22	Write to command register, and stop
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to the interrupt status register to clear the bus idle interrupt
25	Write to command register, and clear stop

Hardware All Call

Table 4-59 I^2C Interrupt Mode Master Device Hardware All Call Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to data transmit register for sending all-call address and write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to data transmit register, for sending the master address and bit 1
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to data transmit register, for sending the 1st byte of data
22	Write to the interrupt status register to clear the bus idle interrupt
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to data transmit register for sending the 2nd byte of data
25	Write to the interrupt status register to clear the bus idle interrupt
	……
26	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
27	Write to data transmit register for sending the nth byte of data

Steps	Operation Flow
28	Write to the interrupt status register to clear the bus idle interrupt
29	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
30	Write to the interrupt status register to clear the bus idle interrupt
31	Write to command register, and stop
32	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
33	Write to the interrupt status register to clear the bus idle interrupt
34	Write to command register, and clear stop

Start Byte

Table 4-60 I^{2}C Interrupt Mode Master Device Start Byte Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to the data transmit register, for sending the start byte
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read the interrupt status register to detect no acknowledge
18	Write to the interrupt status register to clear the no acknowledge interrupt
19	Write to command register, start
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to data transmit register for sending address and write/read flag
22	Write to the interrupt status register to clear the bus idle interrupt
23	Write to command register, and clear start
24	……

Read device identification

Table 4-61 I^2C Interrupt Mode Master Device Read Device Identification Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to data transmit register for sending the device identification address and write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to data transmit register, for sending address and a padding bit
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to the interrupt status register to clear the bus idle interrupt
22	Write to command register, start
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to data transmit register for sending device identification address and read flag
25	Write to the interrupt status register to clear the bus idle interrupt
26	Write to command register, and clear start
27	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
28	Read the 1st byte of device identification from the data receive register
29	Write to the interrupt status register to clear the bus idle interrupt
30	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
31	Read the 2nd byte of device identification from the data receive register
32	Write to the interrupt status register to clear the bus idle interrupt
33	Write to command register, no acknowledge
34	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
35	Read the 3rd byte of device identification from the data receive register
36	Write to the interrupt status register to clear the bus idle interrupt
37	Write to the command register, to stop and clear no acknowledge

Steps	Operation Flow
38	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
39	Write to the interrupt status register to clear the bus idle interrupt
40	Write to command register, and clear stop

10-Bit Addressing Write

Table 4-62 I^{2}C Interrupt Mode Master Device 10-Bit Addressing Write Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to the data transmit register for sending the first 7 bits of the address and the write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to the data transmit register for sending the 2nd byte of the address
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to data transmit register, for sending the 1st byte of data
22	Write to the interrupt status register to clear the bus idle interrupt
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to data transmit register for sending the 2nd byte of data
25	Write to the interrupt status register to clear the bus idle interrupt
26	……
27	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
28	Write to data transmit register for sending the nth byte of data
29	Write to the interrupt status register to clear the bus idle interrupt
30	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
31	Write to the interrupt status register to clear the bus idle interrupt
32	Write to command register, and stop

Steps	Operation Flow
33	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
34	Write to the interrupt status register to clear the bus idle interrupt
35	Write to command register, and clear stop

10-Bit Addressing Read

Table 4-63 I^2C Interrupt Mode Master Device 10-Bit Addressing Read Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to the data transmit register for sending the first 7 bits of the address and the write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to the data transmit register for sending the 2nd byte of the address
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to the interrupt status register to clear the bus idle interrupt
22	Write to command register, start
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to the data transmit register for sending the first 7 bits of the address and the read flag
25	Write to the interrupt status register to clear the bus idle interrupt
26	Write to command register, and clear start
27	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
28	Read the 1st byte from the data receive register
29	Write to the interrupt status register to clear the bus idle interrupt
30	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
31	Read the 2nd byte from the data receive register
32	Write to the interrupt status register to clear the bus idle interrupt

Steps	Operation Flow
33	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
34	Read the 3rd byte from the data receive register
35	Write to the interrupt status register to clear the bus idle interrupt
36	……
37	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
38	Read the (0-2)th byte from the data receive register
39	Write to the interrupt status register to clear the bus idle interrupt
40	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
41	Read the (0-1)th byte from the data receive register
42	Write to the interrupt status register to clear the bus idle interrupt
43	Write to command register, no acknowledge
44	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
45	Read the nth byte from the data receive register
46	Write to the interrupt status register to clear the bus idle interrupt
47	Write to the command register, to stop and clear no acknowledge
48	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
49	Write to the interrupt status register to clear the bus idle interrupt
50	Write to command register, and clear stop

10-Bit Addressing Repeat Write

Table 4-64 I^{2}C Interrupt Mode Master Device 10-Bit Addressing Repeat Write Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to the data transmit register for sending the first 7 bits of the address and the write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness

Steps	Operation Flow
18	Write to the data transmit register for sending the 2nd byte of the address
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to data transmit register, for sending the 1st byte of data
22	Write to the interrupt status register to clear the bus idle interrupt
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to data transmit register for sending the 2nd byte of data
25	Write to the interrupt status register to clear the bus idle interrupt
26	……
27	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
28	Write to data transmit register for sending the n1th byte of data
29	Write to the interrupt status register to clear the bus idle interrupt
30	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
31	Write to the interrupt status register to clear the bus idle interrupt
32	Write to command register, start
33	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
34	Write to the data transmit register for sending the first 7 bits of the address and the write flag
35	Write to the interrupt status register to clear the bus idle interrupt
36	Write to command register, and clear start
37	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
38	Write to the data transmit register for sending the 2nd byte of the address
39	Write to the interrupt status register to clear the bus idle interrupt
40	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
41	Write to data transmit register, for sending the 1st byte of data
42	Write to the interrupt status register to clear the bus idle interrupt
43	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
44	Write to data transmit register for sending the 2nd byte of data
45	Write to the interrupt status register to clear the bus idle interrupt
46	……
47	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
48	Write to data transmit register for sending the n2th byte of data
49	Write to the interrupt status register to clear the bus idle interrupt
50	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
51	……
52	Write to command register, start
53	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
54	Write to the data transmit register for sending the first 7 bits of the address and the write flag
55	Write to the interrupt status register to clear the bus idle interrupt
56	Write to command register, and clear start

Steps	Operation Flow
57	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
58	Write to the data transmit register for sending the 2nd byte of the address
59	Write to the interrupt status register to clear the bus idle interrupt
60	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
66	Write to data transmit register, for sending the 1st byte of data
67	Write to the interrupt status register to clear the bus idle interrupt
68	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
69	Write to data transmit register for sending the 2nd byte of data
70	Write to the interrupt status register to clear the bus idle interrupt
71	……
72	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
73	Write to data transmit register for sending the nkth byte of data
74	Write to the interrupt status register to clear the bus idle interrupt
75	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
76	Write to the interrupt status register to clear the bus idle interrupt
77	Write to command register, and stop
78	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
79	Write to the interrupt status register to clear the bus idle interrupt
80	Write to command register, and clear stop

10-Bit Addressing Repeat Read

Table 4-65 I^{2}C Interrupt Mode Master Device 10-Bit Addressing Repeat Read Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to the data transmit register for sending the first 7 bits of the address and the write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start

Steps	Operation Flow
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to the data transmit register for sending the 2nd byte of the address
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to the interrupt status register to clear the bus idle interrupt
22	Write to command register, start
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to the data transmit register for sending the first 7 bits of the address and the read flag
25	Write to the interrupt status register to clear the bus idle interrupt
26	Write to command register, and clear start
27	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
28	Read the 1st byte from the data receive register
29	Write to the interrupt status register to clear the bus idle interrupt
30	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
31	Read the 2nd byte from the data receive register
32	Write to the interrupt status register to clear the bus idle interrupt
33	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
34	Read the 3rd byte from the data receive register
35	Write to the interrupt status register to clear the bus idle interrupt
36	……
37	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
38	Read the (n1-2)th byte of data from the data receive register
39	Write to the interrupt status register to clear the bus idle interrupt
40	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
41	Read the (n1-1)th byte of data from the data receive register
42	Write to the interrupt status register to clear the bus idle interrupt
43	Write to command register, no acknowledge
44	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
45	Read the n1th byte of data from the data receive register
46	Write to the interrupt status register to clear the bus idle interrupt
47	Write to the command register, to start and clear no acknowledge
48	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
49	Write to the data transmit register for sending the first 7 bits of the address and the write flag
50	Write to the interrupt status register to clear the bus idle interrupt
51	Write to command register, and clear start
52	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
53	Write to the data transmit register for sending the 2nd byte of the address
54	Write to the interrupt status register to clear the bus idle interrupt
55	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness

Steps	Operation Flow
56	Write to the interrupt status register to clear the bus idle interrupt
57	Write to command register, start
58	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
59	Write to the data transmit register for sending the first 7 bits of the address and the read flag
60	Write to the interrupt status register to clear the bus idle interrupt
66	Write to command register, and clear start
67	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
68	Read the 1st byte from the data receive register
69	Write to the interrupt status register to clear the bus idle interrupt
70	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
71	Read the 2nd byte from the data receive register
72	Write to the interrupt status register to clear the bus idle interrupt
73	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
74	Read the 3rd byte from the data receive register
75	Write to the interrupt status register to clear the bus idle interrupt
76	……
77	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
78	Read the (n2-2)th byte of data from the data receive register
79	Write to the interrupt status register to clear the bus idle interrupt
80	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
81	Read the (n2-1)th byte of data from the data receive register
82	Write to the interrupt status register to clear the bus idle interrupt
83	Write to command register, no acknowledge
84	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
85	Read the n2th byte of data from the data receive register
86	Write to the interrupt status register to clear the bus idle interrupt
87	……
88	Write to the command register, to start and clear no acknowledge
89	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
90	Write to the data transmit register for sending the first 7 bits of the address and the write flag
91	Write to the interrupt status register to clear the bus idle interrupt
92	Write to command register, and clear start
93	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
94	Write to the data transmit register for sending the 2nd byte of the address
95	Write to the interrupt status register to clear the bus idle interrupt
96	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
97	Write to the interrupt status register to clear the bus idle interrupt
98	Write to command register, start
99	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness

Steps	Operation Flow
100	Write to the data transmit register for sending the first 7 bits of the address and the read flag
101	Write to the interrupt status register to clear the bus idle interrupt
102	Write to command register, and clear start
103	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
104	Read the 1st byte from the data receive register
105	Write to the interrupt status register to clear the bus idle interrupt
106	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
107	Read the 2nd byte from the data receive register
108	Write to the interrupt status register to clear the bus idle interrupt
109	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
110	Read the 3rd byte from the data receive register
111	Write to the interrupt status register to clear the bus idle interrupt
112	……
113	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
114	Read the (nk-2)th byte of data from the data receive register
115	Write to the interrupt status register to clear the bus idle interrupt
116	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
117	Read the (nk-1)th byte of data from the data receive register
118	Write to the interrupt status register to clear the bus idle interrupt
119	Write to command register, no acknowledge
120	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
121	Read the nkth byte of data from the data receive register
122	Write to the interrupt status register to clear the bus idle interrupt
123	Write to the command register, to stop and clear no acknowledge
124	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
125	Write to the interrupt status register to clear the bus idle interrupt
126	Write to command register, and clear stop

10-Bit Addressing Write Before Read

Table 4-66 I^{2}C Interrupt Mode Master Device 10-Bit Addressing Write Before Read Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0

Steps	Operation Flow
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to the data transmit register for sending the first 7 bits of the address and the write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to the data transmit register for sending the 2nd byte of the address
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to data transmit register, for sending the 1st byte of data
22	Write to the interrupt status register to clear the bus idle interrupt
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to data transmit register for sending the 2nd byte of data
25	Write to the interrupt status register to clear the bus idle interrupt
26	……
27	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
28	Write to data transmit register for sending the mth byte of data
29	Write to the interrupt status register to clear the bus idle interrupt
30	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
31	Write to the interrupt status register to clear the bus idle interrupt
32	Write to command register, start
33	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
34	Write to the data transmit register for sending the first 7 bits of the address and the write flag
35	Write to the interrupt status register to clear the bus idle interrupt
36	Write to command register, and clear start
37	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
38	Write to the data transmit register for sending the 2nd byte of the address
39	Write to the interrupt status register to clear the bus idle interrupt
40	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
41	Write to the interrupt status register to clear the bus idle interrupt
42	Write to command register, start
43	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
44	Write to the data transmit register for sending the first 7 bits of the address and the read flag
45	Write to the interrupt status register to clear the bus idle interrupt
46	Write to command register, and clear start
47	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness

Steps	**Operation Flow**
48	Read the 1st byte from the data receive register
49	Write to the interrupt status register to clear the bus idle interrupt
50	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
51	Read the 2nd byte from the data receive register
52	Write to the interrupt status register to clear the bus idle interrupt
53	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
54	Read the 3rd byte from the data receive register
55	Write to the interrupt status register to clear the bus idle interrupt
56	……
57	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
58	Read the (0-2)th byte from the data receive register
59	Write to the interrupt status register to clear the bus idle interrupt
60	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
66	Read the (0-1)th byte from the data receive register
67	Write to the interrupt status register to clear the bus idle interrupt
68	Write to command register, no acknowledge
69	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
70	Read the nth byte from the data receive register
71	Write to the interrupt status register to clear the bus idle interrupt
72	Write to command register, and stop
73	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
74	Write to the interrupt status register to clear the bus idle interrupt
75	Write to command register, and clear stop

10-Bit Addressing Read Before Write

Table 4-67 I^2C Interrupt Mode Master Device 10-Bit Addressing Read Before Write Operation Process

Steps	**Operation Flow**
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start

Steps	Operation Flow
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to the data transmit register for sending the first 7 bits of the address and the write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to the data transmit register for sending the 2nd byte of the address
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to the interrupt status register to clear the bus idle interrupt
22	Write to command register, start
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to the data transmit register for sending the first 7 bits of the address and the read flag
25	Write to the interrupt status register to clear the bus idle interrupt
26	Write to command register, and clear start
27	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
28	Read the 1st byte from the data receive register
29	Write to the interrupt status register to clear the bus idle interrupt
30	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
31	Read the 2nd byte from the data receive register
32	Write to the interrupt status register to clear the bus idle interrupt
33	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
34	Read the 3rd byte from the data receive register
35	Write to the interrupt status register to clear the bus idle interrupt
36	……
37	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
38	Read the (m-2)th byte of data from the data receive register
39	Write to the interrupt status register to clear the bus idle interrupt
40	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
41	Read the (m-1)th byte of data from the data receive register
42	Write to the interrupt status register to clear the bus idle interrupt
43	Write to command register, no acknowledge
44	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
45	Read the mth byte of data from the data receive register
46	Write to the interrupt status register to clear the bus idle interrupt
47	Write to the command register, to start and clear no acknowledge
48	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
49	Write to the data transmit register for sending the first 7 bits of the address and the write flag
50	Write to the interrupt status register to clear the bus idle interrupt
51	Write to command register, and clear start

Steps	Operation Flow
52	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
53	Write to the data transmit register for sending the 2nd byte of the address
54	Write to the interrupt status register to clear the bus idle interrupt
55	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
56	Write to data transmit register, for sending the 1st byte of data
57	Write to the interrupt status register to clear the bus idle interrupt
58	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
59	Write to data transmit register for sending the 2nd byte of data
60	Write to the interrupt status register to clear the bus idle interrupt
66	……
67	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
68	Write to data transmit register for sending the nth byte of data
69	Write to the interrupt status register to clear the bus idle interrupt
70	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
71	Write to the interrupt status register to clear the bus idle interrupt
72	Write to command register, and stop
73	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
74	Write to the interrupt status register to clear the bus idle interrupt
75	Write to command register, and clear stop

10-Bit Addressing Hardware All Call

Table 4-68 I^{2}C Interrupt Mode Master Device 10-Bit Addressing Hardware All Call Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
14	Write to data transmit register for sending all-call address and write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start

Steps	Operation Flow
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to the data transmit register, for sending the first 7 bits of master address and bit 1
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to the data transmit register for sending the 2nd byte of master address
22	Write to the interrupt status register to clear the bus idle interrupt
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to data transmit register, for sending the 1st byte of data
25	Write to the interrupt status register to clear the bus idle interrupt
26	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
27	Write to data transmit register for sending the 2nd byte of data
28	Write to the interrupt status register to clear the bus idle interrupt
29	……
30	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
31	Write to data transmit register for sending the nth byte of data
32	Write to the interrupt status register to clear the bus idle interrupt
33	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
34	Write to the interrupt status register to clear the bus idle interrupt
35	Write to command register, and stop
36	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
37	Write to the interrupt status register to clear the bus idle interrupt
38	Write to command register, and clear stop

10-Bit Addressing Read Device Identification

Table 4-69 I^{2}C Interrupt Mode Master Device 10-Bit Addressing Read Device Identification Operation Process

Steps	Operation Flow
1	Write to clock low-level register 0
2	Write to clock low-level register 1
3	Write to clock high-level register 0
4	Write to clock high-level register 1
5	Write to start register
6	Write to restart register
7	Write to stop register
8	Write to delay register 0
9	Write to delay register 1
10	Write to interrupt control register
11	Write to control register
12	Write to command register, start
13	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness

Steps	Operation Flow
14	Write to data transmit register for sending the device identification address and write flag
15	Write to the interrupt status register to clear the bus idle interrupt
16	Write to command register, and clear start
17	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
18	Write to the data transmit register for sending the first 7 bits of the address and the write flag
19	Write to the interrupt status register to clear the bus idle interrupt
20	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
21	Write to the data transmit register for sending the 2nd byte of the address
22	Write to the interrupt status register to clear the bus idle interrupt
23	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
24	Write to the interrupt status register to clear the bus idle interrupt
25	Write to command register, start
26	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
27	Write to data transmit register for sending device identification address and read flag
28	Write to the interrupt status register to clear the bus idle interrupt
29	Write to command register, and clear start
30	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
31	Read the 1st byte of device identification from the data receive register
32	Write to the interrupt status register to clear the bus idle interrupt
33	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
34	Read the 2nd byte of device identification from the data receive register
35	Write to the interrupt status register to clear the bus idle interrupt
36	Write to command register, no acknowledge
37	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
38	Read the 3rd byte of device identification from the data receive register
39	Write to the interrupt status register to clear the bus idle interrupt
40	Write to the command register, to stop and clear no acknowledge
41	Upon receiving an interrupt, read from the interrupt status register to detect bus idleness
42	Write to the interrupt status register to clear the bus idle interrupt
43	Write to command register, and clear stop

4.5.2.2 Slave Device

7-Bit Addressing Write/Repeat Write

Table 4-70 I^{2}C Interrupt Mode Slave Device Write/Repeat Write Operation Process

Steps	Operation Flow
1	Write to address register
2	Write to delay register 0
3	Write to delay register 1

Steps	Operation Flow
4	Write to clock stretch register 0
5	Write to clock stretch register 1
6	Write to interrupt control register
7	Write to control register
8	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
9	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
10	Write to the interrupt status register to clear the bus idle interrupt
11	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
12	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
13	Write to the interrupt status register to clear the bus idle interrupt
14	……
15	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
16	When the write operation bus is detected idle, read the nth byte of data from the data receive register
17	Write to the interrupt status register to clear the bus idle interrupt

7-Bit Addressing Write/Repeat Read

Table 4-71 I^{2}C Interrupt Mode Slave Device Write/Repeat Read Operation Process

Steps	Operation Flow
1	Write to address register
2	Write to delay register 0
3	Write to delay register 1
4	Write to clock stretch register 0
5	Write to clock stretch register 1
6	Write to interrupt control register
7	Write to control register
8	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
9	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
10	Write to the interrupt status register to clear the bus idle interrupt
11	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
12	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
13	Write to the interrupt status register to clear the bus idle interrupt
14	……
15	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
16	When the read operation bus is detected idle, write the nth byte of data to the data transmit register
17	Write to the interrupt status register to clear the bus idle interrupt

7-Bit Addressing Write Before Read

Table 4-72 I^{2}C Interrupt Mode Slave Device Write Before Read Operation Process

Steps	**Operation Flow**
1	Write to address register
2	Write to delay register 0
3	Write to delay register 1
4	Write to clock stretch register 0
5	Write to clock stretch register 1
6	Write to interrupt control register
7	Write to control register
8	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
9	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
10	Write to the interrupt status register to clear the bus idle interrupt
11	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
12	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
13	Write to the interrupt status register to clear the bus idle interrupt
14	……
15	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
16	When the write operation bus is detected idle, read the mth byte of data from the data receive register
17	Write to the interrupt status register to clear the bus idle interrupt
18	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
19	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
20	Write to the interrupt status register to clear the bus idle interrupt
21	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
22	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
23	Write to the interrupt status register to clear the bus idle interrupt
24	……
25	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
26	When the read operation bus is detected idle, write the nth byte of data to the data transmit register
27	Write to the interrupt status register to clear the bus idle interrupt

7-Bit Addressing Read Before Write

Table 4-73 I^{2}C Interrupt Mode Slave Device Read Before Write Operation Process

Steps	**Operation Flow**
1	Write to address register
2	Write to delay register 0
3	Write to delay register 1
4	Write to clock stretch register 0
5	Write to clock stretch register 1
6	Write to interrupt control register

Steps	**Operation Flow**
7	Write to control register
8	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
9	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
10	Write to the interrupt status register to clear the bus idle interrupt
11	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
12	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
13	Write to the interrupt status register to clear the bus idle interrupt
14	……
15	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
16	When the read operation bus is detected idle, write the mth byte of data to the data transmit register
17	Write to the interrupt status register to clear the bus idle interrupt
18	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
19	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
20	Write to the interrupt status register to clear the bus idle interrupt
21	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
22	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
23	Write to the interrupt status register to clear the bus idle interrupt
24	……
25	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
26	When the write operation bus is detected idle, read the nth byte of data from the data receive register
27	Write to the interrupt status register to clear the bus idle interrupt

10-Bit Addressing Write/Repeat Write

Table 4-74 I^{2}C Interrupt Mode Slave Device 10-Bit Write/Repeat Write Operation Process

Steps	**Operation Flow**
1	Write to address register
2	Write to 10-bit addressing address register
3	Write to delay register 0
4	Write to delay register 1
5	Write to clock stretch register 0
6	Write to clock stretch register 1
7	Write to interrupt control register
8	Write to control register
9	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
10	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
11	Write to the interrupt status register to clear the bus idle interrupt
12	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
13	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
14	Write to the interrupt status register to clear the bus idle interrupt

Steps	Operation Flow
15	……
16	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
17	When the write operation bus is detected idle, read the nth byte of data from the data receive register
18	Write to the interrupt status register to clear the bus idle interrupt

10-Bit Addressing Read/Repeat Read

Table 4-75 I^{2}C Interrupt Mode Slave Device 10-Bit Read/Repeat Read Operation Process

Steps	Operation Flow
1	Write to address register
2	Write to 10-bit addressing address register
3	Write to delay register 0
4	Write to delay register 1
5	Write to clock stretch register 0
6	Write to clock stretch register 1
7	Write to interrupt control register
8	Write to control register
9	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
10	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
11	Write to the interrupt status register to clear the bus idle interrupt
12	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
13	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
14	Write to the interrupt status register to clear the bus idle interrupt
15	……
16	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
17	When the read operation bus is detected idle, write the nth byte of data to the data transmit register
18	Write to the interrupt status register to clear the bus idle interrupt

10-Bit Addressing Write Before Read

Table 4-76 I^{2}C Interrupt Mode Slave Device 10-Bit Write Before Read Operation Process

Steps	Operation Flow
1	Write to address register
2	Write to 10-bit addressing address register
3	Write to delay register 0
4	Write to delay register 1
5	Write to clock stretch register 0
6	Write to clock stretch register 1
7	Write to interrupt control register
8	Write to control register
9	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status

Steps	Operation Flow
10	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
11	Write to the interrupt status register to clear the bus idle interrupt
12	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
13	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
14	Write to the interrupt status register to clear the bus idle interrupt
15	……
16	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
17	When the write operation bus is detected idle, read the mth byte of data from the data receive register
18	Write to the interrupt status register to clear the bus idle interrupt
19	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
20	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
21	Write to the interrupt status register to clear the bus idle interrupt
22	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
23	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
24	Write to the interrupt status register to clear the bus idle interrupt
25	……
26	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
27	When the read operation bus is detected idle, write the nth byte of data to the data transmit register
28	Write to the interrupt status register to clear the bus idle interrupt

10-Bit Addressing Read Before Write

Table 4-77 I^{2}C Interrupt Mode Slave Device 10-Bit Read Before Write Operation Process

Steps	Operation Flow
1	Write to address register
2	Write to 10-bit addressing address register
3	Write to delay register 0
4	Write to delay register 1
5	Write to clock stretch register 0
6	Write to clock stretch register 1
7	Write to interrupt control register
8	Write to control register
9	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
10	When the read operation bus is detected idle, write the 1st byte of data to the data transmit register
11	Write to the interrupt status register to clear the bus idle interrupt
12	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
13	When the read operation bus is detected idle, write the 2nd byte of data to the data transmit register
14	Write to the interrupt status register to clear the bus idle interrupt
15	……
16	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status

Steps	**Operation Flow**
17	When the read operation bus is detected idle, write the mth byte of data to the data transmit register
18	Write to the interrupt status register to clear the bus idle interrupt
19	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
20	When the write operation bus is detected idle, read the 1st byte of data from the data receive register
21	Write to the interrupt status register to clear the bus idle interrupt
22	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
23	When the write operation bus is detected idle, read the 2nd byte of data from the data receive register
24	Write to the interrupt status register to clear the bus idle interrupt
25	……
26	Upon receiving an interrupt, read the status register to detect ongoing operations and bus status
27	When the write operation bus is detected idle, read the nth byte of data from the data receive register
28	Write to the interrupt status register to clear the bus idle interrupt

Chapter 5 **Timer Hard Core**

CPLD Family products include a Timer IP hard core. The timer is a common16-bit timing counter module, featuring an independent output comparison unit and Pulse Width Modulation (PWM) function.

5.1 Features

- 8-bit slave APB interface, compatible with AMBA APB3 protocol, with 1K/2K/4K/7K clock frequency up to 100MHz, and 10K clock frequency up to 76MHz
- Working modes: Watchdog, Auto-reset Timer, Pulse Width Modulation, Phase and Frequency Correction Pulse Width Modulation
- Counting precision range: 0.25μs-78.982ms
- Input clock division
- Auto reload
- Time stamps
- Interrupt

5.2 Timer Primitive

When using Timer hard cores, the user must instantiate the corresponding GTP_TIMER primitive, which needs to be used in conjunction with GTP_APB. The relevant information for GTP_TIMER is described as below.

```
GTP_TIMER     U_GTP_TIMER
(
       .RST_N      (rst_sys_n        ),
       .CLK        (clk              ),
       .STAMP      (stamp            ),
       .PWM        (pwm              ),
       .IRQ        (irq_timer        )
);
```

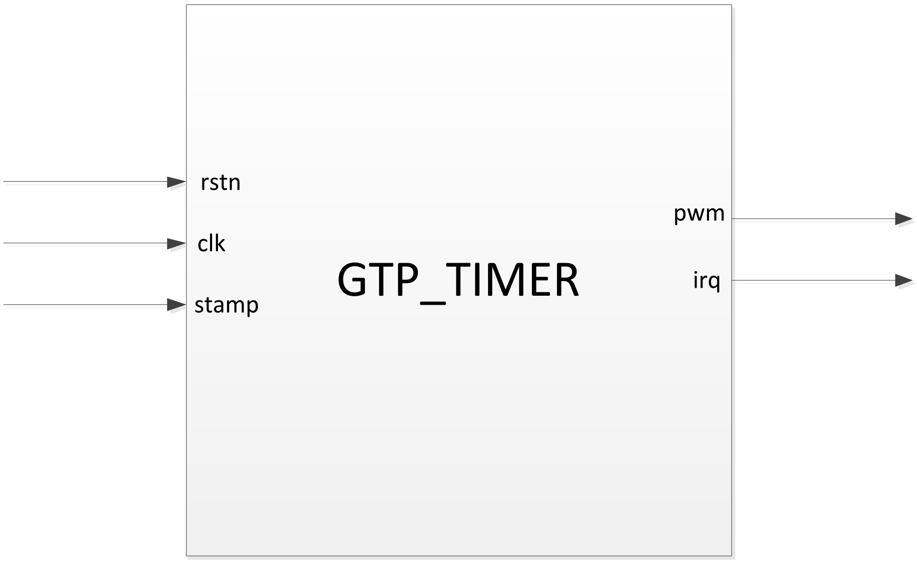

Figure 5-1 Timer Module Signal Input/Output Diagram

Table 5-1 Timer Input/Output Signal List

Item	**Direction**	**Description**
rstn	Input	Asynchronous reset, active low
clk	Input	Timing clock, with the maximum frequency of 4MHz pclk and clk are asynchronous clocks
stamp	Input	Time stamp collection Pulse signal
pwm	Output	Pulse width modulation
irq	Output	Interrupt request

5.3 Register Description

Table 5-2 Timer Register List

Item	**R/W**	**Address**	**Description**
CTLR	R/W	00000	Control Register
OPTIONR	R/W	00001	Option register
IRQCTLR	R/W	00010	Interrupt Control Register
CMDR	R/W	00011	Command register
CYCLER0	R/W	00100	Cycle register 0
CYCLER1	R/W	00101	Cycle register 1
PHASER0	R/W	00110	Phase register 0
PHASER1	R/W	00111	Phase register 1
CCYCLER0	R	01000	Current cycle register 0
CCYCLER1	R	01001	Current cycle register 1
CPHASER0	R	01010	Current phase register 0
CPHASER1	R	01011	Current phase register 1

Item	R/W	Address	Description
STAMPR0	R	01100	Timestamp register 0
STAMPR1	R	01101	Timestamp register 1
CNTR0	R	01110	Count register 0
CNTR1	R	01111	Count register 1
STATUSR	R	10000	Status register
IRQSTATUSR	R/W	10001	Interrupt Status Registers

5.3.1 Control Register

Table 5-3 Timer Control Register List

Bit	Item	Initial Value	Description
[7:6]	Reserved		
[5:4]	mode	2’d0	Mode selection 00: Watchdog 01: Counter 10: Pulse Width Modulator 11: Phase/Frequency Correction Pulse Width Modulator
[3:1]	div_sel	3’d0	Count clock division selection (Modes 10 and 11 do not support 1 division) 000: No Clock 001: Divide-by-1 010: Divide-by-8 011: Divide-by-64 100: Divide-by-256 101: Divide-by-1024 110: Divide-by-2048 111: Divide-by-4096
[0]	timer_en	1’b0	Timer enable 1: Enabled 0: Disabled

5.3.2 Option register

Table 5-4 Timer Option Register List

Bit	Item	Initial Value	Description
[7:5]	Reserved		
[4]	rf_sel	1’b0	Output synchronization selection 0: Rising edge 1: Falling edge
[3]	pwm_inv	1’b0	Pulse width modulation output inversion 0: Not inverted 1: Inverted
[2]	pwm_en	1’b0	Pulse width modulation output enable 0: at 0 1: Enabled
[1]	autorld_en	1’b0	Auto-reload enable 0: Disabled 1: Enabled When the counter is zero, if auto-reload is enabled, the values of the

Bit	Item	Initial Value	Description
			cycle register and phase register are loaded into the current cycle register and current phase register. If auto-reload is disabled, 16’hFFFF and 16’h7FFF are loaded into the current cycle register and current phase register respectively.
[0]	stamp_en	1’b0	Timestamp enable 0: disable; 1: enable

5.3.3 Interrupt Control Register

Table 5-5 Timer Interrupt Control Register List

Bit	Item	Initial Value	Description
[7:3]	Reserved		
[2]	irq_stamp_en	1’b0	Timestamp interrupt enable 1: Enabled 0: Disabled This function is available for watchdog, counter, pulse width modulator, and phase/frequency correction pulse width modulator.
[1]	irq_phase_en	1’b0	Phase interrupt enable 1: Enabled 0: Disabled This function is available for pulse width modulator and phase/frequency correction pulse width modulator.
[0]	irq_overflow_en	1’b0	Overflow interrupt enable 1: Enabled 0: Disabled This function is available for watchdog, counter, pulse width modulator, and phase/frequency correction pulse width modulator.

5.3.4 Command register

Reset counting and pause counting functions are available for watchdog, counter, pulse width modulator, and phase/frequency correction pulse width modulator.

Table 5-6 Timer Command Register List

Bit	Item	Initial Value	Description
[7:2]	Reserved		
[1]	pause	1’b0	Pause counting
[0]	reset	1’b0	Reset counting

5.3.5 Cycle register 0

Table 5-7 Timer Cycle Register 0 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	cycle[7:0]	8’hFF	Low 8 bits of cycle register

5.3.6 Cycle register 1

Table 5-8 Timer Cycle Register 1 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	cycle[15:8]	8’hFF	High 8 bits of cycle register

5.3.7 Phase register 0

Table 5-9 Timer Phase Register 0 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	phase[7:0]	8’hFF	Low 8 bits of phase register

5.3.8 Phase register 1

Table 5-10 Timer Phase Register 1 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	phase[15:8]	8’h7F	High 8 bits of phase register

5.3.9 Current cycle register 0

Table 5-11 Timer Current Cycle Register 0 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	ccycle[7:0]	8’hFF	Low 8 bits of current cycle register

5.3.10 Current cycle register 1

Table 5-12 Timer Current Cycle Register 1 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	ccycle[15:8]	8’hFF	High 8 bits of current cycle register

5.3.11 Current phase register 0

Table 5-13 Timer Current Phase Register 0 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	cphase[7:0]	8’hFF	Low 8 bits of current phase register

5.3.12 Current phase register 1

Table 5-14 Timer Current Phase Register 1 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	cphase[15:8]	8’h7F	High 8 bits of current phase register

5.3.13 Timestamp register 0

Table 5-15 Timer Timestamp Register 0 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	stamp[7:0]	8’d0	Low 8 bits of timestamp register

5.3.14 Timestamp register 1

Table 5-16 Timer Timestamp Register 1 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	stamp[15:8]	8’d0	High 8 bits of timestamp register

5.3.15 Count register 0

Table 5-17 Timer Count Register 0 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	cnt[7:0]	8’d0	Low 8 bits of counter

5.3.16 Count register 1

Table 5-18 Timer Count Register 0 List

Bit	**Item**	**Initial Value**	**Description**
[7:0]	cnt[15:8]	8’d0	High 8 bits of counter

5.3.17 Status register

Table 5-19 Timer Status Register List

Bit	**Item**	**Description**
[7:2]	Reserved	
[1]	phase	Phase top indication
[0]	cycle	Cycle top indication

5.3.18 Interrupt Status Registers

Table 5-20 Timer Interrupt Status Register List

Bit	**Item**	**Description**
[7:3]	Reserved	
[2]	irq_stamp	Timestamp interrupt indication. Setting the timestamp interrupt enable bit of the interrupt control register to 0 can clear the timestamp interrupt indication.
[1]	irq_phase	Phase top interrupt indication. Setting the phase top interrupt enable bit of the interrupt control register to 0 can clear the phase top interrupt indication.
[0]	irq_overflow	Overflow interrupt indication. Setting the overflow interrupt enable bit of the interrupt control register to 0 can clear the overflow interrupt indication.

5.4 Interface timing

The timing diagrams for the timer in different modes are described as below, where cnt[15:0] is the internal 16-bit counter of the timer, and "cycle" is the internal cycle signal.

5.4.1 Watchdog

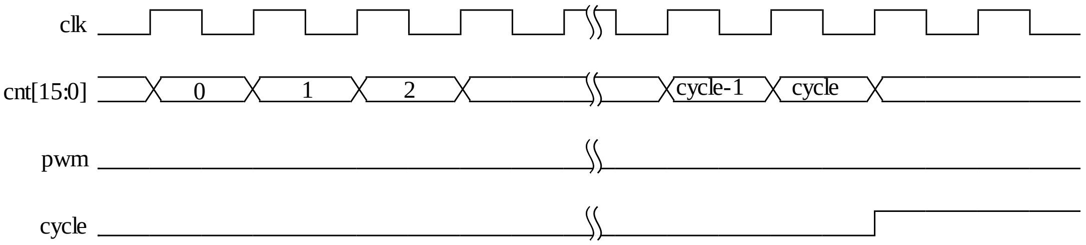

Figure 5-2 Watchdog Mode Timing Diagram

5.4.2 Counter

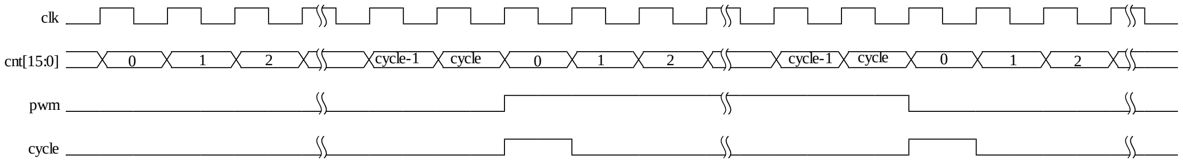

Figure 5-3 Counter Mode Timing Diagram

5.4.3 Pulse Width Modulator

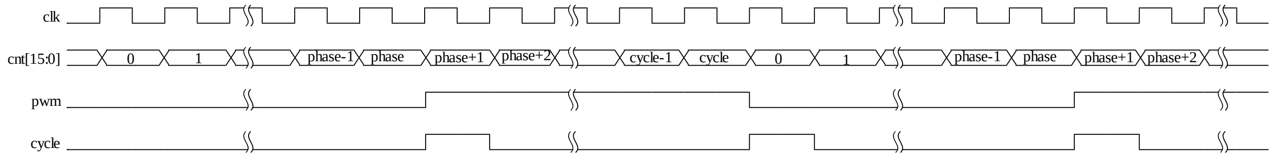

Figure 5-4 Pulse Width Modulator Mode Timing Diagram

5.4.4 Phase/Frequency Correction Pulse Width Modulator

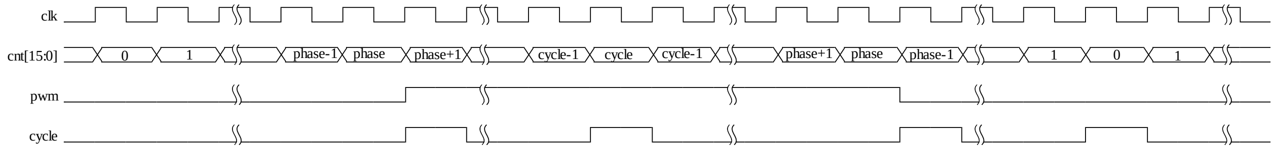

Figure 5-5 Phase/Frequency Correction Pulse Width Modulator Mode Timing Diagram

5.5 Operation Flow

5.5.1 Watchdog

Table 5-21 Watchdog Operation Process

Steps	Operation Flow
1	Write to cycle register 0
2	Write to cycle register 1
3	Write to option register
4	Write to interrupt control register
5	Write to control register

5.5.2 Counter

Table 5-22 Counter Operation Process

Steps	Operation Flow
1	Write to cycle register 0
2	Write to cycle register 1
3	Write to option register
4	Write to interrupt control register
5	Write to control register

5.5.3 Pulse Width Modulator

Table 5-23 Pulse Width Modulator Operation Process

Steps	Operation Flow
1	Write to cycle register 0
2	Write to cycle register 1
3	Write to phase register 0
4	Write to phase register 1
5	Write to option register
6	Write to interrupt control register
7	Write to control register

5.5.4 Phase/Frequency Correction Pulse Width Modulator

Table 5-24 Phase/Frequency Correction Pulse Width Modulator Operation Process

Steps	Operation Flow
1	Write to cycle register 0
2	Write to cycle register 1
3	Write to phase register 0
4	Write to phase register 1
5	Write to option register
6	Write to interrupt control register
7	Write to control register

5.5.5 Reset counting

Table 5-25 Reset Counting Operation Process

Steps	Operation Flow
1	Write to command register, and set reset bit to 1
2	Write to command register, and set reset bit to 0

5.5.6 Pause counting

Table 5-26 Pause Counting Operation Process

Steps	**Operation Flow**
1	Write to command register, and set pause bit to 1

5.5.7 Monitor Counting

Table 5-27 Monitor Counting Operation Process

Steps	**Operation Flow**
1	Read from count register 0
2	Read from count register 1

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