PK02010_PGL50G_FBG484

(V1.1)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.1	26.08.2022	Initial release

About this Manual

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Terms and Abbreviations	Meaning
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PGL50G_FBG484 uses a Wire Bond BGA type of packaging. Package size: 23x23mm; Number of balls: 484; Ball pitch: 1.0mm; Maximum package thickness: 2.4mm.

Chapter 2 Package Dimension

Table 2-1 Dimensional Values

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	2.00	2.20	2.40	c	0.51	0.56	0.61
A1	0.37	0.47	0.57	e	-	1.0	-
A2	1.12	1.17	1.22	b	0.50	0.60	0.70
D	22.8	23.0	23.2	aaa	-	-	0.20
E	22.8	23.0	23.2	ccc	-	-	0.20
D1	-	21.0	-	ddd	-	-	0.15
E1	-	21.0	-	eee	-	-	0.25
D2	19.30	19.5	19.70	D3	-	14.7	-
E2	19.30	19.5	19.70	E3	-	14.7	-

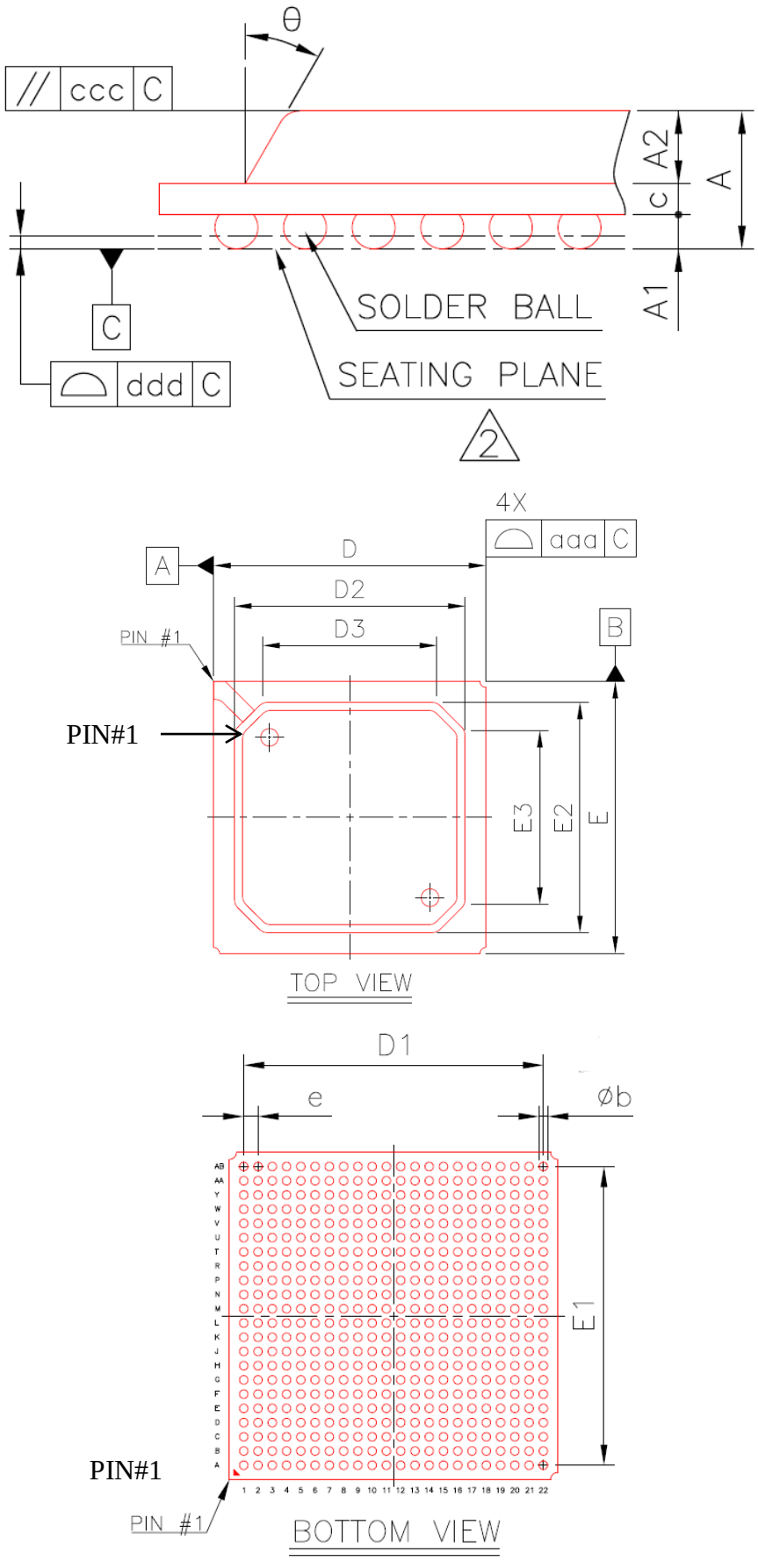

Figure 2-1 Package Outline Dimension (POD)

Note: PIN#1 is the pin 1 position of the chip.

Chapter 3 Pin Definitions

The number of user IOs for the PGL50G_FBG484 product is 332.

Table 3-1 Product Pin Definitions

PIN name	PIN type	PIN description
General PIN		
DIFFIO_[0,1,2,3]_[0…n][N,P]	I/O	**General** IO: (1) "DIFFIO" indicates the pin supports differential input/output and can be used for transmitting and receiving LVDS signals; (2) "B[0,1,2,3]" indicates bank numbers; (3) "[0…n]" indicates the number of programmable I/O pairs in a bank; (4) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end; (5) Before or during configuration, when IO_STATUS_C=0, enable internal pull-up resistors, when IO_STATUS_C=1,disable internal pull-up resistors; (6) In user mode, Unused I/Os default to PLLDOWN, but can be set to PLLUP, PLLDOWN, or UNUSED via bitstream;
DIFFI_[0,1,2,3]_[0…n]_[N,P]	I/O	**General** IO: (1) "DIFFI" indicates the pin only supports differential input and can receive differential input signals; (2) "B[0,1,2,3]" indicates bank numbers; (3) "[0…n]" indicates the number of programmable I/O pairs in a bank; (4) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end; (5) Before or during configuration, when IO_STATUS_C=0, enable internal pull-up resistors, when IO_STATUS_C=1,disable internal pull-up resistors; (6) In user mode, Unused I/Os default to PLLDOWN, but can be set to PLLUP, PLLDOWN, or UNUSED via bitstream;
Multiplexed Pin		
Configurable Multiplexed PIN		
MODE_1	input	Multi-function configuration input pin, used for selecting between master and slave configuration modes: (1) MODE_1=0, master mode; (2) MODE_1=1, slave mode.
MODE_0	input	Multi-function configuration input pin, used for selecting between parallel and serial configuration modes: (1) MODE_0=0, parallel configuration; (2) MODE_0=1, serial configuration.
INIT_FLAG_N	Bidirectional (open-drain)	Initialization and configuration status pin: (1) When it is low, it indicates that the FPGA's internal

PIN name	PIN type	PIN description
		CRAM is being cleared, and this pin will be released by internal control upon completion. (2) If this pin is pulled low externally, it will delay the configuration process; (3) If this pin is low during configuration, it indicates an internal configuration error occurred; (4) This pin is an open-drain output and should be connected to VCCIO2 via an external pull-up resistor.
CFG_CLK	inpu, output	Multi-function configuration clock pin: (1) In the slave mode, this pin serves as a clock input to obtain configuration data from external sources; (2) In the master mode, this pin serves as a clock output to obtain configuration data from external sources; (3) When the clock is not needed (such as in the JTAG mode), this pin is in the high-z state.
ECCLK	input	Multi-function configuration clock pin: Optional external configuration clock input pin in the master mode
CS_N	inpu, output	Multi-function configuration pin: (1) In the Slave Parallel configuration mode, this pin enables the configuration data interface when it is low; (2) In the SPI x1 mode, when this pin is connected to the Slave Data input interface of the SPI Flash, FPGA will send instructions and initial address to the SPI Flash; (3) In the SPI x2 and x4 modes, it is connected to the SPI flash's IO0 as the [0]th bit of the data bus.
CSO_N	output	Multi-function configuration pin: (1) In the slave parallel configuration mode, it serves as the cascaded chip select signal output; (2) In the master SPI mode, it serves as the chip select signal output.
D0	input	Multi-function configuration pin: (1) In the SPI x1 mode, this pin connects to the Slave Data output interface of the SPI Flash, and FPGA receives serial data from the SPI Flash, i.e., Master Input/Slave Output; (2) In the SPI x2 and x4 modes, this pin also serves as the [1]st bit of the SPI data bus; (3) In the parallel or BPI mode, this pin serves as the lowest bit of the data bus (4) In the Slave Serial mode, this pin serves as data input.
D[1,2]	inpu, output	Multi-function configuration pins: (1) In the SPI x2 and x4 modes, pin D[1] serves as the [2]nd bit connected to SPI flash's IO2, pin D[2] as the [3]rd bit connected to SPI flash's IO3.; (2) In the Slave parallel mode, this pin serve as the [1:2] bits of the data bus.
D[3, 4, 5…15]	inpu, output	Multi-function configuration pins: (1) In the Slave Parallel mode with x8 width, D[7:3] serves as the [7:3]th bit of the data bus; (2) In the Slave Parallel mode with x16 width, D[15:3] serves as the [15:3]th bit of the data bus.
RWSEL	input	Multi-function configuration pin, for selecting the read/write input in the Slave Parallel configuration mode:

PIN name	PIN type	PIN description
		(1) When it is high, the Slave Parallel configuration mode reads data from the data bus; (2) When it is low, the Slave Parallel configuration mode writes data to the data bus; (3) Read and write can be switched only when CS_N is high.
DOUT_BUSY	output	Multi-function configuration pin: (1) During readback in the slave parallel mode, this pin indicates the device status; It indicates the data read from the bus is invalid when high; (2) In the Slave serial configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK (3) In the SPI configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK.
IO_STATUS_C	input	Multi-function configuration pin, used for controlling whether the pull-up resistors for all user IOs are enabled during the configuration process: (1) When it is set to "0", the internal pull-up resistors for user IOs are enabled before or during configuration; (2) When it is set to "1", the internal pull-up resistors for user IOs are disabled before or during configuration; (3) This pin must not be left floating before or during configuration.
ADR[0, 1, …, 25]	output	Multi-function configuration pin, address output in BPI configuration mode; (1) After configuration is complete, it can be used as user IO.
BFWE_N	output	Multi-function configuration pin, used for providing a low-level write enable signal for parallel NOR FLASH in the BPI configuration mode.
BFOE_N	output	Multi-function configuration pin, used for providing a low-level output enable signal for parallel NOR FLASH in the BPI configuration mode.
BFCE_N	output	Multi-function configuration pin, used for providing a low-level chip select control signal for parallel NOR FLASH in the BPI configuration mode；
BHDC	output	In BPI mode, there is high output during the configuration
BLDC	output	In BPI mode, there is low output during the configuration
Clock Pin		
GCLK[0,1,2,3…,30,31]	input	Dedicated global clock pin. Can also serve as a general user I/O, 8 PADs for each bank When it serves as a differential clock input, GCLK[1,3,5,…,27,29,31] are the internal valid input.
PLL[1,2,3,4,5]_CLK[0,1,2,…,13,14,15]	input	Optional PLL reference clock input, PLL can directly input the clock from these pin. Optional PLL feedback clock input, PLL can externally feedback the clock from these pin. Also used as general user I/Os.
External Memory Interface PIN		
DQS[0,1,2,3,4,5,6,7,8][#]_[1,3]	DQS	Multi-function pin. Used to connect to the DQS/DQS# signal pins of external memory. Also used as general user I/Os.

PIN name	PIN type	PIN description
DQ[0,1,2,3,4,5,6,7,8][#]_[1,3]	DQ	Multi-function pin, can connect to the DQ signal pins of external memory. Also used as general user I/Os.
Reference Pin		
VREF_[B0,B1,B2,B3]	input	External reference Voltage pin, for providing reference voltage input for each BANK.
Dedicated Pin		
CFG_DONE	Bidirectional (open-drain)	Dedicated configuration status pin. Serves as a status output, driven low before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.
RST_N	input	Dedicated configuration pin, internally weak pull-up, for restarting the configuration process, active-low. It is recommended that users externally pull up the RST_N with a resistor when using this pin. When this pin is low, the FPGA enters a reset state, and all IOs are in the High-z state.
TCK	input	Dedicated JTAG test clock input pin
TMS	input	Dedicated JTAG test mode selection input pin
TDI	input	Dedicated JTAG test data input pin
TDO	output	Dedicated JTAG test data output pin
Power Pin, Ground Pin		
VCC	POWER	Core power supply, 1.2V. Power supply for core logic
VCCAUX	POWER	Auxiliary power, 3.3V.
VCCEFUSE	POWER	eFuse power pin; should be used in the following two situations: When the configuration of eFuse function is needed, this pin is connected to 3.3V power and should be powered up according to the recommended power-up sequence. After configuration, the voltage can be maintained at 3.3V or grounded after powering down according to the power-down sequence requirements; it should not be left floating. If the configuration of eFuse function is not needed. This pin should be grounded.
VCCIO[0,1,2,3]	POWER	IO BANK power
VSS	GROUND	GND
Reserved Pin		
NC		No need to be connected, left floating
CMPCS_B		No need to be connected, left floating
STAND_BY		No need to be connected, left floating

Chapter 4 Pin Name list

Table 4-1 Pin Name List

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
BANK0	DIFFIO_B0_0P/IO_STATUS_C	A3	IO_1_P	83.0848	
BANK0	DIFFIO_B0_0N/VREF_B0	A4	IO_1_N	86.4574	
BANK0	DIFFIO_B0_1P	C5	IO_2_P	89.9436	
BANK0	DIFFIO_B0_1N	A5	IO_2_N	91.3424	
BANK0	DIFFIO_B0_2P	D6	IO_3_P	57.9014	
BANK0	DIFFIO_B0_2N	C6	IO_3_N	69.3227	
BANK0	DIFFIO_B0_3P	B6	IO_4_P	86.3187	
BANK0	DIFFIO_B0_3N	A6	IO_4_N	82.6487	
BANK0	DIFFIO_B0_4P	C7	IO_5_P	79.2449	
BANK0	DIFFIO_B0_4N	A7	IO_5_N	82.6322	
BANK0	DIFFIO_B0_5P	G9	IO_6_P	75.7397	
BANK0	DIFFIO_B0_5N	H10	IO_6_N	76.9324	
BANK0	DIFFIO_B0_6P	B8	IO_7_P	71.7224	
BANK0	DIFFIO_B0_6N	A8	IO_7_N	82.9509	
BANK0	DIFFIO_B0_7P	D9	IO_8_P	65.8025	
BANK0	DIFFIO_B0_7N	C8	IO_8_N	66.5072	
BANK0	DIFFIO_B0_8P	E10	IO_9_P	63.4859	
BANK0	DIFFIO_B0_8N	F10	IO_9_N	63.7796	
BANK0	DIFFIO_B0_9P	C9	IO_10_P	80.0236	
BANK0	DIFFIO_B0_9N/VREF_B0	A9	IO_10_N	80.7546	
BANK0	DIFFIO_B0_10P	D7	IO_11_P	75.6042	
BANK0	DIFFIO_B0_10N	D8	IO_11_N	75.503	
BANK0	DIFFIO_B0_11P	D10	IO_12_P	62.0945	
BANK0	DIFFIO_B0_11N	C10	IO_12_N	50.4411	
BANK0	DIFFIO_B0_12P	G11	IO_13_P	89.5826	
BANK0	DIFFIO_B0_12N	H11	IO_13_N	87.7015	
BANK0	DIFFIO_B0_13P/GCLK19/PLL1_CLK0	B10	IO_14_P	86.0851	
BANK0	DIFFIO_B0_13N/GCLK18/PLL1_CLK1	A10	IO_14_N	65.9978	
BANK0	DIFFIO_B0_14P/GCLK17/PLL1_CLK2	C11	IO_15_P	88.5156	
BANK0	DIFFIO_B0_14N/GCLK16/PLL1_CLK3	A11	IO_15_N	88.4943	
BANK0	DIFFIO_B0_15P/GCLK15/PLL1_CLK4	D11	IO_16_P	69.2437	

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
BANK0	DIFFIO_B0_15N/GCLK14/PLL1_CLK5	C12	IO_16_N	56.5025	
BANK0	DIFFIO_B0_16P/GCLK13/PLL1_CLK6	B12	IO_17_P	74.0222	
BANK0	DIFFIO_B0_16N/GCLK12/PLL1_CLK7	A12	IO_17_N	76.2449	
BANK0	DIFFIO_B0_17P	C13	IO_18_P	81.5534	
BANK0	DIFFIO_B0_17N/VREF_B0	A13	IO_18_N	82.8527	
BANK0	DIFFIO_B0_18P	E12	IO_19_P	79.4066	
BANK0	DIFFIO_B0_18N	D12	IO_19_N	81.3475	
BANK0	DIFFIO_B0_19P	H12	IO_20_P	77.6835	
BANK0	DIFFIO_B0_19N	F12	IO_20_N	76.6838	
BANK0	DIFFIO_B0_20P	F13	IO_21_P	67.5335	
BANK0	DIFFIO_B0_20N	D13	IO_21_N	68.2045	
BANK0	DIFFIO_B0_21P	H13	IO_22_P	81.6396	
BANK0	DIFFIO_B0_21N	G13	IO_22_N	80.7181	
BANK0	DIFFIO_B0_22P	E14	IO_23_P	72.9927	
BANK0	DIFFIO_B0_22N	F15	IO_23_N	71.343	
BANK0	DIFFIO_B0_23P	D14	IO_24_P	66.5006	
BANK0	DIFFIO_B0_23N	C14	IO_24_N	45.5873	
BANK0	DIFFIO_B0_24P	B14	IO_25_P	61.7965	
BANK0	DIFFIO_B0_24N	A14	IO_25_N	83.4305	
BANK0	DIFFIO_B0_25P	C15	IO_26_P	77.9182	
BANK0	DIFFIO_B0_25N	A15	IO_26_N	79.6858	
BANK0	DIFFIO_B0_26P	D15	IO_27_P	84.1993	
BANK0	DIFFIO_B0_26N/VREF_B0	C16	IO_27_N	83.0123	
BANK0	DIFFIO_B0_27P	B16	IO_28_P	65.3333	
BANK0	DIFFIO_B0_27N	A16	IO_28_N	83.4252	
BANK0	DIFFIO_B0_28P	C17	IO_29_P	85.5204	
BANK0	DIFFIO_B0_28N	A17	IO_29_N	87.7209	
BANK0	DIFFIO_B0_29P	B18	IO_30_P	77.1897	
BANK0	DIFFIO_B0_29N	A18	IO_30_N	76.4697	
BANK0	DIFFIO_B0_30P	E16	IO_31_P	64.6914	
BANK0	DIFFIO_B0_30N	D17	IO_31_N	63.7538	
BANK1	DIFFI_B1_0P/ADR25	C19	IO_32_P	87.3953	DQ0_B1/DQ0_B1_G

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
					ATE_OUT
BANK1	DIFFI_B1_0N/ADR24/VREF_B1	B20	IO_32_N	88.4766	DQ0_B1/DQ0_B1_GATE_IN
BANK1	DIFFI_B1_1P	G16	IO_33_P	65.1706	DQ0_B1
BANK1	DIFFI_B1_1N	G17	IO_33_N	64.2551	DQ0_B1
BANK1	DIFFI_B1_2P	F16	IO_34_P	68.0297	DQS0_B1
BANK1	DIFFI_B1_2N	F17	IO_34_N	60.1652	DQS0#_B1
BANK1	DIFFI_B1_11P	B21	IO_43_P	111.446	DQ1_B1
BANK1	DIFFI_B1_11N	B22	IO_43_N	113.999	DQ1_B1
BANK1	DIFFI_B1_12P	A20	IO_44_P	121.961	DQ1_B1
BANK1	DIFFI_B1_12N	A21	IO_44_N	110.82	DQ1_B1
BANK1	DIFFI_B1_13P/	H16	IO_45_P	76.4754	DQ2_B1
BANK1	DIFFI_B1_13N/VREF_B1	H17	IO_45_N	77.4966	DQ2_B1
BANK1	DIFFI_B1_14P/ADR23	D19	IO_46_P	89.9305	DQ2_B1
BANK1	DIFFI_B1_14N/ADR22	D20	IO_46_N	90.2218	DQ2_B1
BANK1	DIFFI_B1_15P/ADR21	F18	IO_47_P	79.3155	DQS2_B1
BANK1	DIFFI_B1_15N/ADR20	F19	IO_47_N	78.9583	DQS2#_B1
BANK1	DIFFI_B1_16P/ADR19	D21	IO_48_P	101.853	DQ2_B1
BANK1	DIFFI_B1_16N/ADR18	D22	IO_48_N	102.501	DQ2_B1
BANK1	DIFFI_B1_17P/ADR17	C20	IO_49_P	119.376	DQ2_B1
BANK1	DIFFI_B1_17N/ADR16	C22	IO_49_N	117.314	DQ2_B1
BANK1	DIFFI_B1_18P/ADR15	G19	IO_50_P	96.6666	DQ2_B1
BANK1	DIFFI_B1_18N/ADR14	F20	IO_50_N	96.1613	DQ2_B1
BANK1	DIFFI_B1_19P/ADR13	H19	IO_51_P	46.5441	DQ2_B1/DQ2_B1_GATE_OUT
BANK1	DIFFI_B1_19N/ADR12	H18	IO_51_N	66.4718	DQ2_B1/DQ2_B1_GATE_IN
BANK1	DIFFI_B1_20P/ADR11	E20	IO_52_P	103.38	DQ3_B1
BANK1	DIFFI_B1_20N/ADR10	E22	IO_52_N	104.093	DQ3_B1
BANK1	DIFFI_B1_21P/ADR9	J17	IO_53_P	70.9984	DQ3_B1
BANK1	DIFFI_B1_21N/ADR8	K17	IO_53_N	75.87	DQ3_B1
BANK1	DIFFI_B1_22P/ADR7	F21	IO_54_P	84.7175	DQS3_B1
BANK1	DIFFI_B1_22N/ADR6	F22	IO_54_N	79.2471	DQS3#_B1
BANK1	DIFFI_B1_23P/ADR5	H20	IO_55_P	76.6528	DQ3_B1
BANK1	DIFFI_B1_23N/ADR4	J19	IO_55_	69.5454	DQ3_B1

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
			N		
BANK1	DIFFI_B1_24P	G20	IO_56_P	96.4917	DQ3_B1
BANK1	DIFFI_B1_24N	G22	IO_56_N	99.2525	DQ3_B1
BANK1	DIFFI_B1_25P/GCLK11/PLL1_CLK8/PLL4_CLK0/PLL5_CLK0	K20	IO_57_P	79.5061	DQ3_B1
BANK1	DIFFI_B1_25N/GCLK10/PLL1_CLK9/PLL4_CLK1/PLL5_CLK1	K19	IO_57_N	82.1782	DQ3_B1
BANK1	DIFFI_B1_26P/GCLK9/PLL1_CLK10/PLL4_CLK2/PLL5_CLK2	H21	IO_58_P	87.2117	DQ3_B1/DQ3_B1_GATE_OUT
BANK1	DIFFI_B1_26N/GCLK8/PLL1_CLK11/PLL4_CLK3/PLL5_CLK3	H22	IO_58_N	88.3852	DQ3_B1/DQ3_B1_GATE_IN
BANK1	DIFFI_B1_27P/GCLK7/PLL2_CLK0/PLL3_CLK0	M20	IO_59_P	69.867	DQ4_B1
BANK1	DIFFI_B1_27N/GCLK6/PLL2_CLK1/PLL3_CLK1	L19	IO_59_N	69.3193	DQ4_B1
BANK1	DIFFI_B1_28P/GCLK5/PLL2_CLK2/PLL3_CLK2	J20	IO_60_P	88.1307	DQ4_B1
BANK1	DIFFI_B1_28N/GCLK4/PLL2_CLK3/PLL3_CLK3	J22	IO_60_N	84.6286	DQ4_B1
BANK1	DIFFI_B1_29P/ADR3	K21	IO_61_P	89.1012	DQ4_B1
BANK1	DIFFI_B1_29N/ADR2	K22	IO_61_N	76.5072	DQ4_B1
BANK1	DIFFI_B1_30P/ADR1	L20	IO_62_P	85.4676	DQS4_B1
BANK1	DIFFI_B1_30N/ADR0	L22	IO_62_N	90.7106	DQS4#_B1
BANK1	DIFFI_B1_31P/BFCS_N	M21	IO_63_P	68.252	DQ4_B1
BANK1	DIFFI_B1_31N/BFOE_N	M22	IO_63_N	71.1742	DQ4_B1
BANK1	DIFFI_B1_32P/BFWE_N	N20	IO_64_P	91.026	DQ4_B1
BANK1	DIFFI_B1_32N/BLDC	N22	IO_64_N	88.2231	DQ4_B1
BANK1	DIFFI_B1_33P/BHDC	P21	IO_65_P	72.2235	DQ5_B1/DQ4_B1_GATE_OUT
BANK1	DIFFI_B1_33N	P22	IO_65_N	81.3298	DQ5_B1/DQ4_B1_GATE_IN
BANK1	DIFFI_B1_34P	R20	IO_66_P	80.43	DQ5_B1
BANK1	DIFFI_B1_34N	R22	IO_66_N	85.8943	DQ5_B1
BANK1	DIFFI_B1_35P	T21	IO_67_P	82.9593	DQS5_B1
BANK1	DIFFI_B1_35N	T22	IO_67_N	85.3188	DQS5#_B1
BANK1	DIFFI_B1_36P	U20	IO_68_P	115.895	DQ5_B1
BANK1	DIFFI_B1_36N	U22	IO_68_N	115.359	DQ5_B1
BANK1	DIFFI_B1_37P	V21	IO_69_P	82.0006	DQ5_B1
BANK1	DIFFI_B1_37N	V22	IO_69_N	102.953	DQ5_B1
BANK1	DIFFI_B1_38P	M19	IO_70_P	63.5057	DQ5_B1

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
BANK1	DIFFI_B1_38N/VREF_B1	N19	IO_70_N	60.6114	DQ5_B1
BANK1	DIFFI_B1_39P	K16	IO_71_P	179.221	DQ5_B1/DQ5_B1_GATE_OUT
BANK1	DIFFI_B1_39N	J16	IO_71_N	177.941	DQ5_B1/DQ5_B1_GATE_IN
BANK1	DIFFI_B1_40P	M16	IO_72_P	84.8814	DQ6_B1/DQ6_B1_GATE_OUT
BANK1	DIFFI_B1_40N	L15	IO_72_N	90.2123	DQ6_B1/DQ6_B1_GATE_IN
BANK1	DIFFI_B1_41P	P19	IO_73_P	78.8505	DQ6_B1
BANK1	DIFFI_B1_41N	P20	IO_73_N	80.0318	DQ6_B1
BANK1	DIFFI_B1_42P	W20	IO_74_P	110.84	DQS6_B1
BANK1	DIFFI_B1_42N	W22	IO_74_N	111.327	DQS6#_B1
BANK1	DIFFI_B1_43P	L17	IO_75_P	147.282	DQ6_B1
BANK1	DIFFI_B1_43N	K18	IO_75_N	131.85	DQ6_B1
BANK1	DIFFI_B1_51P	U19	IO_83_P	87.1736	DQ7_B1
BANK1	DIFFI_B1_51N	V20	IO_83_N	86.257	DQ7_B1
BANK1	DIFFI_B1_52P	M17	IO_84_P	66.7568	DQ7_B1
BANK1	DIFFI_B1_52N	M18	IO_84_N	79.1252	DQ7_B1
BANK1	DIFFI_B1_53P	P17	IO_85_P	74.2957	
BANK1	DIFFI_B1_53N	N16	IO_85_N	73.4907	
BANK1	DIFFI_B1_54P	P18	IO_86_P	66.3355	
BANK1	DIFFI_B1_54N	R19	IO_86_N	66.0896	
BANK1	DIFFI_B1_55P	T19	IO_87_P	78.555	
BANK1	DIFFI_B1_55N/DOUT_BUSY	T20	IO_87_N	74.8189	
BANK2	DIFFIO_B2_1N/CSO_N	T5	IO_89_N	56.8989	
BANK2	DIFFIO_B2_1P/INIT_FLAG_N	T6	IO_89_P	60.9934	
BANK2	DIFFIO_B2_2N/D9	AB2	IO_90_N	91.8971	
BANK2	DIFFIO_B2_2P/D8	AA2	IO_90_P	99.1211	
BANK2	DIFFIO_B2_3N	V5	IO_91_N	62.6312	
BANK2	DIFFIO_B2_3P	U6	IO_91_P	61.2485	
BANK2	DIFFIO_B2_4N/D6	Y4	IO_92_N	77.3372	
BANK2	DIFFIO_B2_4P/D5	W4	IO_92_P	80.8263	
BANK2	DIFFIO_B2_5N	R7	IO_93_N	87.1706	

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
BANK2	DIFFIO_B2_5P	T7	IO_93_P	87.9132	
BANK2	DIFFIO_B2_6N	R8	IO_94_N	77.9049	
BANK2	DIFFIO_B2_6P	R9	IO_94_P	79.9753	
BANK2	DIFFIO_B2_7N	AB3	IO_95_N	111.541	
BANK2	DIFFIO_B2_7P	Y3	IO_95_P	111.053	
BANK2	DIFFIO_B2_8N	AB4	IO_96_N	79.0614	
BANK2	DIFFIO_B2_8P	AA4	IO_96_P	84.6046	
BANK2	DIFFIO_B2_9N	AB5	IO_97_N	96.6234	
BANK2	DIFFIO_B2_9P	Y5	IO_97_P	95.1048	
BANK2	DIFFIO_B2_10N	Y6	IO_98_N	54.9821	
BANK2	DIFFIO_B2_10P	W6	IO_98_P	72.8847	
BANK2	DIFFIO_B2_11N	U10	IO_99_N	89.058	
BANK2	DIFFIO_B2_11P	T10	IO_99_P	89.8228	
BANK2	DIFFIO_B2_12N	U8	IO_100_N	73.2441	
BANK2	DIFFIO_B2_12P	T8	IO_100_P	72.9202	
BANK2	DIFFIO_B2_13N	V9	IO_101_N	63.5182	
BANK2	DIFFIO_B2_13P	U9	IO_101_P	67.19	
BANK2	DIFFIO_B2_14N/D4	AB6	IO_102_N	81.2523	
BANK2	DIFFIO_B2_14P/D3	AA6	IO_102_P	91.7538	
BANK2	DIFFIO_B2_15N/RWSEL/VREF_B2	AB7	IO_103_N	88.9763	
BANK2	DIFFIO_B2_15P/D7	Y7	IO_103_P	88.5269	
BANK2	DIFFIO_B2_16N	Y8	IO_104_N	69.838	
BANK2	DIFFIO_B2_16P	W9	IO_104_P	69.5315	
BANK2	DIFFIO_B2_17N	V7	IO_105_N	86.0799	
BANK2	DIFFIO_B2_17P	W8	IO_105_P	84.0484	
BANK2	DIFFIO_B2_18N	AB8	IO_106_N	70.0767	
BANK2	DIFFIO_B2_18P	AA8	IO_106_P	84.2483	
BANK2	DIFFIO_B2_19N	Y10	IO_107_N	55.7749	
BANK2	DIFFIO_B2_19P	W10	IO_107_P	68.8234	

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
BANK2	DIFFIO_B2_20N	AB9	IO_108_N	81.9347	
BANK2	DIFFIO_B2_20P	Y9	IO_108_P	81.9811	
BANK2	DIFFIO_B2_21N	W11	IO_109_N	59.9929	
BANK2	DIFFIO_B2_21P	V11	IO_109_P	52.0848	
BANK2	DIFFIO_B2_22N/VREF_B2	AB10	IO_110_N	69.5791	
BANK2	DIFFIO_B2_22P	AA10	IO_110_P	81.3009	
BANK2	DIFFIO_B2_23N	T11	IO_111_N	91.2557	
BANK2	DIFFIO_B2_23P	R11	IO_111_P	92.2329	
BANK2	DIFFIO_B2_24N/GCLK28/PLL4_CLK4/PLL5_CLK4	AB11	IO_112_N	81.1514	
BANK2	DIFFIO_B2_24P/GCLK29/PLL4_CLK5/PLL5_CLK5	Y11	IO_112_P	76.7782	
BANK2	DIFFIO_B2_25N/GCLK30/PLL4_CLK6/PLL5_CLK6/D15	AB12	IO_113_N	68.697	
BANK2	DIFFIO_B2_25P/GCLK31/PLL4_CLK7/PLL5_CLK7/D14	AA12	IO_113_P	70.6855	
BANK2	DIFFIO_B2_26N/GCLK0/PLL4_CLK8/PLL5_CLK8/ECCLK	AB13	IO_114_N	84.036	
BANK2	DIFFIO_B2_26P/GCLK1/PLL4_CLK9/PLL5_CLK9/D13	Y13	IO_114_P	81.9013	
BANK2	DIFFIO_B2_27N/GCLK2/PLL4_CLK10/PLL5_CLK10	Y12	IO_115_N	43.4088	
BANK2	DIFFIO_B2_27P/GCLK3/PLL4_CLK11/PLL5_CLK11	W12	IO_115_P	65.1903	
BANK2	DIFFIO_B2_28N	R13	IO_116_N	81.5643	
BANK2	DIFFIO_B2_28P	T14	IO_116_P	84.0391	
BANK2	DIFFIO_B2_29N	U12	IO_117_N	69.8791	
BANK2	DIFFIO_B2_29P	T12	IO_117_P	70.3294	
BANK2	DIFFIO_B2_30N	AB15	IO_118_N	84.8778	
BANK2	DIFFIO_B2_30P	Y15	IO_118_P	72.6915	
BANK2	DIFFIO_B2_31N	Y14	IO_119_N	76.7328	
BANK2	DIFFIO_B2_31P	W14	IO_119_P	76.0111	
BANK2	DIFFIO_B2_32N	AB16	IO_120_N	74.5711	
BANK2	DIFFIO_B2_32P	AA16	IO_120_P	73.1231	
BANK2	DIFFIO_B2_33N	W13	IO_121_N	67.8445	

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
BANK2	DIFFIO_B2_33P	V13	IO_121_P	67.1904	
BANK2	DIFFIO_B2_34N	W15	IO_122_N	72.9866	
BANK2	DIFFIO_B2_34P	Y16	IO_122_P	73.5064	
BANK2	DIFFIO_B2_35N/VREF_B2	AB14	IO_123_N	70.1697	
BANK2	DIFFIO_B2_35P	AA14	IO_123_P	71.7709	
BANK2	DIFFIO_B2_36N	AB17	IO_124_N	89.4056	
BANK2	DIFFIO_B2_36P	Y17	IO_124_P	90.0256	
BANK2	DIFFIO_B2_37N/D12	AB18	IO_125_N	102.779	
BANK2	DIFFIO_B2_37P/D11	AA18	IO_125_P	101.686	
BANK2	DIFFIO_B2_38N/D10	V15	IO_126_N	40.2982	
BANK2	DIFFIO_B2_38P/MODE_1	U15	IO_126_P	39.0253	
BANK2	DIFFIO_B2_39N/D2	U13	IO_127_N	63.6929	
BANK2	DIFFIO_B2_39P/D1	U14	IO_127_P	71.3165	
BANK2	DIFFIO_B2_40N	W17	IO_128_N	86.2373	
BANK2	DIFFIO_B2_40P	V17	IO_128_P	85.593	
BANK2	DIFFIO_B2_41N	R15	IO_129_N	99.6767	
BANK2	DIFFIO_B2_41P	R16	IO_129_P	99.0962	
BANK2	DIFFIO_B2_42N	V18	IO_130_N	97.7301	
BANK2	DIFFIO_B2_42P	V19	IO_130_P	98.9351	
BANK2	DIFFIO_B2_43N	U16	IO_131_N	92.1406	
BANK2	DIFFIO_B2_43P	U17	IO_131_P	93.7584	
BANK2	DIFFIO_B2_44N	T15	IO_132_N	61.7782	
BANK2	DIFFIO_B2_44P	T16	IO_132_P	62.0335	
BANK2	DIFFIO_B2_45N	Y18	IO_133_N	92.5666	
BANK2	DIFFIO_B2_45P	W18	IO_133_P	90.1973	
BANK2	DIFFIO_B2_46N	AB19	IO_134_N	98.7624	
BANK2	DIFFIO_B2_46P	Y19	IO_134_P	97.6973	

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
BANK2	DIFFIO_B2_47N/VREF_B2	T17	IO_135_N	99.8127	
BANK2	DIFFIO_B2_47P	T18	IO_135_P	100.892	
BANK2	DIFFIO_B2_52N/CS_N	AB20	IO_140_N	80.2558	
BANK2	DIFFIO_B2_52P/D0	AA20	IO_140_P	97.9918	
BANK2	DIFFIO_B2_53N	AB21	IO_141_N	84.0983	
BANK2	DIFFIO_B2_53P	AA21	IO_141_P	103.517	
BANK2	DIFFIO_B2_54N/MODE_0	AA22	IO_142_N	98.8402	
BANK2	DIFFIO_B2_54P/CFG_CLK	Y21	IO_142_P	98.4376	
BANK3	DIFFI_B3_0N/VREF_B3	B3	IO_143_N	98.0256	DQ0_B3/DQ0_B3_GATE_IN
BANK3	DIFFI_B3_0P	A2	IO_143_P	99.0397	DQ0_B3/DQ0_B3_GATE_OUT
BANK3	DIFFI_B3_1N	E6	IO_144_N	60.1638	DQ0_B3
BANK3	DIFFI_B3_1P	E5	IO_144_P	62.6194	DQ0_B3
BANK3	DIFFI_B3_2N	C4	IO_145_N	80.5792	DQ0_B3
BANK3	DIFFI_B3_2P	D3	IO_145_P	70.5277	DQ0_B3
BANK3	DIFFI_B3_3N	F7	IO_146_N	50.4586	DQ0_B3
BANK3	DIFFI_B3_3P	G7	IO_146_P	49.7319	DQ0_B3
BANK3	DIFFI_B3_11N	B1	IO_154_N	110.27	DQ1_B3
BANK3	DIFFI_B3_11P	B2	IO_154_P	113.573	DQ1_B3
BANK3	DIFFI_B3_12N	H8	IO_155_N	81.32	DQ1_B3
BANK3	DIFFI_B3_12P	J7	IO_155_P	80.6092	DQ1_B3
BANK3	DIFFI_B3_13N/VREF_B3	K8	IO_156_N	99.8479	DQ2_B3
BANK3	DIFFI_B3_13P	K7	IO_156_P	100.332	DQ2_B3
BANK3	DIFFI_B3_14N	F5	IO_157_N	74.3619	DQ2_B3
BANK3	DIFFI_B3_14P	G6	IO_157_P	67.5943	DQ2_B3
BANK3	DIFFI_B3_15N	C1	IO_158_N	121.175	DQS2#_B3
BANK3	DIFFI_B3_15P	C3	IO_158_P	122.036	DQS2_B3
BANK3	DIFFI_B3_16N	D1	IO_159_N	83.2114	DQ2_B3

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
BANK3	DIFFI_B3_16P	D2	IO_159_P	82.9481	DQ2_B3
BANK3	DIFFI_B3_17N	E1	IO_160_N	97.7786	DQ2_B3
BANK3	DIFFI_B3_17P	E3	IO_160_P	99.8024	DQ2_B3
BANK3	DIFFI_B3_18N	F3	IO_161_N	75.0394	DQ2_B3
BANK3	DIFFI_B3_18P	G4	IO_161_P	65.9223	DQ2_B3
BANK3	DIFFI_B3_19N	F1	IO_162_N	80.8327	DQ2_B3/DQ2_B3_GATE_IN
BANK3	DIFFI_B3_19P	F2	IO_162_P	79.4457	DQ2_B3/DQ2_B3_GATE_OUT
BANK3	DIFFI_B3_20N	H5	IO_163_N	60.0411	DQ3_B3/DQ3_B3_GATE_IN
BANK3	DIFFI_B3_20P	H6	IO_163_P	47.3795	DQ3_B3/DQ3_B3_GATE_OUT
BANK3	DIFFI_B3_21N	G1	IO_164_N	86.5729	DQ3_B3
BANK3	DIFFI_B3_21P	G3	IO_164_P	86.9152	DQ3_B3
BANK3	DIFFI_B3_22N	H1	IO_165_N	81.9004	DQ3_B3
BANK3	DIFFI_B3_22P	H2	IO_165_P	73.0581	DQ3_B3
BANK3	DIFFI_B3_23N	H3	IO_166_N	87.0884	DQ3_B3
BANK3	DIFFI_B3_23P	H4	IO_166_P	79.8949	DQ3_B3
BANK3	DIFFI_B3_24N	J6	IO_167_N	42.9881	DQS3#_B3
BANK3	DIFFI_B3_24P	K6	IO_167_P	54.1565	DQS3_B3
BANK3	DIFFI_B3_25N/GCLK20/PLL1_CLK12/PLL4_CLK4/PLL5_CLK4	J4	IO_168_N	68.6537	DQ3_B3
BANK3	DIFFI_B3_25P/GCLK21/PLL1_CLK13/PLL4_CLK5/PLL5_CLK5	K3	IO_168_P	76.7351	DQ3_B3
BANK3	DIFFI_B3_26N/GCLK22/PLL1_CLK14/PLL4_CLK6/PLL5_CLK6	K4	IO_169_N	52.4439	DQ3_B3/DQ4_B3_GATE_IN
BANK3	DIFFI_B3_26P/GCLK23/PLL1_CLK15/PLL4_CLK7/PLL5_CLK7	K5	IO_169_P	55.2598	DQ3_B3/DQ4_B3_GATE_OUT
BANK3	DIFFI_B3_27N/GCLK24/PLL2_CLK4/PLL3_CLK4	L4	IO_170_N	63.6515	DQ4_B3
BANK3	DIFFI_B3_27P/GCLK25/PLL2_CLK5/PLL3_CLK5/TRDY2	M3	IO_170_P	68.918	DQ4_B3
BANK3	DIFFI_B3_28N/GCLK26/PLL2_CLK6/PLL3_CLK6	J1	IO_171_N	76.4229	DQ4_B3
BANK3	DIFFI_B3_28P/GCLK27/PLL2_CLK7/PLL3_CLK7	J3	IO_171_P	87.5878	DQ4_B3
BANK3	DIFFI_B3_29N	K1	IO_172_N	79.348	DQ4_B3
BANK3	DIFFI_B3_29P	K2	IO_172_P	82.0541	DQ4_B3

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
BANK3	DIFFI_B3_30N	L1	IO_173_N	80.7228	DQS4#_B3
BANK3	DIFFI_B3_30P	L3	IO_173_P	82.0814	DQS4_B3
BANK3	DIFFI_B3_31N	M1	IO_174_N	65.7038	DQ4_B3
BANK3	DIFFI_B3_31P	M2	IO_174_P	65.5065	DQ4_B3
BANK3	DIFFI_B3_32N	N1	IO_175_N	79.8739	DQ4_B3
BANK3	DIFFI_B3_32P	N3	IO_175_P	80.1058	DQ4_B3
BANK3	DIFFI_B3_33N	P1	IO_176_N	83.5255	DQ5_B3
BANK3	DIFFI_B3_33P	P2	IO_176_P	78.6957	DQ5_B3
BANK3	DIFFI_B3_34N	R1	IO_177_N	111.347	DQ5_B3
BANK3	DIFFI_B3_34P	R3	IO_177_P	113.007	DQ5_B3
BANK3	DIFFI_B3_35N	T1	IO_178_N	78.3968	DQS5#_B3
BANK3	DIFFI_B3_35P	T2	IO_178_P	71.41	DQS5_B3
BANK3	DIFFI_B3_36N	U1	IO_179_N	111.577	DQ5_B3
BANK3	DIFFI_B3_36P	U3	IO_179_P	113.322	DQ5_B3
BANK3	DIFFI_B3_37N	V1	IO_180_N	85.0472	DQ5_B3
BANK3	DIFFI_B3_37P	V2	IO_180_P	104.566	DQ5_B3
BANK3	DIFFI_B3_38N/VREF_B3	M4	IO_181_N	64.8419	DQ5_B3
BANK3	DIFFI_B3_38P	M5	IO_181_P	68.4335	DQ5_B3
BANK3	DIFFI_B3_39N	E4	IO_182_N	165.528	DQ5_B3/DQ5_B3_GATE_IN
BANK3	DIFFI_B3_39P	D5	IO_182_P	168.057	DQ5_B3/DQ5_B3_GATE_OUT
BANK3	DIFFI_B3_40N	N4	IO_183_N	73.7966	DQ6_B3/DQ6_B3_GATE_IN
BANK3	DIFFI_B3_40P	P3	IO_183_P	74.9614	DQ6_B3/DQ6_B3_GATE_OUT
BANK3	DIFFI_B3_41N	L6	IO_184_N	80.7069	DQ6_B3
BANK3	DIFFI_B3_41P	M6	IO_184_P	86.8712	DQ6_B3
BANK3	DIFFI_B3_42N	P4	IO_185_N	62.3998	DQ6_B3
BANK3	DIFFI_B3_42P	R4	IO_185_P	61.8486	DQ6_B3
BANK3	DIFFI_B3_45N	M8	IO_188_N	105.952	DQ6_B3

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
BANK3	DIFFI_B3_45P	M7	IO_188_P	99.9988	DQ6_B3
BANK3	DIFFI_B3_51N	N7	IO_194_N	87.1149	DQ7_B3
BANK3	DIFFI_B3_51P	N6	IO_194_P	86.1494	DQ7_B3
BANK3	DIFFI_B3_52N	V3	IO_195_N	77.4253	DQ7_B3
BANK3	DIFFI_B3_52P	U4	IO_195_P	77.1288	DQ7_B3
BANK3	DIFFI_B3_53N	T3	IO_196_N	49.7283	DQ8_B3
BANK3	DIFFI_B3_53P	T4	IO_196_P	66.5023	DQ8_B3
BANK3	DIFFI_B3_54N	P5	IO_197_N	60.9673	DQ8_B3
BANK3	DIFFI_B3_54P	P6	IO_197_P	60.4052	DQ8_B3
BANK3	DIFFI_B3_55N	P7	IO_198_N	71.4302	DQS8#_B3
BANK3	DIFFI_B3_55P	P8	IO_198_P	74.9919	DQS8_B3
BANK3	DIFFI_B3_56N	W1	IO_199_N	93.5804	DQ8_B3
BANK3	DIFFI_B3_56P	W3	IO_199_P	95.6811	DQ8_B3
BANK3	DIFFI_B3_57N/VREF_B3	Y1	IO_200_N	93.6709	DQ8_B3
BANK3	DIFFI_B3_57P	Y2	IO_200_P	92.5373	DQ8_B3
BANK2	CFG_DONE	Y22		95.0627	
BANK2	CMPCS_B	Y20		88.9877	
BANK2	RST_N	AA1		88.331	
	STAND_BY	N15		103.269	
	TCK	G15		48.5298	
	TDI	E18		64.9325	
	TDO	A19		94.268	
	TMS	C18		69.0055	
	VCC	J8			
	VCC	J10			
	VCC	J12			
	VCC	J14			
	VCC	K9			
	VCC	K11			
	VCC	K13			
	VCC	L10			
	VCC	L12			

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
	VCC	L14			
	VCC	M9			
	VCC	M11			
	VCC	M13			
	VCC	N10			
	VCC	N12			
	VCC	N14			
	VCC	P9			
	VCC	P11			
	VCC	P13			
	VCC	R14			
	VCCAUX	D16			
	VCCAUX	F11			
	VCCAUX	G12			
	VCCAUX	H9			
	VCCAUX	H15			
	VCCAUX	K15			
	VCCAUX	L8			
	VCCAUX	M15			
	VCCAUX	N8			
	VCCAUX	R6			
	VCCAUX	R10			
	VCCAUX	R12			
	VCCAUX	U11			
	VCCAUX	V6			
	VCCIO0	B4			
	VCCIO0	B7			
	VCCIO0	B11			
	VCCIO0	B15			
	VCCIO0	B19			
	VCCIO0	E9			
	VCCIO0	E13			
	VCCIO0	E17			
	VCCIO0	G10			
	VCCIO0	G14			
	VCCIO1	C21			
	VCCIO1	E19			

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
	VCCIO1	G21			
	VCCIO1	J18			
	VCCIO1	L16			
	VCCIO1	L21			
	VCCIO1	N18			
	VCCIO1	R21			
	VCCIO1	U18			
	VCCIO1	W21			
	VCCIO2	T9			
	VCCIO2	T13			
	VCCIO2	V8			
	VCCIO2	V12			
	VCCIO2	V16			
	VCCIO2	W5			
	VCCIO2	AA3			
	VCCIO2	AA7			
	VCCIO2	AA11			
	VCCIO2	AA15			
	VCCIO2	AA19			
	VCCIO3	C2			
	VCCIO3	F4			
	VCCIO3	F6			
	VCCIO3	G2			
	VCCIO3	J5			
	VCCIO3	L2			
	VCCIO3	L7			
	VCCIO3	N5			
	VCCIO3	R2			
	VCCIO3	U5			
	VCCIO3	W2			
	VCCEFUSE	M14			
	VSS	A1			
	VSS	A22			
	VSS	B5			
	VSS	B9			

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
	VSS	B13			
	VSS	B17			
	VSS	D4			
	VSS	D18			
	VSS	E2			
	VSS	E7			
	VSS	E11			
	VSS	E15			
	VSS	E21			
	VSS	G5			
	VSS	G18			
	VSS	H7			
	VSS	J2			
	VSS	J9			
	VSS	J11			
	VSS	J13			
	VSS	J15			
	VSS	J21			
	VSS	K10			
	VSS	K12			
	VSS	K14			
	VSS	L5			
	VSS	L9			
	VSS	L11			
	VSS	L13			
	VSS	L18			
	VSS	M10			
	VSS	M12			
	VSS	N2			
	VSS	N9			
	VSS	N11			
	VSS	N13			
	VSS	N17			
	VSS	N21			
	VSS	P10			
	VSS	P12			
	VSS	P14			

Bank Name	Pin Name(Function name)	Pin #	Differential Pair	Time Delay (ps)	DQS Grouping
	VSS	R5			
	VSS	R18			
	VSS	U2			
	VSS	U7			
	VSS	U21			
	VSS	V4			
	VSS	V10			
	VSS	V14			
	VSS	W7			
	VSS	W16			
	VSS	W19			
	VSS	AA5			
	VSS	AA9			
	VSS	AA13			
	VSS	AA17			
	VSS	AB1			
	VSS	AB22			
	NC	E8			
	NC	F8			
	NC	F9			
	NC	F14			
	NC	G8			
	NC	H14			
	NC	P15			
	NC	P16			
	NC	R17			

Chapter 5 Thermal Resistance

Table 5-1 Thermal Resistance

θJA(°C/W) (Flow: 0m/s)	**θJB (°C/W)**	**θJC (°C/W)**	**θJA(°C/W) (Flow: 1m/s)**	**θJA(°C/W) (Flow: 2m/s)**
16.7	10.3	6.3	14.6	13.3

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