Logos2 Family FPGAs Clock Resources (Clock) User Guide

(UG040004, V1.2)

(31.07.2023)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	31.07.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
USCM	User Select Clock Mux
SRB	Signal Relay Block
HCKB	Horizontal Clock Buffer
RCKB	Regional Clock Buffer
MRCKB	Multi-Region Clock Buffer
GMCLK	Global Multiplex Clock
GSCLK	Global Single Clock
GTP	General Technology Primitive

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Chapter 1 General Introduction

This document introduces the Logos2 Family devices' clock resources, as well as the applications and features of general PLLs. Herein, the clock resources consists of dedicated clock pin resources, clock network resources, clock buffer resources, and clock GTP resources. The general PLLs cover GPLLs and PPLLs.

For the default values of the GTP parameters in this document, please refer to the "***UG040007_Logos2 Family Product GTP User Guide***".

1.1 Clock Resources Overview

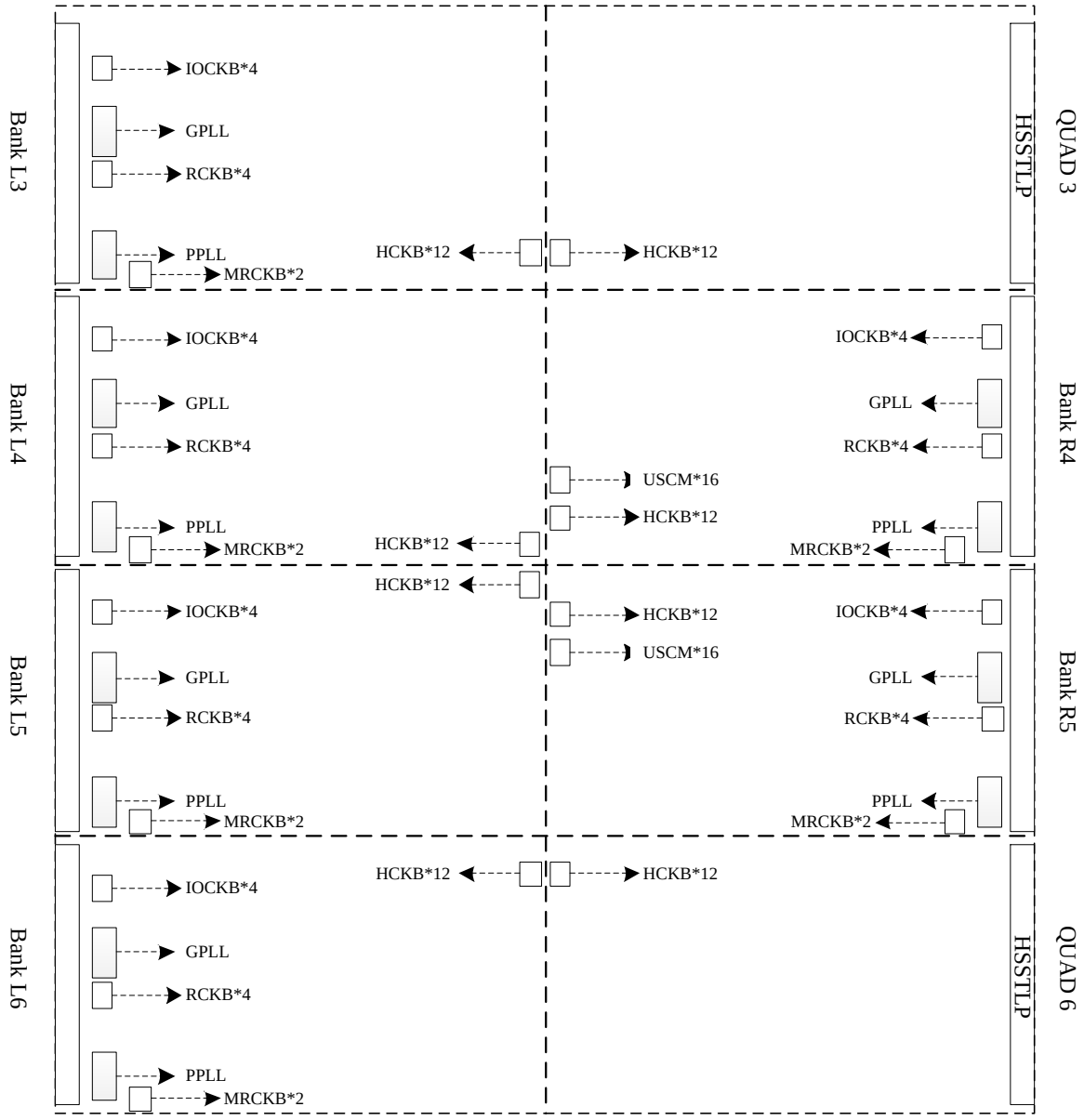

Figure 1-1 PG2L100H Clock Resources Diagram

The Logos2 Family products provide extensive on-chip clock resources. The clock resources for the PG2L100H are illustrated in the above diagram, which include 32 GLOBAL CLKs. The entire device is divided into upper and lower parts, each with 16 separated GLOBAL CLK networks. The whole device is divided into multiple regions based on the region-specific concept of REGIONAL CLKs. Except for the location bank of HSSTLP, each region has 4 REGIONAL CLK networks and 4 IO CLK networks. IOCLK is designated for high-speed interface applications. Additionally, HORIZONTAL CLK networks for horizontally adjacent clock regions and multi-region clock networks for vertically adjacent clock regions are also available.

The overall chip clock resources are shown below:

- The PG2L100H chip has 32 GLOBAL CLOCKs, with 16 separate clocks respectively assigned to the upper part and lower part.
- Apart from the two regions housing of HSST, each region has 4 REGION CLOCKs, totalling 24 REGION CLOCKs in the PG2L100H chip.
- The PG2L100H chip has 96 HORIZONTAL CLOCKs, with 12 allocated to each region.
- The PG2L100H chip has 24 IO CLOCKs, with 4 in each IO bank.

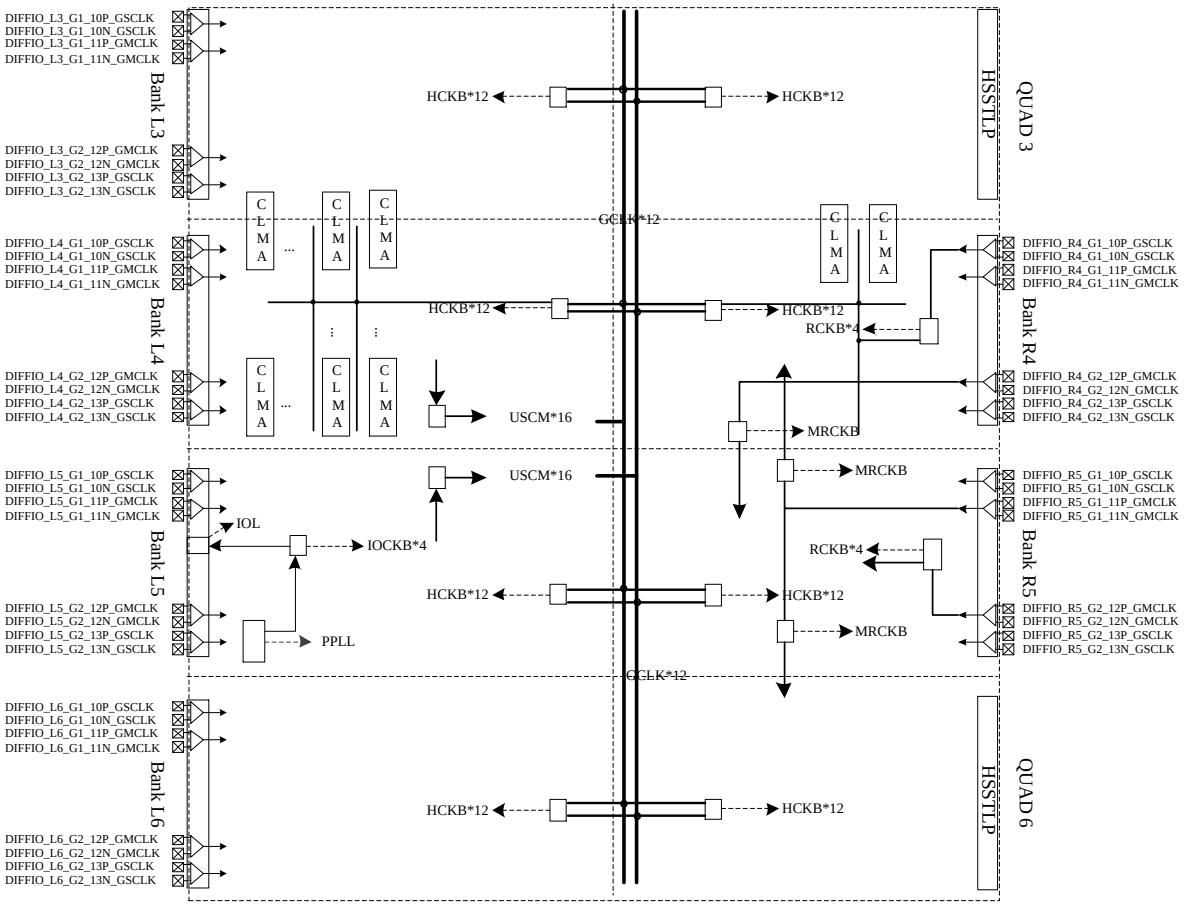

Figure 1-2 PG2L100H Clock Architecture Diagram

The clock architecture of PG2L100H is depicted in the above figure, which also applies to other devices, but the number of regions and resources may vary. The GLOBAL CLOCKs vertically driven by USCMs provides the synchronous clock sources for the synchronous logic unit on the chip. 16 USCMs are situated in the upper half of the chip, while another 16 USCMs are located in the lower half.

It can be seen from above that the clocks of users can access the following domains via the clock pins:

- USCMs in the same upper/lower half region
- HCKBs within the same or adjacent horizontal regions, enabling the accessibility to the clock networks in the same region
- Regional clock networks are accessible through connection to RCKBs within the same region
- MRCKBs within the same region (only supporting input clock pin GMCLK) serve as the clock sources for the current clock regions and the verticvally adjacent regions.
- Clocks are provided for IOLs within the same region by establishing connection to IOCKBs in the same region.

1.2 Clock Connection Overview

The following table summarizes the Logos2 Family FPGAs clock pins, as well as the input clock sources and output direct drive resources of various clock buffers. The determination of relevant constraints and information of the characteristics of all clock resources help us optimize clock planning and FPGA designs.

Table 1-1 Clock Connection Overview

Clock Buffers/Pins	Input Clock Sources	Output Direct Drive Resources
GMCLK, with two pairs of differential inputs in each IO bank	External clock source	Same region: • RCKB • IOCKB • MRCKB Same or adjacent horizontal region: • HCKB Same left half or right half region: • One or more GPLLs/PPLLs Same upper half or lower half region: • USCM
GSCLK, with two pairs of differential inputs in each IO bank	External clock source	Same region: • RCKB • IOCKB Same or adjacent horizontal region: HCKB Same left half or right half region: • One or more GPLLs/PPLLs Same upper half or lower half region:

Clock Buffers/Pins	Input Clock Sources	Output Direct Drive Resources
		• USCM
USCM	Same upper half or lower half region: • GSCLK and GMCLK • GPLL and PPLL • HCKB (not supported for the region where HSSTLP is located) • RCKB • SRB (not recommended) • Adjacent USCM • HSSTLP (HSSTLP clock in this table)	• Drive GPLL/PPLL via HCKB • Adjacent USCM in the same half region • Any logic units with global clock pins • HSSTLP (HSSTLP clock in this table) • All HCKBs • CLMA control signals
HCKB	Same region and adjacent horizontal region: • GSCLK and GMCLK • PPLL and GPLL • HSSTLP (HSSTLP clock in this table) Entire chip: • USCM in the same upper/lower half region • SRB (not recommended)	Same region: • GPLL/PPLL • HSSTLP (HSSTLP clock in this table) • Any logic units with clock pins. • I/O logic (IOL) Same upper/lower half region: • USCM
RCKB	Same region: • GSCLK and GMCLK • PPLL and GPLL CLKOUT0~3/N • SRB Same and vertically adjacent regions: • MRCKB	Same region: • GPLL/PPLL Any logic units with clock pins • I/O logic (IOL) Same upper half or lower half region: • USCM
IOCKB	Same region: • GSCLK and GMCLK • PPLL and GPLL CLKOUT0~3/N Same and vertically adjacent regions: • MRCKB	Same region: • I/O logic (IOL)
MRCKB	Same region: • GMCLK • SRB	Same and vertically adjacent regions: • RCKB • IOCKB
GPLL/PPLL	• GMCLK and GSCLK in the same left or right half region • USCM in the same upper/lower half region • RCKB in the same region • HCKB in the same region • GPLL/PPLL CLKOUT0~3/N on the same left/right side	GPLL: CLKOUT0~3/N, CLKOUT4~6, CLKOUTF/CLKOUTFN: • USCM in the same half region and HCKB in the same or adjacent horizontal regions CLKOUT0~3: • RCKB and IOCKB in the same region PPLL: CLKOUT0/N, CLKOUT1~4, CLKOUTF/CLKOUTFN: • USCM in the same half region and HCKB in the same or adjacent horizontal regions CLKOUT0~3: • RCKB and IOCKB in the same region CLKOUTPHY/N:

Clock Buffers/Pins	Input Clock Sources	Output Direct Drive Resources
		• DDR PHY
HSSTLP input clock pin: P_TX_CLK_FR_CORE P_TCLK2_FR_CORE P_RX_CLK_FR_CORE P_RCLK2_FR_CORE	USCM in the same upper/lower half region HCKB in the same region	None
HSSTLP clock output pin: P_RCLK2FABRIC P_TCLK2FABRIC	None	• USCM in the same upper/lower half region • HCKB in the same region
HSSTLP reference clock: REFCLK_CML_P REFCLK_CML_N	External HSSTLP reference clock	• USCM in the same upper/lower half region • HCKB in the same region

Note: For HSSTLP clocks, please refer to the "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSST) User Guide***"

1.3 CLOCK REGION

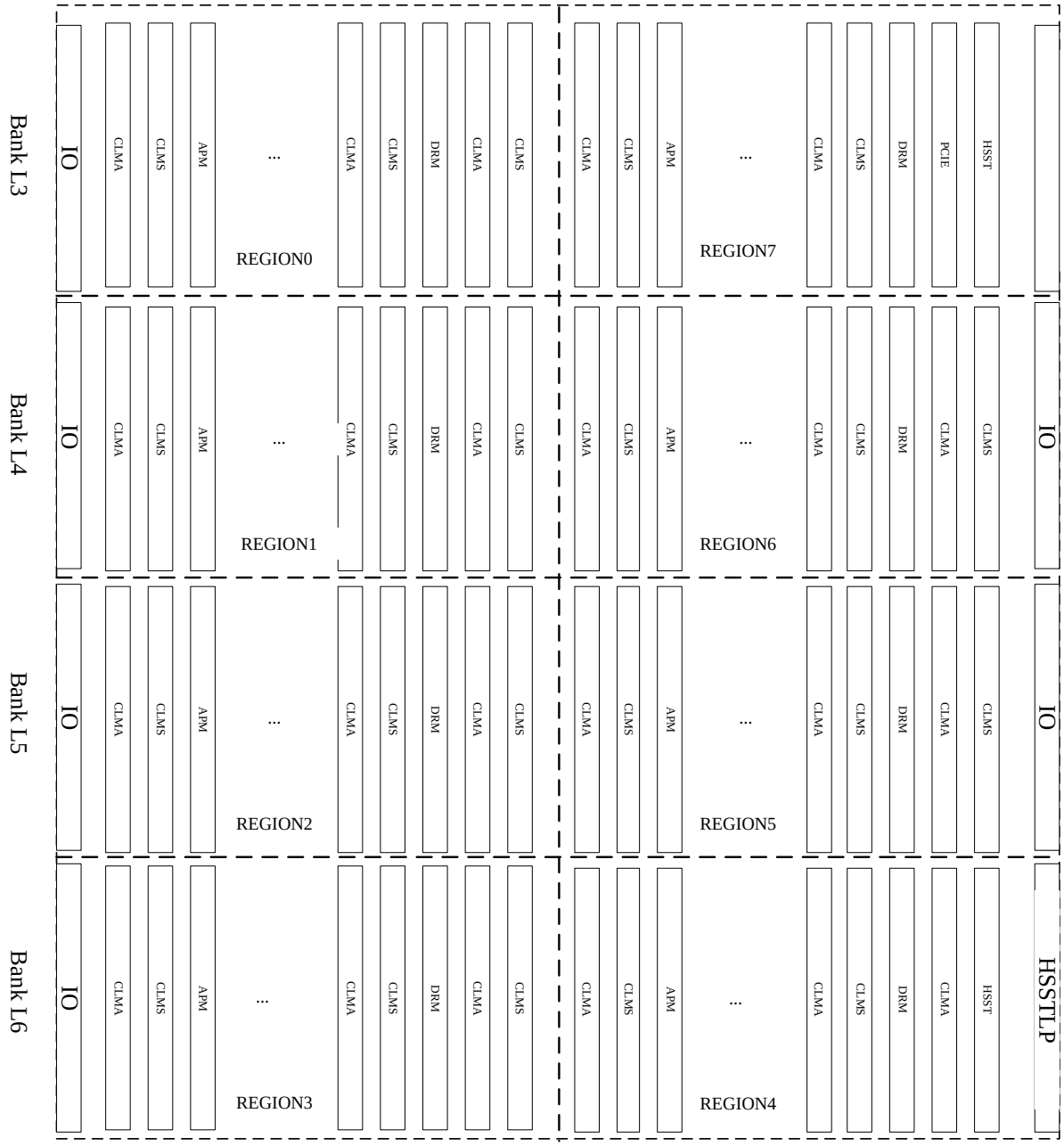

Figure 1-3 Clock Region Structure Diagram

The internal logic resources of the Logos2 Family products are distributed by region, each comprising a certain number of CLMA, CLMS, DRM, IO, and APM columns. The regions have a vertical height of about 50 CLMAs or CLMSs and 1 IO logic, while the horizontal widths vary according to the chip logic capacity. The PG2L100H consists of 8 regions as shown in the above diagram.

Chapter 2 Detailed Introduction

2.1 Clock Pin Resources

2.1.1 Clock Pin Introduction

The Logos2 Family products provide GSCLK/GMCLK IO pins with clock functions, two pairs of GMCLKs and two pairs of GSCLKs for users in each bank. It is recommended for users to prioritize selecting these clock pins as their clock inputs, as they can help avoid interferences caused by regular routing resources, resulting in improved clock performance. When not used as clock inputs, these clock input pins can still be taken as general IO.

GSCLK/GMCLK clock IO pins allow for differential or single-ended uses. GSCLK_P/GSCLK_N or GMCLK_P/GMCLK_N differential pair ports are required for differential signal applications. GSCLK_P or GMCLK_P single-ended ports are needed when applied to single-ended signals. In these cases, GSCLK_N/GMCLK_N are no longer regarded as clock ports but simply as general IO. The chip clock IO pin location diagram is shown as follows.

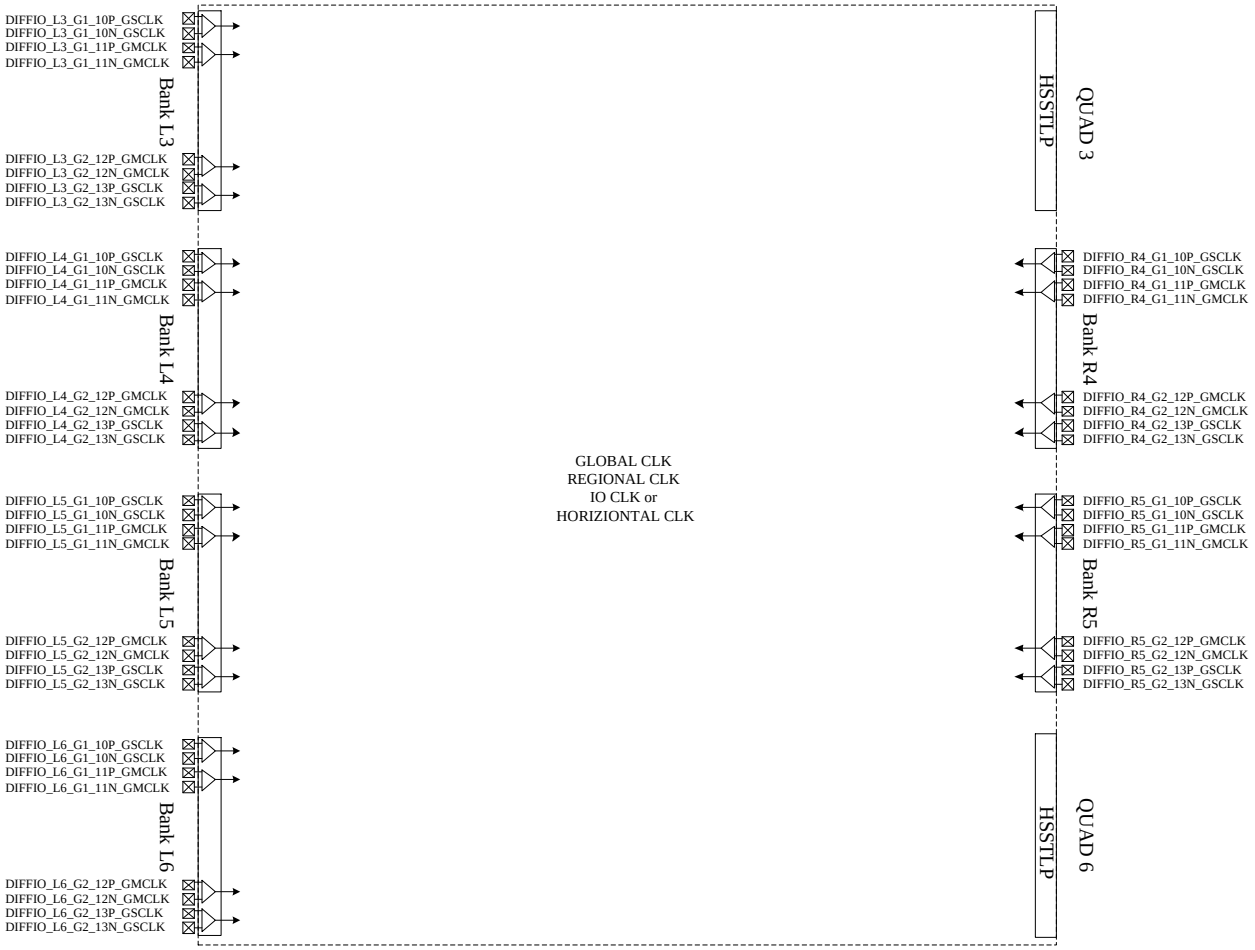

Figure 2-1 Clock Pin Location Diagram

It should be noted that GSCLK and GMCLK clock input pins are different in use. This is reflected in the fact that GMCLK can serve as a synchronous clock to drive vertically adjacent clock regions via MRCKB, while GSCLK cannot. The diagram below shows the connection between GSCLK and GMCLK pairs in BankL4..

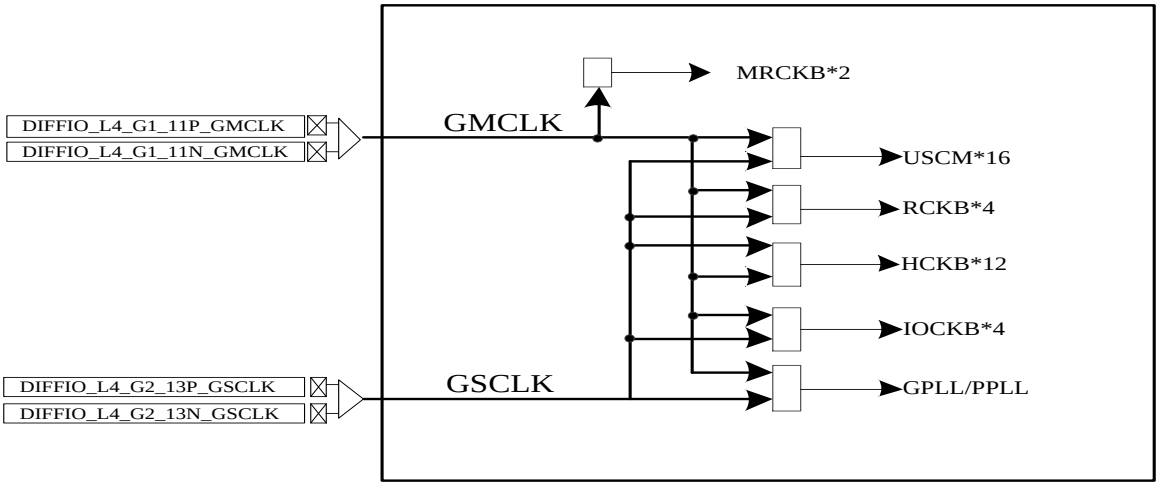

Figure 2-2 Clock Pin Connection Diagram

2.1.2 Clock Input Pin Placement Planning

The following main factors should be taken into considerations when selecting clock input pins:

- Ensure that the input clock pins connect to the desired clock network resources
- Ensure that the desired clock resources are available and not taken by other clock sources. If the expected input clock resources are occupied by GPLL output clocks, an error will occur when compiling the software

The specific placement rules for the input clock pins are shown in the table below:

Table 2-1 Input Clock Pin Placement Planning

Input Clock Connected To	**Clock Resource Usage and Placement Rules**	**Active Input Clock Pins**
I/O resources and logic resources of the entire chip	Input clock pins → USCM → Global clock tree • Clock pins must be located in the same upper or lower half region as USCM • Both the upper and lower half regions have 16 USCMs • Each region has 12 independent global clocks that share these clock networks with the horizontal clocks	GMCLK or GSCLK
I/O resources and HCKB drive logic resources for single region	Input clock pins → HCKB → Horizontal clock network • Clock pins must be placed in the same or adjacent horizontal regions as HCKB • Each region has 12 HCKBs and horizontal clock networks	GMCLK or GSCLK
I/O resources and GPLL/PPLL drive logic	Entire chip: • Input clock pins → GPLL/PPLL → USCM →	GMCLK or GSCLK

Input Clock Connected To	Clock Resource Usage and Placement Rules	Active Input Clock Pins
resources	Global clock tree Single region: • Input clock pins → GPLL/PPLL → RCKB → Regional clock tree Single or adjacent horizontal regions: • Input clock pins → GPLL/PPLL → HCKB → Horizontal clock network Routing rules for inputting clock to GPLL/PPLL: • Connect by PLL clock tree between the same left half regions or between the right half regions • Connect to GPLL/PPLL by USCM across left and right half regions, or by HCKB in the adjacent horizontal regions • Each region has 1 GPLL/PPLL except for the area housing HSSTLP	
I/O resources and RCKB drive logic resources for single region	Input clock pins → RCKB → Regional clock tree • The input clock pins must be located in the same region as the RCKB, I/O resources, and logic resources driven by this clock • Each region has 4 differential clock pin inputs and 4 RCKBs, except for the region of HSSTLP	GMCLK or GSCLK
I/O resources and MRCKB drive logic resources for adjacent three regions	Input clock pins → MRCKB → RCKB → Regional clock tree • The positioning of RCKB drive I/O resources and logic resources must be in the same or adjacent horizontal region as the input clock pin. • The placement of MRCKB drive RCKB must be in the same or adjacent horizontal region as the input clock pin. • Each region has 4 pairs of differential clock pin inputs, 4 RCKBs and 2 MRCKBs, except for the region of HSSTLP	Only GMCLK
High-speed interfaces in the same region	Input clock pins → IOCKB → I/O clock tree • The input clock pins must be located in the same region as the IOCKB and the driven IOL • Each region has 4 pairs of differential clock pin inputs, 4 IOCKBs and 2 MRCKBs, except for the region of HSSTLP	GMCLK or GSCLK
High-speed interfaces in the same and vertically adjacent regions	Input clock pins → MRCKB → IOCKB → I/O clock tree • The input clock pins must be located in the same or vertically adjacent regions as the IOCKB and the driven IOL • The placement of MRCKB drive IOCKB must be in the same or adjacent horizontal region as the input clock pin. • Each region has 4 pairs of differential clock pin inputs, 4 IOCKBs and 2 MRCKBs, except for the region of HSSTLP	Only GMCLK

2.2 Global Clock Resources

2.2.1 Global Clock Network

As a global clock driver, USCMs provide GCLK global clocks to the synchronous logic units in the clock regions. The global clock sources include GSCLK_P, GMCLK_P, PPLL, GPLL, HSST, HCKB, RCKB, SRB and other clocks. The USCM connection is shown in the dashed circle below.

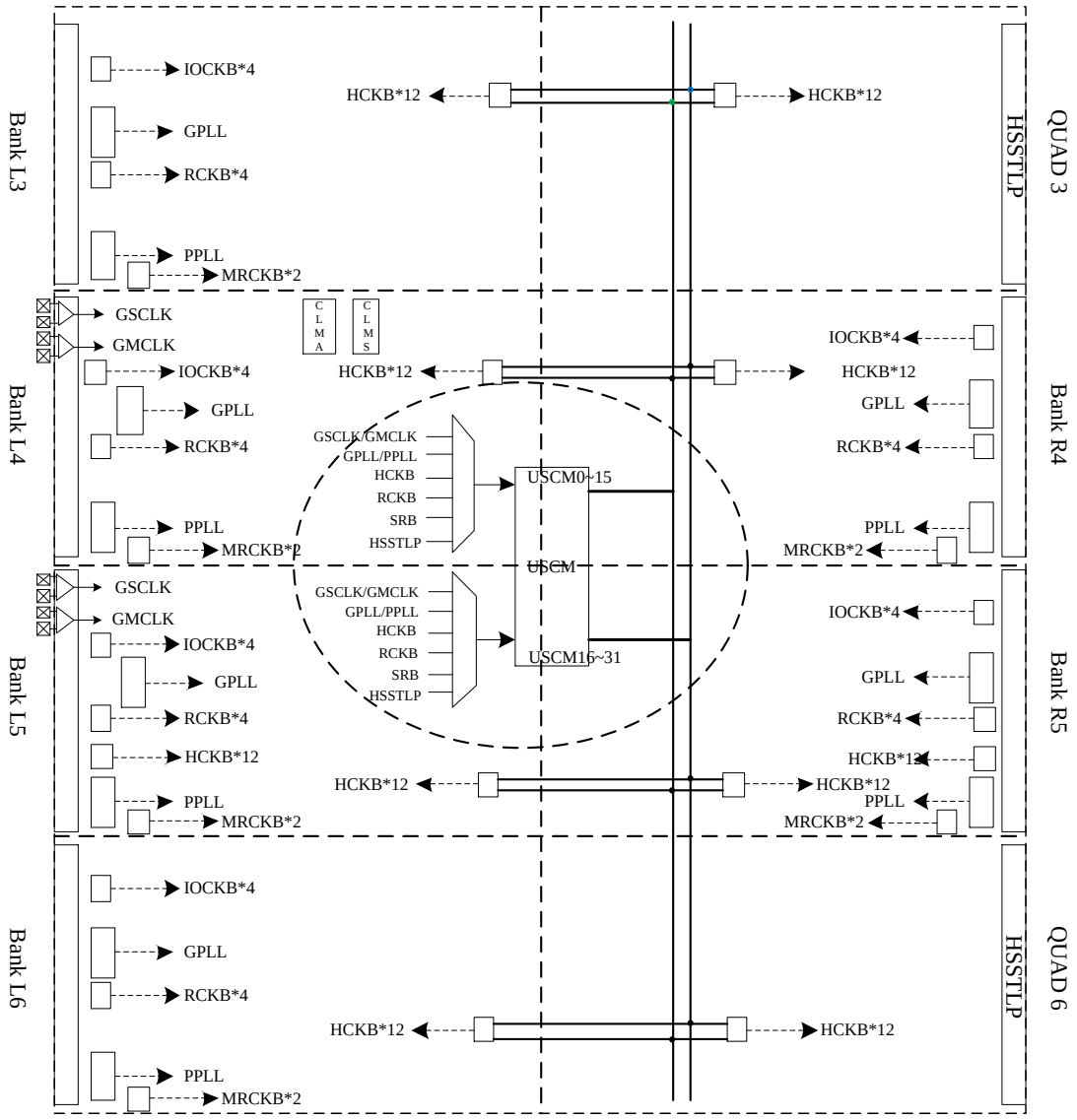

Figure 2-3 Global Clock Connection Diagram

As shown in the above diagram, the chip is divided into the upper and lower half regions by the horizontal dashed line, and the left and right half regions by the vertical dashed line in the circle. The clock input source located in the upper half region can only reach 16 USCMs in the upper half region, while the clock input source located in the lower half region can only reach 16 USCMs in the lower half region. HSSTLPs consume a substantial number of clock resources and can only

utilize global and horizontal clock resources. It is recommended to give preference to the utilization of horizontal clock resources.

The GMCLK/GSCLK, GPLL/PPLL, HCKB and RCKB global clock sources are distributed across 6 clock regions, and the HSSTLP global clock sources are distributed across 2 clock regions. Each clock region can provide up to 14 global clock sources simultaneously. Users need to consider this when using the global clocks and rationally arrange the locations of the clock sources. Additionally, each clock region can have up to 12 global clock drive logics.

2.2.2 Global Clock GTPs

USCM provides clock gating and clock selection features for the global CLK, supporting three modes: CLKBUFG, CLKBUFGCE, and CLKBUFGMUX.

CLKBUFG provides a simple clock buffer function, typically inserted automatically by software. CLKBUFGCE is a clock buffer with clock gating feature, implemented by instantiating GTP directly in RTL. CLKBUFGMUX enables dynamic switching between two clock sources, which also entails instantiating GTP in the code.

2.2.2.1 GTP_CLKBUFGCE

Instantiation of GTP_CLKBUFGCE Primitive:

```
GTP_CLKBUFGCE #(
.DEFAULT_VALUE      (1'b0           ),
.SIM_DEVICE         ("LOGOS2"       )
) GTP_CLKBUFGCE_INST (
.CLKOUT             (CLKOUT         ),
.CE                 (CE             ),
.CLKIN              (CLKIN          )
);
```

Table 2-2 GTP_CLKBUFGCE Port Description

Port Signal	**Input/Output**	**Description**
CLKIN	Input	Input Clock
CE	Input	Clock enable signal (active-high)
CLKOUT	Output	Output clock

Table 2-3 GTP_CLKBUFGCE Parameter List Description

Parameter Name	Parameter Type	Setting Value	Function Description
DEFAULT_VALUE	<string>	1'b0, 1'b1	When CE = 0, clkout outputs DEFAULT_VALUE; When CE = 1, clkout outputs CLKIN;
SIM_DEVICE	<string>	"TITAN" "LOGOS" "COMPACT" "LOGOS2"	Simulation Model Device Identification "TITAN": When triggered on a rising or falling edge, it switches after 2 beats of the clock "LOGOS" "COMPACT" "LOGOS2" "TITAN2": When triggered on a rising or falling edge, it switches after 4 beats of the clock

GTP Timing

When the parameter DEFAULT_VALUE equals to 1, CLKIN is used for sampling on the rising edge. The timing is shown below. When CE remains high, the input clock signal is transmitted to the output clock port. When CE changes from high to low and then remains unchanged, the output clock remains high after CLKIN samples two low-level CE signals. And when CE transitions from low to high and then remains unchanged, an output clock inversion appears after two high CE samplings by the CLKIN.

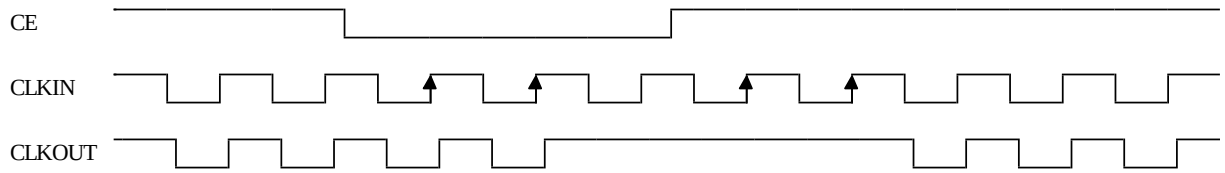

Figure 2-4 GTP_CLKBUFGCE Port Timing Diagram 1

When the parameter DEFAULT_VALUE equals to 0, CLKIN is used for sampling on the falling edge. The timing is shown below. When CE remains high, the input clock signal transmitted to the output clock port. When CE changes from high to low and remains low, the output clock remains low after CLKIN samples two low-level CE signals. And when CE transitions from low to high and holds high, an output clock inversion appears after two high CE samplings by the CLKIN.

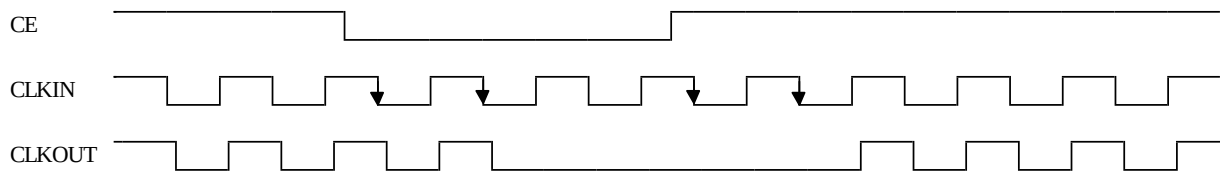

Figure 2-5 GTP_CLKBUFGCE Port Timing Diagram 2

2.2.2.2 GTP_CLKBUFGMUX

GTP_CLKBUFGMUX with clock selection can also be instantiated for dynamic switching between two global clock input sources, allowing users to choose forced switching (corresponding to TRIGGER_MODE = "NORMAL"), together with glitchless switching triggered by the clock's falling edge (corresponding to TRIGGER_MODE = "NEGEDGE") and rising edge (corresponding to TRIGGER_MODE = "POSEDGE").

Glitches are introduced when users switch the input clocks in the case of TRIGGER_MODE = "NORMAL". The relevant logic should be reset after switching to achieve the expected functionality.

Instantiation of CLKBUFGMUX Primitive:

```
GTP_CLKBUFGMUX #(
.TRIGGER_MODE   ("NEGEDGE"    ),
.SIM_DEVICE     ("LOGOS2"     )
) GTP_CLKBUFGMUX_INST (
.CLKOUT         (CLKOUT       ),
.CLKIN0         (CLKIN0       ),
.CLKIN1         (CLKIN1       ),
.SEL            (SEL          )
);
```

Table 2-4 GTP_CLKBUFGMUX Port Description

Port Signal	**Input/Output**	**Description**
CLKIN0	Input	Input clock 0
CLKIN1	Input	Input clock 1
SEL	Input	Clock selection signal, 0 selects CLK0; 1 selects CLK1;
CLKOUT	Output	Output clock

Table 2-5 GTP_CLKBUFGMUX Parameter Description

Parameter Name	**Parameter Type**	**Valid Values**	**Function Description**
TRIGGER_MODE	<string>	"NORMAL" "NEGEDGE" "POSEDGE"	(1) "NORMAL": In this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched and the glitchless function is not available (2) "NEGEDGE": In this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched with the glitchless function triggered on the falling edge of the clock. (3) "POSEDGE": In this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched with the glitchless function triggered on the rising edge of the clock.

Parameter Name	Parameter Type	Valid Values	Function Description
SIM_DEVICE	<string>	"TITAN" "LOGOS" "COMPACT" "LOGOS2"	Simulation Model Device Identification "TITAN": When triggered on a rising or falling edge, it switches after 2 beats of the clock "LOGOS" "COMPACT" "LOGOS2" "TITAN2": When triggered on a rising or falling edge, it switches after 4 beats of the clock

GTP Timing

The Timing Diagram of GTP_CLKBUFGMUX is shown below. When switching clocks in the modes of TRIGGER_MODE = "NEGEDGE" and TRIGGER_MODE = "POSEDGE", the levels remain at the respective current values until the next falling or rising edge of the clock.

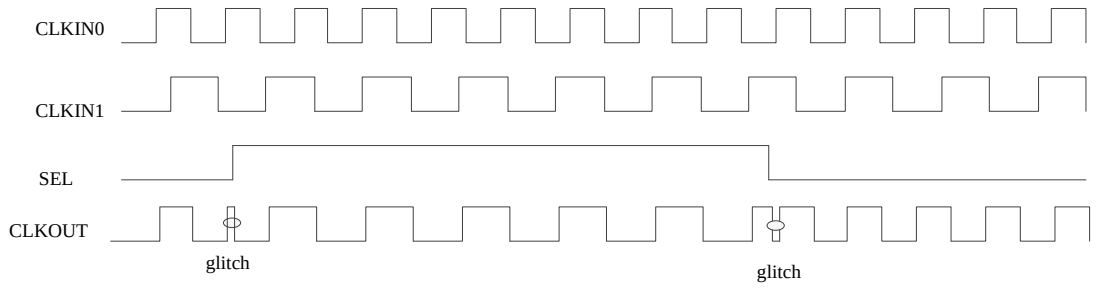

Figure 2-6 CLKBUFGMUX Timing Diagram 1 (TRIGGER_MODE = "NORMAL")

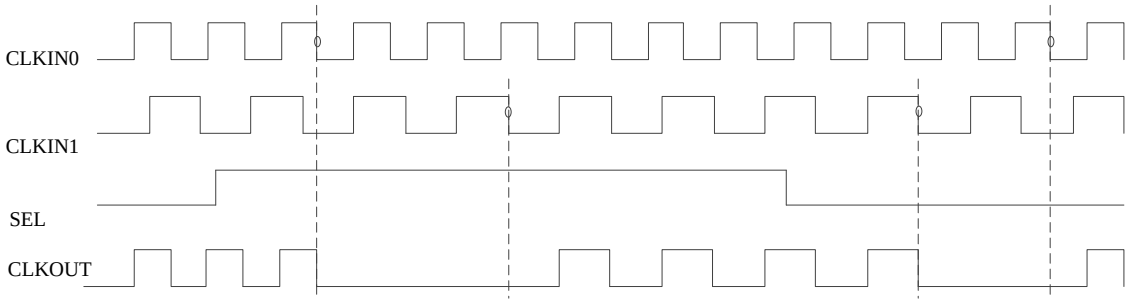

Figure 2-7 CLKBUFGMUX Timing Diagram 2 (TRIGGER_MODE = "NEGEDGE")

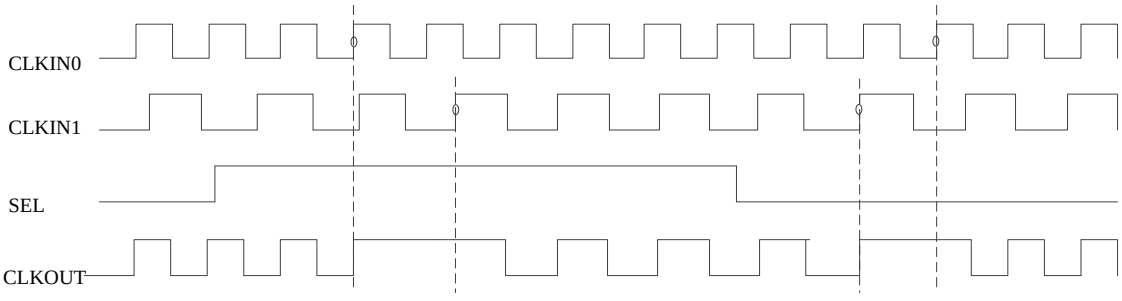

Figure 2-8 CLKBUFGMUX Timing Diagram 3 (TRIGGER_MODE = "POSEDGE")

2.2.2.3 GTP_CLKBUFGMUX_E1

GTP_CLKBUFGMUX_E1 has partial features of GTP_CLKBUFGCE and GTP_CLKBUFGMUX. The EN signal controls the clock signal output behaviour of CLKOUT, while the SEL signal allows for dynamic switching between input clocks. It must ensure that the current switching action is completed before performing the next switch. Differing from GTP_CLKBUFGMUX parameter setting, it only supports two switching modes, namely "NEGEDGE" mode and "POSEDGE" mode. The "INIT_SEL" parameter can be used to set the initial output clock.

Instantiation of GTP_CLKBUFGMUX_E1 Primitive:

```
GTP_CLKBUFGMUX_E1 #(
.TRIGGER_MODE   ("NEGEDGE"    ),
.INIT_SEL       ("CLK0"       )
) GTP_CLKBUFGMUX_E1_INST(
.CLKOUT         (CLKOUT       ),
.CLKIN0         (CLKIN0       ),
.CLKIN1         (CLKIN1       ),
.EN             (EN           ),
.SEL            (SEL          ) );
```

Table 2-6 GTP_CLKBUFGMUX_E1 Port Description

Port Signal	**Input/Output**	**Description**
CLKIN0	Input	Input clock 0
CLKIN1	Input	Input clock 1
EN	Input	Clock enable control signal: EN = 1: CLKOUT outputs clock signal EN = 0: CLKOUT does not output clock signal
SEL	Input	Clock selection control signal: SEL = 1: Select CLKIN1 output SEL = 0: Select CLKIN0 output
CLKOUT	Output	Output clock

Table 2-7 GTP_CLKBUFGMUX_E1 Parameter Description

Parameter Name	**Parameter Type**	**Valid Values**	**Function Description**
TRIGGER_MODE	<string>	"POSEDGE" "NEGEDGE"	Choose to trigger on the rising edge or falling edge of the clock: When set to "NEGEDGE", falling edge trigger is used; When set to "POSEDGE", rising edge trigger is used.
INIT_SEL	<string>	"CLK0" "CLK1"	Select the initial output clock: When set to "CLK0", CLKOUT = CLKIN0;

Parameter Name	Parameter Type	Valid Values	Function Description
			When set to "CLK1", CLKOUT = CLKIN1.

GTP Timing

When TRIGGER_MODE = "NEGEDGE" and INIT_SEL = "CLK0", it triggers on the falling edge. The timing diagram of the port is shown below when CLKIN0 is chosen as the initial clock:

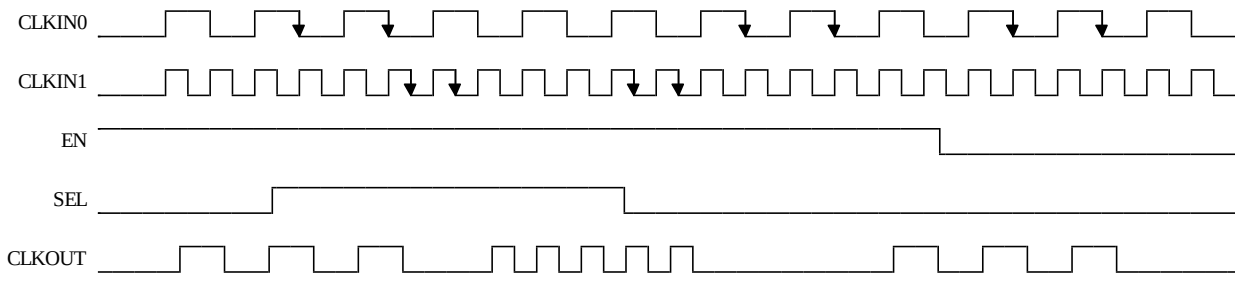

Figure 2-9 GTP_CLKBUFGMUX_E1 Port Timing Diagram 1

1. When EN = 1
    1) When SEL switches from 0 to 1, it requires detecting the falling edge of the current clock CLKIN0 twice and then the falling edge of the switch-to clock CLKIN1 twice (with the CLKOUT output low during the detection of the falling edge of the switch-to clock). After the detection is completed, CLKOUT switches from CLKIN0 to CLKIN1
    2) When SEL switches from 1 to 0, it requires detecting the falling edge of the CLKIN1 twice and then the falling edge of the CLKIN0 twice (with the CLKOUT output low during the detection of the falling edge of the switch-to clock CLKIN0). After the detection is completed, CLKOUT switches from CLKIN1 to CLKIN0
2. When EN = 0, no SEL signal transitions are allowed. For the circumstance of EN transition from 1 to 0 in the above diagram, the output goes to a low level after detecting the falling edge of CLKIN0 twice.

When TRIGGER_MODE = "POSEDGE" and INIT_SEL = "CLK0", it triggers on the rising edge. The timing of the port is shown below when CLKIN0 is chosen as the initial clock:

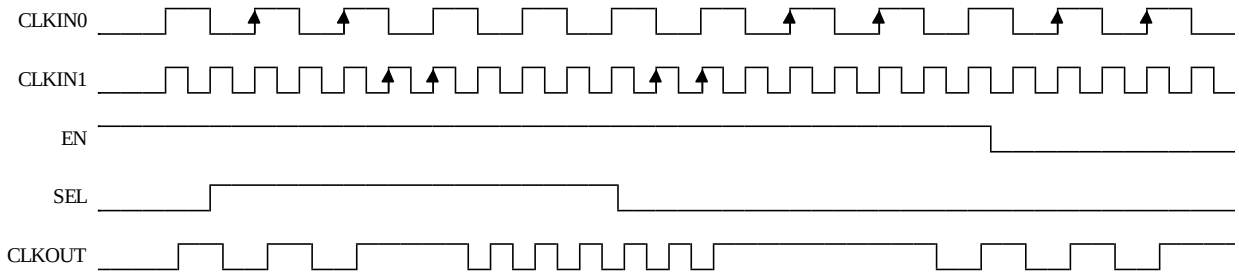

Figure 2-10 GTP_CLKBUFGMUX_E1 Port Timing Diagram 2

1. When EN = 1
    1) When SEL switches from 0 to 1, it requires detecting the rising edge of the current clock CLKIN0 twice and then the rising edge of the switch-to clock CLKIN1 twice (with the CLKOUT output high during the detection of the rising edge of the switch-to clock). After the detection is completed, CLKOUT switches from CLKIN0 to CLKIN1
    2) When SEL switches from 1 to 0, it requires detecting the rising edge of the CLKIN1 twice and then the rising edge of the CLKIN0 twice (with the CLKOUT output high during the detection of the rising edge of the switch-to clock CLKIN0). After the detection is completed, CLKOUT switches from CLKIN1 to CLKIN0
2. When EN = 0, no SEL signal transitions are allowed. For the circumstance of EN transition from 1 to 0, the output goes to a high level after detecting two rising edges of CLKOUT.

In the case of EN = 1 and only one active clock source, it is necessary to ensure that the INIT_SEL parameter setting corresponds to the active clock source, and that the SEL option is set to active clock output:

- CLKIN0 active, CLKIN1=1/0, INIT_SEL="CLK0", SEL=0, CLKOUT=CLKIN0
- CLKIN0 active, CLKIN1=1/0, INIT_SEL="CLK0", SEL=1, CLKOUT=0/1
- CLKIN0=1/0, CLKIN1 active, INIT_SEL="CLK1", SEL=0, CLKOUT=0/1
- CLKIN0=1/0, CLKIN1 active, INIT_SEL="CLK1", SEL=1, CLKOUT= CLKIN1

In the case where TRIGGER_MODE is set to "POSEDGE", CLKOUT holds a value of 1 when its output remains unchanged. And with TRIGGER_MODE set as "NEGEDGE", CLKOUT holds a value of 1 when its output remains unchanged.

Attention:

If the initial output clock and the SEL signal specified by INIT_SEL do not match the active clock source, the active clock output by CLKOUT cannot be guaranteed. For example, assuming the input clock CLKIN0 toggles normally, while the input clock CLKIN1 is set to 1/0, INIT_SEL is configured as "CLK0" to designate CLKIN0

as the initial output clock, and SEL is set to 1 for selecting CLKIN1 output, the output clock remains low after downloading the bitstream. And the output clock persists in a low state even if choosing the CLKIN0 output with SEL set to 0. Similarly, in the event that two clock sources are initially active but one of them is lost during the operation, the same issue may arise. Normal operation resumes when both clock sources become active.

2.2.2.4 GTP_CLKBUFGMUX_E2

GTP_CLKBUFGMUX_E2 also allows for dynamic switching between different input clocks, inheriting some features of GTP_CLKBUFGMUX and GTP_CLKBUFGMUX_E1. The biggest difference from the two GTPs is that this GTP provides users with the option to decide which edge of the input clock to be switched for detection. When choosing to detect one or two clock edges or not detecting either one, it is required to ensure the current switching is completed before initiating the next switching action. When only one input clock edge is detected, the SEL signal can be considered an enable signal. For example, when DETECT_CLK0 = 1 and DETECT_CLK1 = 0, the output clock follows CLKIN0 with the SEL set to 0, while remaining at 1/0 with the SEL set to 1. When DETECT_CLK0 = 0 and DETECT_CLK1 = 1, the output clock remains at 1/0 with the SEL set to 0, while following CLKIN1 with the SEL set to 1. Choose among these 3 GTPs based on the actual application requirements.

The following points need to be noted:

- If neither of the two input clock edges is detected, glitches may occur during clock switching
- If the detection definition involves both input clock edges initially but is later altered to one edge, glitches may also occur during the configuration of DETECT_CLK0 and its transition from 1 to 0 (see Figure 2-12).
- Switching to dual-edge detection requires a wait of 4 beats, while switching to single-edge detection requires a wait of 2 beats. Immediate switching takes place when no clock edge detection is performed. Refer to the interface timing description for details.

Instantiation of GTP_CLKBUFGMUX_E2 Primitive:

```
GTP_CLKBUFGMUX_E2 #(
.TRIGGER_MODE   ("NEGEDGE"      ),
.INIT_SEL       ("CLK0"         )
) GTP_CLKBUFGMUX_E2_INST (
.CLKOUT         (CLKOUT         ),
.CLKIN0         (CLKIN0         ),
.CLKIN1         (CLKIN1         ),
```

```
.DETECT_CLK0    (DETECT_CLK0    ),
.DETECT_CLK1    (DETECT_CLK1    ),
.SEL            (SEL            ) );
```

Table 2-8 GTP_CLKBUFGMUX_E2 Port Description

Port Signal	Input/Output	Description
CLKIN0	Input	Input clock 0
CLKIN1	Input	Input clock 1
DETECT_CLK0	Input	When set to 1: CLKIN0 clock edge detection is performed during clock switching When set to 0: CLKIN0 clock edge detection is not performed during clock switching
DETECT_CLK1	Input	When set to 1: CLKIN1 clock edge detection is performed during clock switching When set to 0: CLKIN1 clock edge detection is not performed during clock switching
SEL	Input	Clock selection control signal SEL = 1: Select CLKIN1 SEL = 0: Select CLKIN0
CLKOUT	Output	Output clock

Table 2-9 GTP_CLKBUFGMUX_E2 Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
TRIGGER_MODE	<string>	"POSEDGE" "NEGEDGE"	Choose to trigger on the rising edge or falling edge of the clock: When set to "NEGEDGE", falling edge trigger is used When set to "POSEDGE", rising edge trigger is used
INIT_SEL	<string>	"CLK0" "CLK1"	Select the initial output clock: When set to "CLK0", CLKOUT = CLKIN0 When set to "CLK1", CLKOUT = CLKIN1

The CLKOUT outputs for different DETECT_CLK0, DETECT_CLK1, SEL, and TRIGGER_MODE configurations are shown in the table below. In the case of CLKIN0 active and CLKIN1 = 1/0, the INIT_SEL parameter is set to "CLK0"; in the case of CLKIN0 = 1/0 and CLKIN1 active, the parameter is set to "CLK1". Under the condition of only one active clock source, it is necessary to ensure that the INIT_SEL parameter setting corresponds to the active clock source.

Table 2-10 CLKOUT Output Results for Various GTP_CLKBUFGMUX_E2 Configurations

CLKIN0	CLKIN1	DETECT_CLK0	DETECT_CLK1	SEL	CLKOUT
Active	Active	0	0	0	CLKOUT=CLKIN0
		0	0	1	CLKOUT=CLKIN1
		1	0	0	CLKOUT=CLKIN0
		1	0	1	"NEGEDGE": 0 "POSEDGE": 1

CLKIN0	CLKIN1	DETECT_CLK0	DETECT_CLK1	SEL	CLKOUT
		0	1	0	"NEGEDGE": 0 "POSEDGE": 1
		0	1	1	CLKOUT=CLKIN1
		1	1	0	CLKOUT=CLKIN0
		1	1	1	CLKOUT=CLKIN1
Active	1/0	0	0	0	CLKOUT=CLKIN0
		0	0	1	0
		1	0	0	CLKOUT=CLKIN0
		1	0	1	"NEGEDGE": 0 "POSEDGE": 1
		0	1	0	"NEGEDGE": 0 "POSEDGE": 1
		0	1	1	"NEGEDGE": 0 "POSEDGE": 1
		1	1	0	CLKOUT=CLKIN0
		1	1	1	"NEGEDGE": 0 "POSEDGE": 1
1/0	Active	0	0	0	0
		0	0	1	CLKOUT=CLKIN1
		1	0	0	"NEGEDGE": 0 "POSEDGE": 1
		1	0	1	"NEGEDGE": 0 "POSEDGE": 1
		0	1	0	"NEGEDGE": 0 "POSEDGE": 1
		0	1	1	CLKOUT=CLKIN1
		1	1	0	"NEGEDGE": 0 "POSEDGE": 1
		1	1	1	CLKOUT=CLKIN1

GTP Timing

In the figure below, CLKOUT_NEG and CLKOUT_POS respectively pertains to the output of CLKOUT when the TRIGGER_MODE parameter is set to "NEGEDGE" and "POSEDGE". The setup is intended for easy reference and does not indicate the presence of 2 clock outputs in this GTP. 1 GTP has only 1 CLKOUT output.

Detection of two clock edges when set DETECT_CLK0=1 and DETECT_CLK1 = 1. The initial clock for CLKOUT_NEG is CLKIN0, and the port timing is shown below:

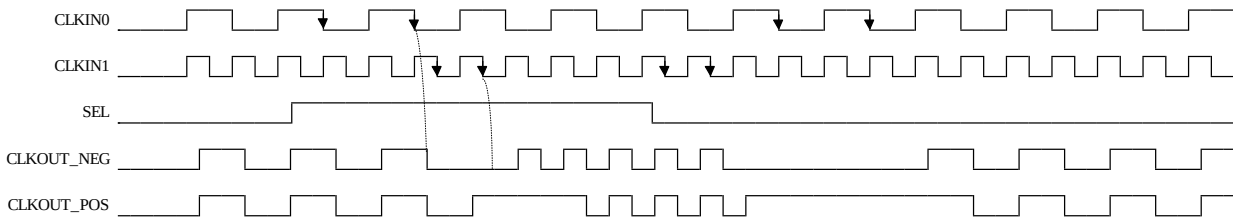

Figure 2-11 GTP_CLKBUFGMUX_E2 Port Timing Diagram 1

Take CLKOUT_NEG as an example:

1. When SEL switches from 0 to 1, it requires detecting the falling edge of the current clock CLKIN0 twice and then the falling edge of the switch-to clock CLKIN1 twice (with the CLKOUT_NEG output low during detecting the falling edge of CLKIN1 twice). Until the detection is completed, CLKOUT_NEG switches from CLKIN0 to CLKIN1.
2. When SEL switches from 1 to 0, it requires detecting the falling edge of the current clock CLKIN1 twice and then the falling edge of the switch-to clock CLKIN0 twice (with the CLKOUT output low during detecting the falling edge of CLKIN0 twice). Until the detection is completed, CLKOUT_NEG switches from CLKIN1 to CLKIN0.

The switching of CLKOUT_POS is similar to that of CLKOUT_NEG, except that the detection of the falling edge is changed by the detection of the rising edge. When detecting the rising edge of the switch-to clock, a high-level signal is output two beats following the CLKOUT_POS switching.

When DETECT_CLK0 equals to 1 and DETECT_CLK1 transitions from 1 to 0, the clock edge detection changes from including both CLKIN0 and CLKIN1 to solely considering CLKIN0 while disregarding CLKIN1. The port timing is shown below:

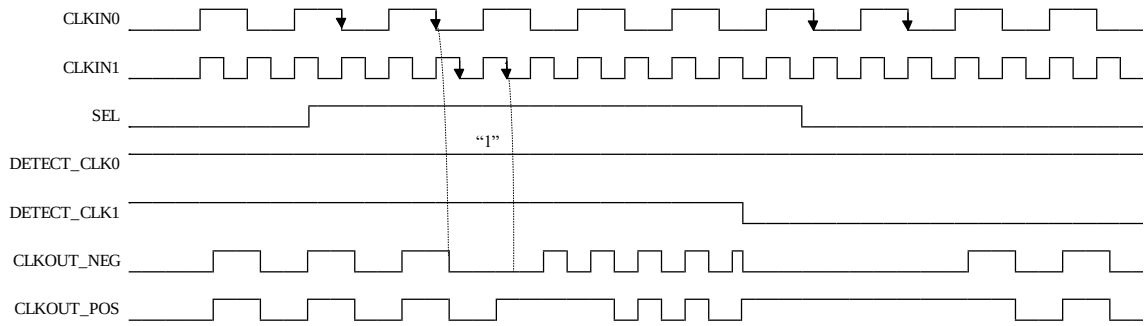

Figure 2-12 GTP_CLKBUFGMUX_E2 Port Timing Diagram 2

Take CLKOUT_NEG as an example, and the initial clock is set to CLKIN0:

1. When DETECT_CLK1 is set to 0, CLKOUT_NEG no longer outputs CLKIN1 but generates a low level signal. When SEL switches from 1 to 0, CLKIN1 clock edge detection is no longer performed, and instead of directly detecting the falling edge of CLKIN0 twice (with the CLKOUT_NEG output low during the detection of the falling edge of CLKIN0). After the detection is completed, CLKOUT_NEG switches to CLKIN0.
2. The switching of CLKOUT_POS is similar to that of CLKOUT_NEG, except that the detection of the falling edge is changed by the detection of the rising edge. CLKOUT_POS outputs a high-level signal when detecting the rising edge of the switch-to clock.

When DETECT_CLK0= 0 and DETECT_CLK1 = 1, the changes in CLKIN0 clock edges are discarded while those in CLKIN1 are detected. The port timing is shown below:

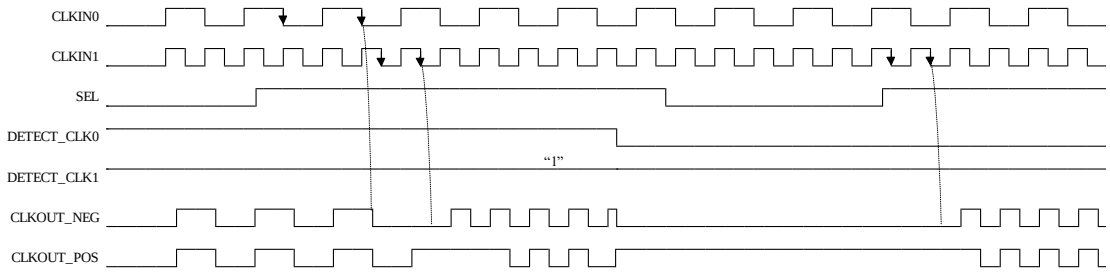

Figure 2-13 GTP_CLKBUFGMUX_E2 Port Timing Diagram 3

Take CLKOUT_NEG as an example, and the initial clock is set to CLKIN1:

When DETECT_CLK0 is set to 0, CLKOUT_NEG no longer outputs CLKIN0 but generates a low level signal. When SEL switches from 0 to 1, CLKIN0 clock edge detection is no longer performed, and instead of directly detecting the falling edge of CLKIN1 twcie (with the CLKOUT_NEG output low during the detection of the falling edge of CLKIN1). After the detection is completed, CLKOUT switches to CLKIN1.

The switching of CLKOUT_POS is similar to that of CLKOUT_NEG, except that the detection of the falling edge is changed by the detection of the rising edge. CLKOUT_POS outputs a high-level signal when detecting the rising edge of the switch-to clock.

In the case of DETECT_CLK0 = 0 and DETECT_CLK1 = 0, the detection of both CLKIN0 and CLKIN1 clock edges is ignored, and the changes in the edges of the current and switch-to clocks are not detected during the clock switching. Instead, when SEL changes, CLKOUT_NEG and CLKOUT_POS switch the clock immediately. The output clock may generate glitches in this mode, and the interface timing is shown below:

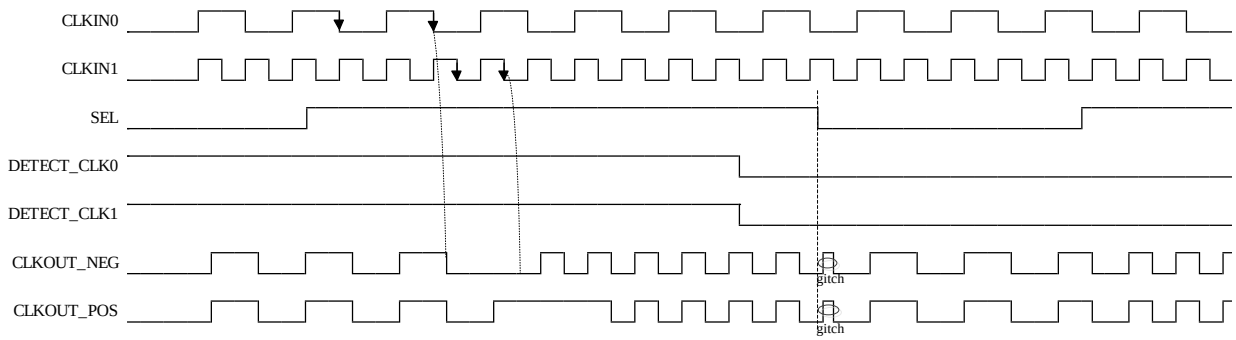

Figure 2-14 GTP_CLKBUFGMUX_E2 Port Timing Diagram 4

2.3 Horizontal Clock Resources

2.3.1 Horizontal Clock Networks

HCKB is a horizontal global clock buffer in the clock region to drive the horizontal clock network. Each region contains 12 HCKBs.

The clock inputs for HCKB are sourced from the clocks in two horizontal regions, including GSCLK, GMCLK, PPLL output clocks, GPLL output clocks, SRB, HSSTLP output clocks, USCM output clocks (global clocks) among others. HCKB provides synchronous or asynchronous dynamic enable functionality.

The connection relationship of HCKB clock input sources in symmetric adjacent horizontal regions conforms to Figure 2-15, and that of HCKB clock input sources in adjacent horizontal regions with or without HSSTLPs is reflected in Figure 2-16. In the diagrams, only USCMs in the same upper or lower half regions are accessible to the HCKB, and the USCM clock sources cannot be the HCKB outputs from the region where HSSTLP is located. However, all USCM outputs have coverage over all HCKBs on the chip. To guarantee the clock signal quality, it is not recommended to use SRB clocks.

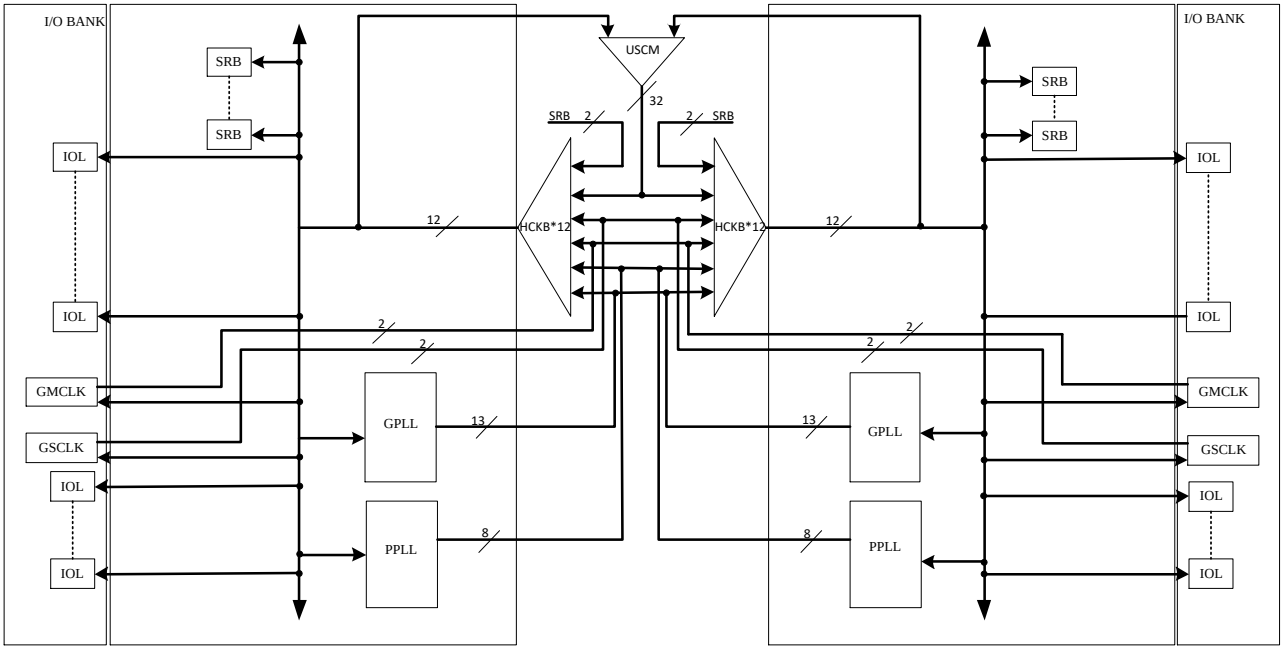

Figure 2-15 Diagram of the HCKB Input Clock Source and Output Connections for Horizontally Adjacent Clock Region without HSSTLP Clock Region

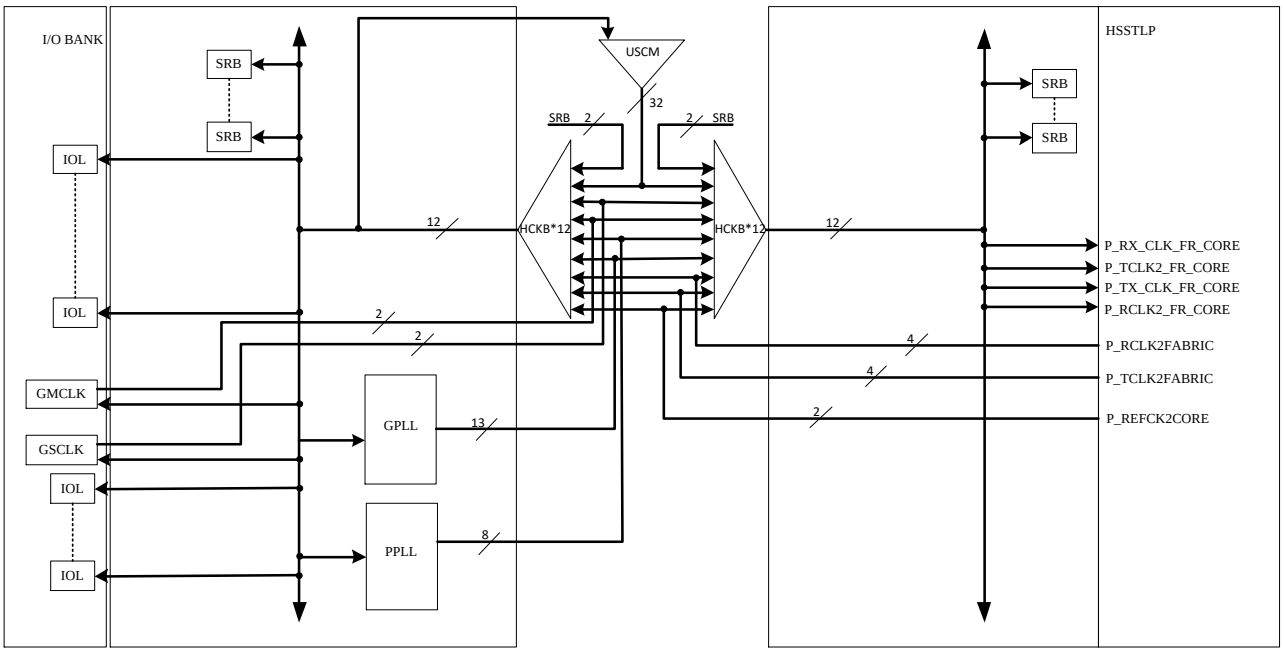

Figure 2-16 Diagram of the HCKB Input Clock Source and Output Connections for Horizontally Adjacent Clock Region with HSSTLP Clock Region

The output clocks of HCKB drive PLL, HSSTLP, SRB, and IOL, as shown in the figure above. The P_REFCK2CORE clock end of HSSTLP is a differential input reference clock that is converted to a single-ended clock for the Fabric.

2.3.2 Horizontal clock GTP

A horizontal clock GTP occupies one HCKB, and each region supports up to 12 simultaneously. The Logos2 Family products have two types of horizontal clock GTPs: one is the GTP_CLKBUFX with only input and output, and the other is the GTP_CLKBUFXCE with an enabled control signal. The CE enabled signal controls whether the clock signal is output, thereby reducing power consumption.

If the design module is only in one region or adjacent horizontal regions, the input clock can bypass the global clock tree. By manually instantiating the horizontal clock GTP, the input clock can directly use HCKB to drive the module logic. Additionally, users can constrain the instantiated primitive to the desired location according to their design requirements to achieve the design purpose.

2.3.2.1 GTP_CLKBUFX

The use of HCKB involves user instantiation of GTP_CLKBUFX, which has no parameters. Taking Verilog as an example:

```
GTP_CLKBUFX    GTP_CLKBUFX_INST
(
                .CLKIN          (CLKIN          ),
                .CLKOUT         (CLKOUT         )
);
```

GTP_CLKBUFX input and output timing description: The output clock CLKOUT is always equal to the input clock CLKIN.

2.3.2.2 GTP_CLKBUFXCE

GTP_CLKBUFXCE has an enable control signal CE, which controls whether to output the clock signal or not. By changing parameters, users can set the enable mode (synchronous enable or asynchronous enable), enable valid level (high level valid or low level valid), and trigger mode (rising edge trigger or falling edge trigger). It should be noted that in asynchronous enable mode, when the enable signal CE changes from high to low level, the output clock will immediately pull down or pull high, which may cause glitches during switching. In synchronous enable mode, each switch requires waiting for 2 clock edges, with the trigger mode determining whether it switches on the rising edge or falling edge.

GTP_CLKBUFXCE primitive instantiation:

```
GTP_CLKBUFXCE #(
```

```
.CE_TYPE        ("SYNC"     ),
.CE_INV         ("FALSE"    ),
.TRIGGER_MODE   ("POSEDGE"  )
) GTP_CLKBUFXCE_INST (
.CLKOUT         (CLKOUT     ),
.CE             (CE         ),
.CLKIN          (CLKIN      )
);
```

Table 2-11 GTP_CLKBUFXCE Port Description

CLKIN0	**Input**	**Input Clock**
CLKIN	Input	Input clock signal
CE	Input	Clock enable end
CLKOUT	Output	Output clock signal

Table 2-12 GTP_CLKBUFXCE Parameter Description

Parameter Name	**Parameter Type**	**Valid Values**	**Function Description**
CE_TYPE	<string>	"SYNC" "ASYNC"	CE_TYPE= "SYNC", supports synchronous enable. CE_TYPE= "ASYNC", supports asynchronous enable.
TRIGGER_MODE	<string>	"POSEDGE" "NEGEDGE"	TRIGGER_MODE = "POSEDGE", supports the initial value of the clock output being 1'b1, triggering on the rising edge. TRIGGER_MODE ="NEGEDGE", supports the initial value of the clock output being 1'b0, triggering on the falling edge.
CE_INV	<string>	"TRUE" "FALSE"	CE_INV= "FALSE", CE active high. CE_INV="TRUE", CE active low.

Synchronous Enable Mode:

When configured for rising edge triggered synchronous enable, the output clock is triggered by the rising edge of the input clock. When the enable is inactive, the output clock remains high; when configured for falling edge triggered synchronous enable, the output clock is triggered by the falling edge of the input clock. When the enable is inactive, the output clock remains low. Port timing is shown in the figure below:

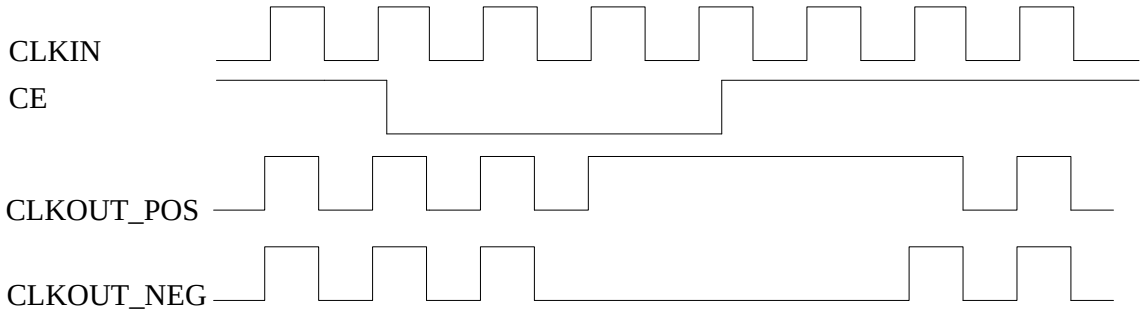

Figure 2-17 GTP_CLKBUFXCE Port Timing Diagrams 1

CLKOUT_POS represents the output clock when TRIGGER_MODE = "POSEDGE", while CLKOUT_NEG represents the output clock when TRIGGER_MODE ="NEGEDGE".

Asynchronous Enable Mode:

When configured for asynchronous enable, the output clock switches immediately when the enable signal CE switches, which may cause glitches. The port timing is as shown in the figure below:

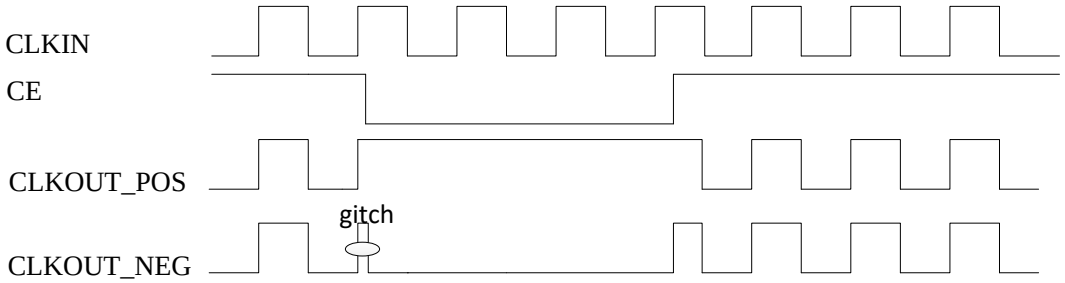

Figure 2-18 GTP_CLKBUFXCE Port Timing Diagrams 2

CLKOUT_POS represents the output clock when TRIGGER_MODE = "POSEDGE", while CLKOUT_NEG represents the output clock when TRIGGER_MODE ="NEGEDGE".

2.4 Regional Clock Resources

2.4.1 Regional Clock Network

REGIONAL CLKs are distributed based on regions, with each region having 4 REGIONAL CLK networks. A regional clock primarily provides a synchronous clock to the logic unit of a single region and is driven by RCKB.

The following figure is a schematic diagram of the RCKB scope for a single region. Since there is no RCKB and MRCKB in the region where HSSTLP is located, the RCKB input-output connection

relationships of all regions except the region where HSSTLP is located are consistent with this figure.

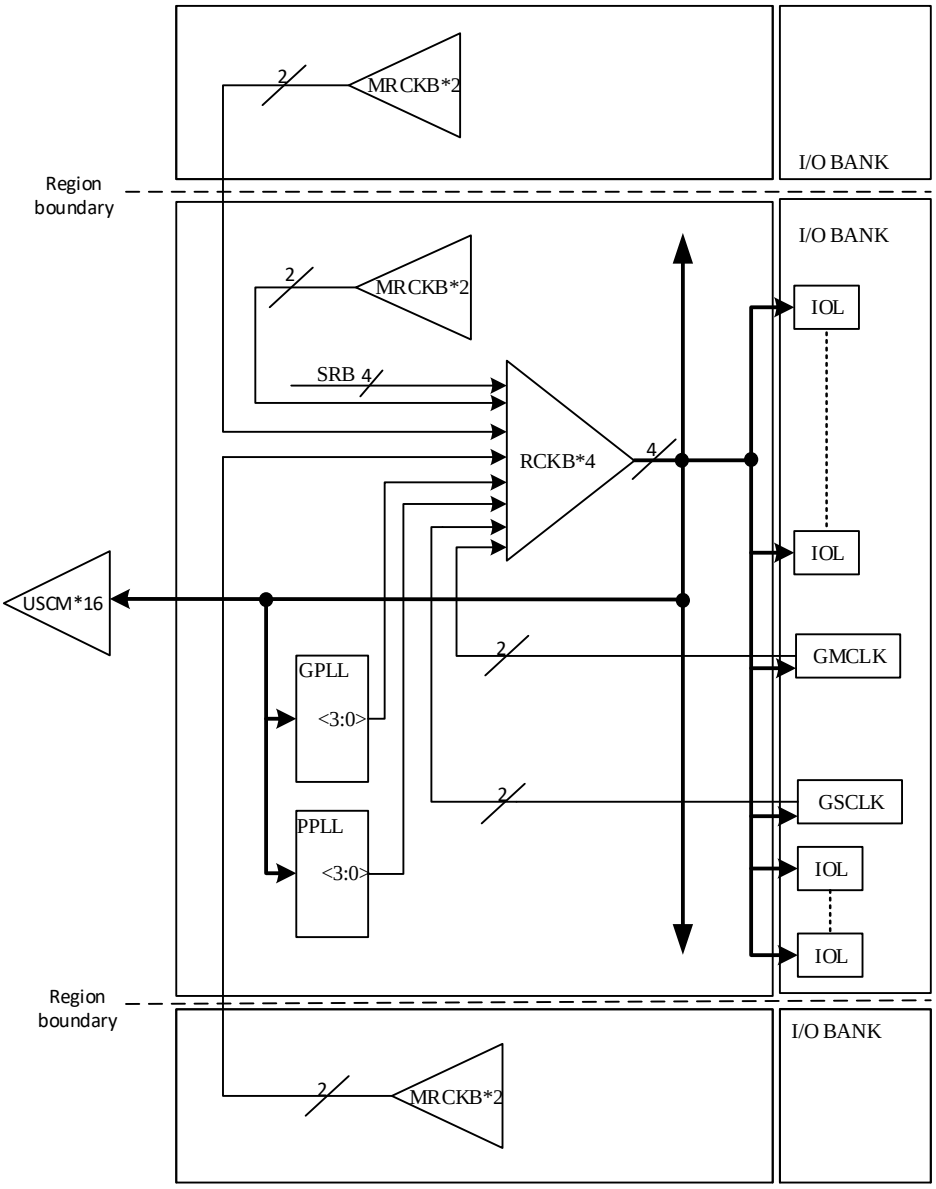

Figure 2-19 Diagram of Regional Clock Source and Scope

2.4.2 Regional Clock GTP

2.4.2.1 GTP_CLKBUFR

The use of RCKB involves user instantiation of GTP_CLKBUFR, which has no parameters. Taking Verilog as an example:

```
GTP_CLKBUFR     GTP_CLKBUFR_INST
                (
                .CLKIN          (CLKIN      ),
                .CLKOUT         (CLKOUT     )
                );
```

The port timing of GTP_CLKBUFR is shown in the figure below:

2.4.2.2 GTP_IOCLKDIV_E2

GTP_IOCLKDIV_E2 has 3 input ports: CLKIN, RST_N, CE, one output port: CLKDIVOUT, and 1 parameter: DIV_FACTOR. By configuring the parameter DIV_FACTOR, it can achieve division from 1 to 8 and bypass mode (BYPASS).

- CE is asynchronous enable control. When CE = 0, CLKDIVOUT maintains the current level; when CE = 1, CLKDIVOUT outputs a active division clock.
- RST_N is a reset signal that supports asynchronous reset and synchronous release, but it is not mandatory to use. When RST_N = 0, the output clock is cleared.
- In BYPASS mode, the output clock is not controlled by CE or RST_N.

Instantiation of the GTP_IOCLKDIV_E2 primitive:

```
GTP_IOCLKDIV_E2 #(
.DIV_FACTOR         ("BYPASS"       )
) IOCLKDIV_E2_INST (
.CLKDIVOUT          (CLKDIVOUT  ),
.CE                 (CE         ),
.CLKIN              (CLKIN      ),
.RST_N              (RST_N      )
);
```

Table 2-13 GTP_IOCLKDIV_E2 Port Description

CLKIN0	**Input**	**Input Clock**
CLKIN	Input	Input Clock
RST_N	Input	Reset signal, active low
CE	Input	Enable control: CE = 1, output clock signal with or without division CE = 0, output clock maintains current level
CLKDIVOUT	Output	Output clock

Table 2-14 GTP_IOCLKDIV_E2 Parameter Description

Parameter Name	**Parameter Type**	**Valid Values**	**Function Description**
DIV_FACTOR	<string>	"BYPASS" "1" "2" "3" "4" "5" "6" "7" "8"	Mode selection includes bypass mode and 1~8 division modes.

Taking division by 1 and division by 2 output clocks as examples, the port timing is shown in the figure below:

When RST_N is low, CLKOUT outputs 0. When RST_N and CE are high, CLKOUT outputs an active clock. When CE is low, CLKOUT immediately pulls down, outputting 0.

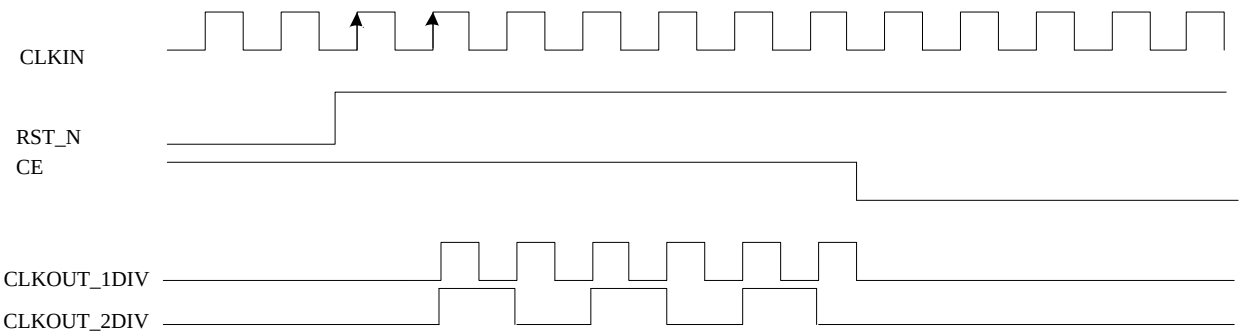

Figure 2-20 GTP_IOCLKDIV_E2 Port Timing Diagram

2.5 IO Clock Resources

2.5.1 IO Clock Network

IO CLK provides high-speed clocks for the IO of the Logos2 Family products, which are commonly used in high-speed interface logic, driven by IOCKB. Compared to GCLK/RCLK, IO CLK has features such as high frequency, short latency, and small skew etc.

PG2L100H has four IOCKB driving IO CLK clock lines in each clock region, as shown in the figure below.

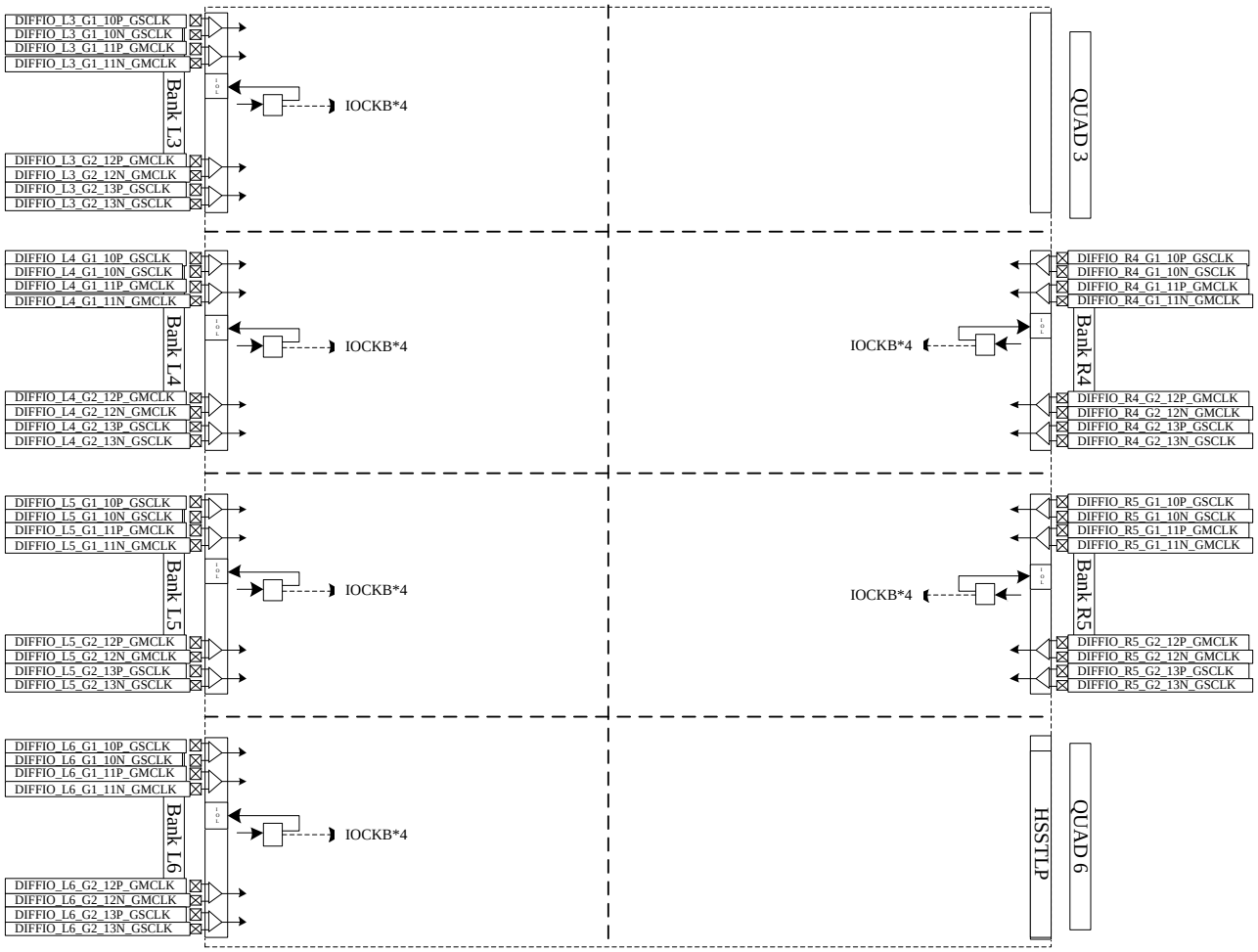

Figure 2-21 IO CLK Clock Resources Diagram

As shown in the figure below, the output clocks CLKOUT0~3 of PPLL provide high-quality high-speed clocks to the IOL within the BANK via IOCKB.

The figure below shows a single region IOCKB schematic, clearly indicating the input clock sources and output driving range of IOCKB. Since the HSSTLP region does not have IOCKB and MRCKB, the IOCKB input-output connection relations in other regions are consistent with this diagram, except for the HSSTLP region.

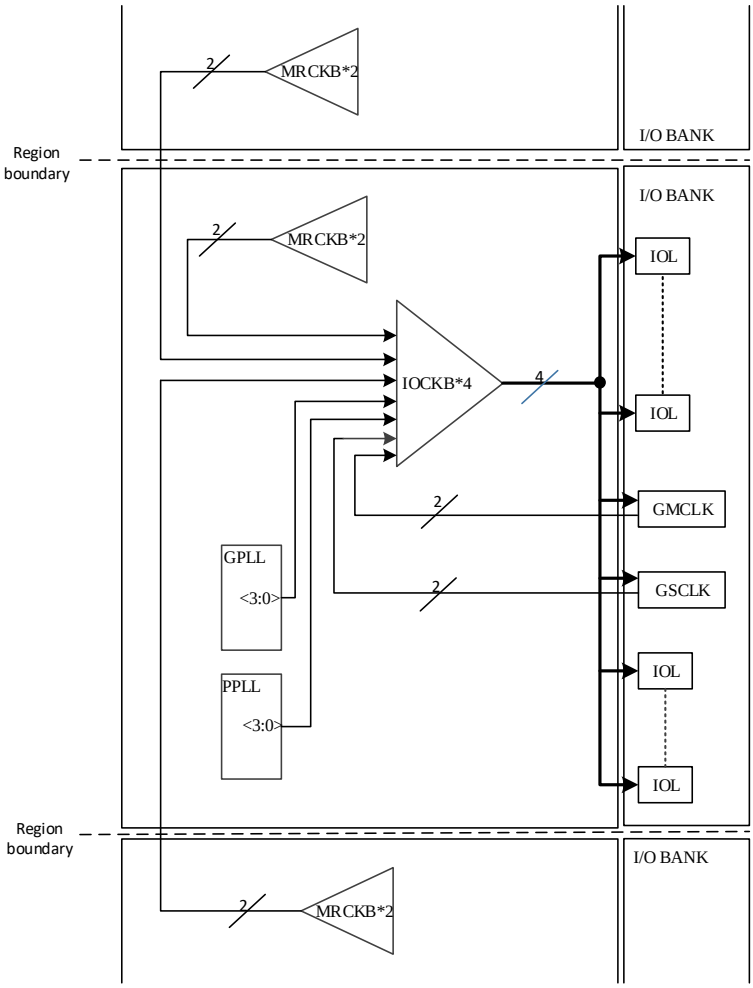

Figure 2-22 Clock Input Clock Source Connection Diagram

2.5.2 IO Clock GTP

The use of IOCKB is instantiated by the user inserting the GTP_IOCLKBUF. Taking Verilog as an example:

```
GTP_IOCLKBUF
#(
.GATE_EN ("FALSE" ) // The Logos2 Family only supports the parameter "FALSE"
) GTP_IOCLKBUF_INST
(
.CLKIN (CLKIN ),
.DI (DI ),
.CLKOUT (CLKOUT )
);
```

Table 2-15 GTP_IOCLKBUF Port Description

Port Signal	Input/Output	Description
CLKIN	Input	Input Clock
DI	Input	Clock enable, not supported by Logos2
CLKOUT	Output	Output clock

Table 2-16 GTP_IOCLKBUF Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
GATE_EN	<string>	<"FALSE","TRUE">	Logos2 can only be configured as "FALSE"

The GTP_IOCLKBUF of the Logos2 Family devices only supports the buffer function. The parameter GATE_EN can only be configured as "FALSE". DI control clock signal is not supported, meaning that whether DI inputs 1 or 0, CLKOUT will still output a valid clock signal.

2.6 Cross-Regional Clock Resources

2.6.1 Cross-Regional Clock Network

MRCKB mainly provides multi-region clock connections. As shown in the figure below, the input sources of MRCKB include GMCLK and SRB.

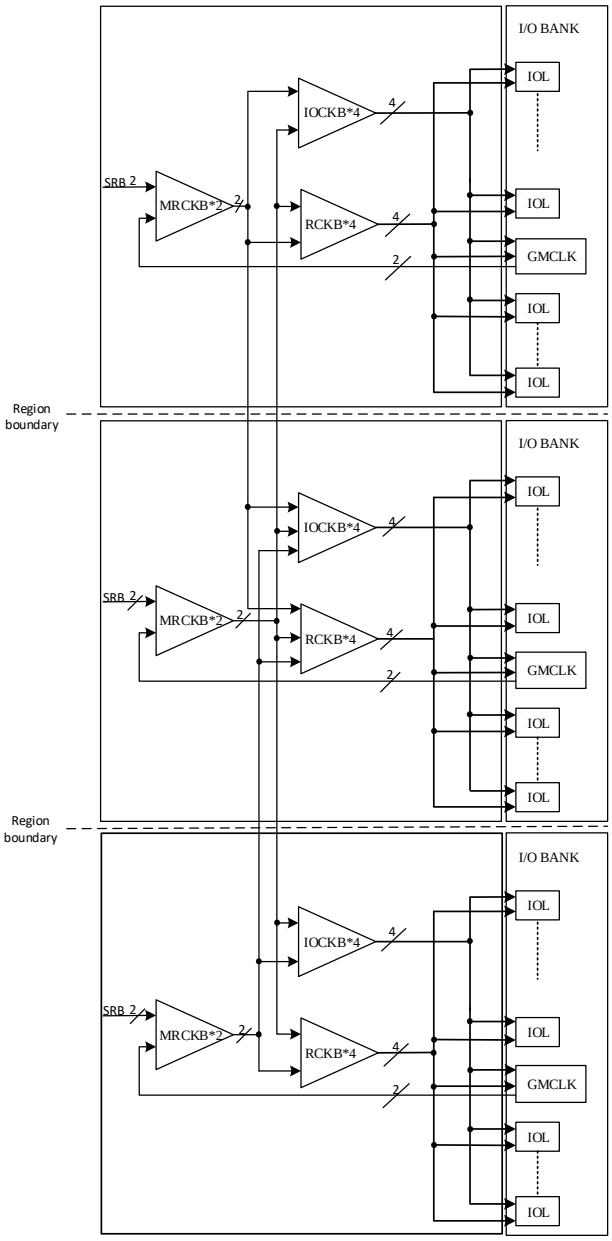

Figure 2-23 Diagram of MRCKB Input Clock Sources and Output Connection Relations

The diagram above shows the multi-region clock buffer input clock sources and output connections. It clearly indicates the input clock sources, output driving resources, and reachable regions of MRCKB. Since the HSSTLP region does not have MRCKB, IOCKB, and RCKB, the MRCKB connection relations in other regions are consistent with this diagram. When an external clock single-ended input is used, only the GMCLK_P side can ensure that the clock signal takes the dedicated clock path to reach MRCKB.

2.6.2 Cross-Region Clock GTP

2.6.2.1 GTP_CLKBUFM

Support for MRCKB is instantiated by inserting user instantiation of GTP_CLKBUFM or GTP_CLKBUFMCE. Taking Verilog as an example, when the user instantiates GTP_CLKBUFM into MRCKB, it is as follows:

```
GTP_CLKBUFM    GTP_CLKBUFM_INST
                    (
                    .CLKIN          (CLKIN        ),
                    .CLKOUT         (CLKOUT       ));
```

GTP_CLKBUFM input and output timing description: The output clock CLKOUT is always equal to the input clock CLKIN.

2.6.2.2 GTP_CLKBUFMCE

When the user instantiates the GTP_CLKBUFMCE with the enable end into MRCKB, as in Verilog, for example.

```
GTP_CLKBUFMCE #(
.CE_TYPE            ("SYNC"         ),
.CE_INV             ("FALSE"        ),
.TRIGGER_MODE       ("POSEDGE"      )
) CLKBUFMCE_INST (
.CLKOUT             (CLKOUT         ),
.CE                 (CE             ),
.CLKIN              (CLKIN          ) );
```

Table 2-17 GTP_CLKBUFMCE Port Description

Port	**Input/Output**	**Function Description**
CLKIN	Input	Input clock signal
CE	Input	Clock enable end
CLKOUT	Output	Output clock signal

Table 2-18 GTP_CLKBUFMCE Parameter Description

Parameter Name	Valid Values	Function Description
CE_TYPE	"SYNC" "ASYNC"	CE_TYPE = "SYNC", supports synchronous enable CE_TYPE = "ASYNC", supports asynchronous enable
TRIGGER_MODE	"POSEDGE" "NEGEDGE"	TRIGGER_MODE = "POSEDGE", supports clock output initial value equal to 1'b1, triggered by the rising edge TRIGGER_MODE = "NEGEDGE", supports clock output initial value equal to 1'b0, triggered by the falling edge
CE_INV	"TRUE" "FALSE"	CE_INV = "FALSE", default CE active high CE_INV = "TRUE", default CE active low

Table 2-19 GTP_CLKBUFMCE Mode Description

CE_TYPE	TRIGGER_MODE	CE_INV	Function
"SYNC"	"POSEDGE"	"FALSE"	Rising edge synchronous enable mode
"SYNC"	"NEGEDGE"	"FALSE"	Falling edge synchronous enable mode
"ASYNC"	"NEGEDGE"	"FALSE"	Asynchronous enable mode 0
"ASYNC"	"POSEDGE"	"FALSE"	Asynchronous enable mode 1

Description of input and output timing for different operating modes of GTP_CLKBUFMCE:

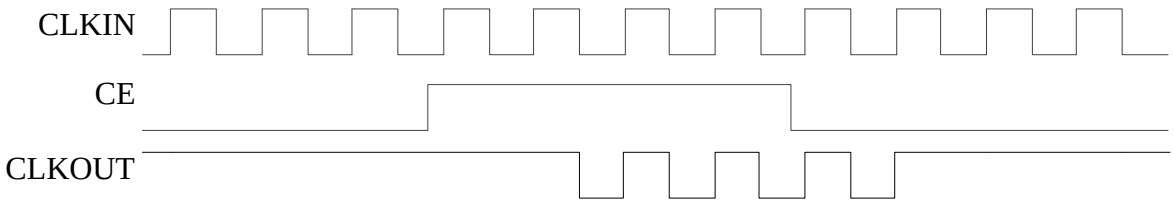

Figure 2-24 GTP_CLKBUFMCE Rising Edge Synchronous Enable Input and Output Timing Diagram

When configured for rising edge-triggered synchronous enable, the output clock is triggered by the rising edge of the input clock, and remains high when the enable is inactive.

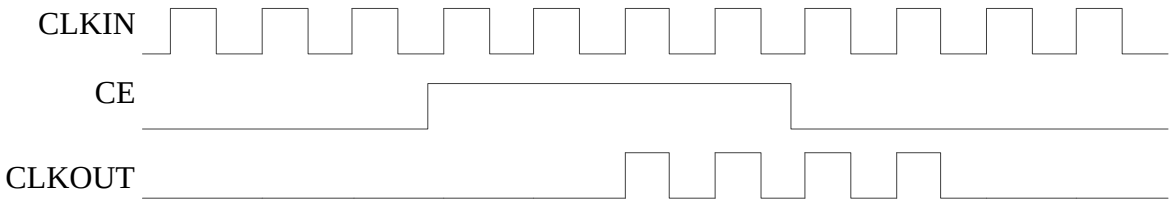

Figure 2-25 GTP_CLKBUFMCE Falling Edge Synchronous EnableInput and Output Timing Diagram

When configured for falling edge-triggered synchronous enable, the output clock is triggered by the falling edge of the input clock, and remains low when the enable is inactive.

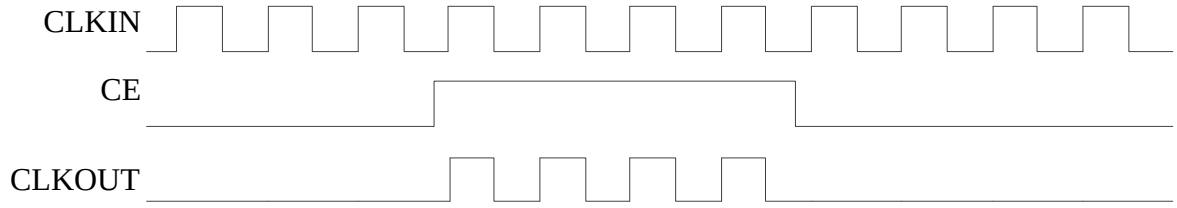

Figure 2-26 GTP_CLKBUFMCE Asynchronous Enable Mode 0 Input and Output Timing Diagram

When configured for asynchronous enable mode 0, the output clock outputs low when the enable is inactive, as shown in the above function timing diagram.

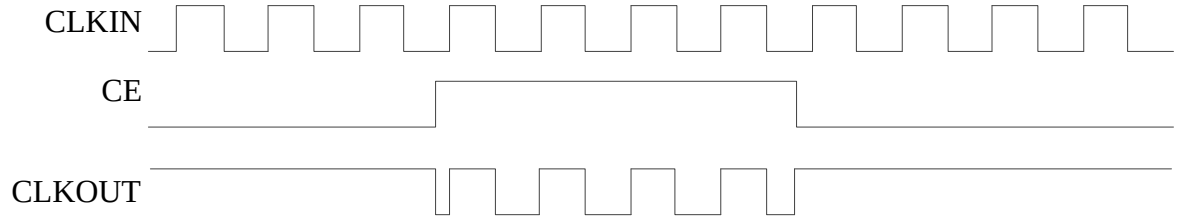

Figure 2-27 GTP_CLKBUFMCE Asynchronous Enable Mode 1 Input and Output Timing Diagram

When configured for asynchronous enable mode 1, the output clock outputs high when the enable is inactive, as shown in the above timing diagram.

2.7 PLL Clock Connection

The input sources for GPLL and PPLL include:

- GMCLK and GSCLK on the same left or right side
- USCM
- RCKB in the same region
- HCKB in the same region
- GPLL/PPLL CLKOUT0~3/N
- HSSTLP clock, please refer to 1.2 section for clock connection overview

As shown in the figure below, the clock source connections for GPLL and PPLL are the same for other banks except for the horizontally adjacent area with HSSTLP.

As the HSSTLP area does not have GPLL and PPLL, the HSSTLP output clock must go through USCM or HCKB to reach GPLL/PPLL to serve as its input clock source, and can be inserted into GTP_CLKBUFG or GTP_CLKBUFX.

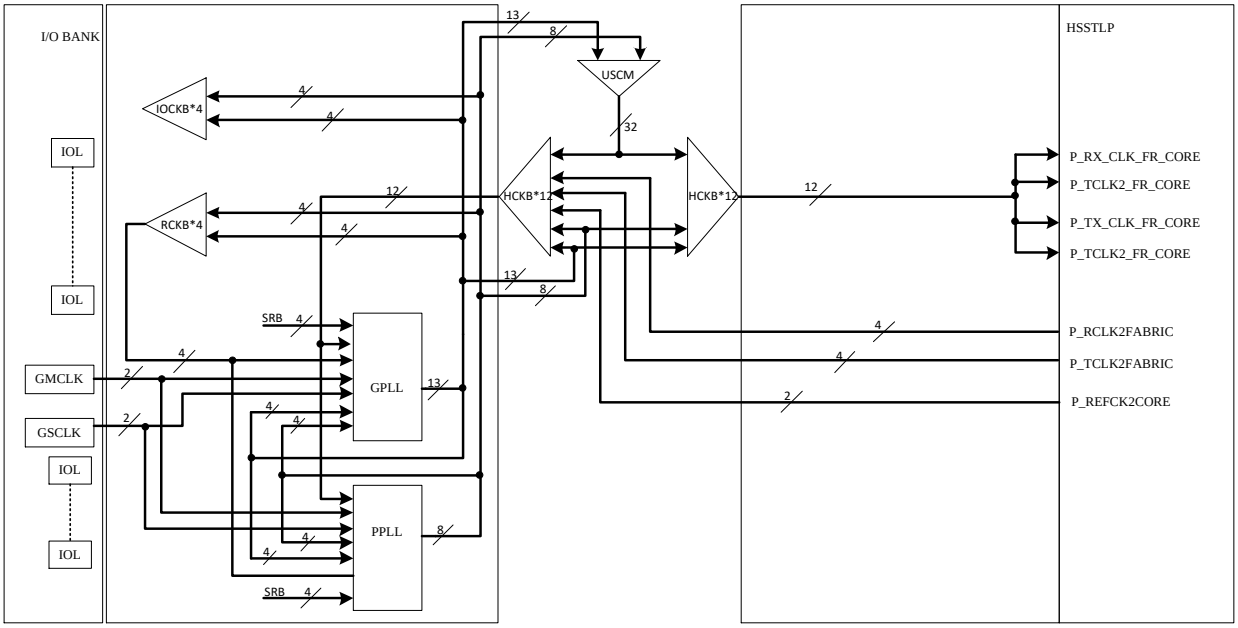

Figure 2-28 PLL Input Clock Source and Output Clock Connection Diagram

Through the master clock route or clock tree (RCKB, HCKB) of the PLL, PPLL and GPLL's CLKOUT0~3 can serve as the input clocks for PPLL and GPLL in other PLLs, thus completing the PLL cascade.

Notes:

1. The clock signals from the GMCLK and GSCLK pins can reach the left and right half areas of the GPLL/PPLL, but they must go through the USCM or the adjacent horizontal region's HCKB to proceed.
2. The output clocks CLKOUT0N~3N from the GPLL and CLKOUT0N from the PPLL can only drive the USCM and HCKB when used individually. The output clocks CLKOUT1N~3N from the PPLL cannot be used as standalone user clocks.

2.8 Usage Instructions for GPLL

2.8.1 GPLL Overview

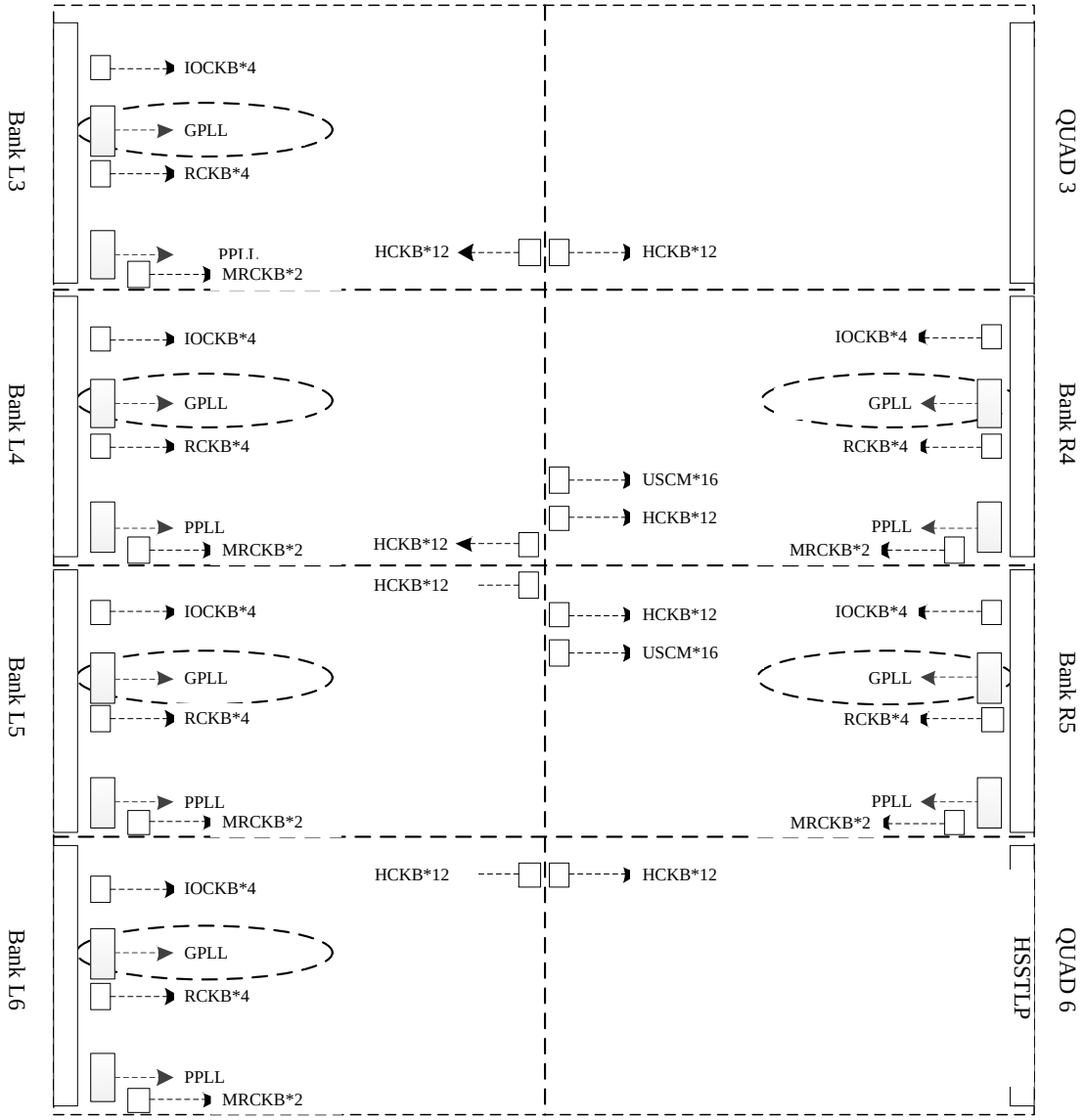

Figure 2-29 GPLL Resource Diagram (Top View)

The PGL2G100H has 6 GPLLs internally, with one GPLL in each clock region, as shown in the figure above. The GPLL has the following main features: clock frequency synthesis, clock deskew, phase adjustment, spread spectrum output, clock cascade, output clock gating, APB dynamic reconfiguration, etc.

The block diagram of the GTP_GPLL system is as shown below:

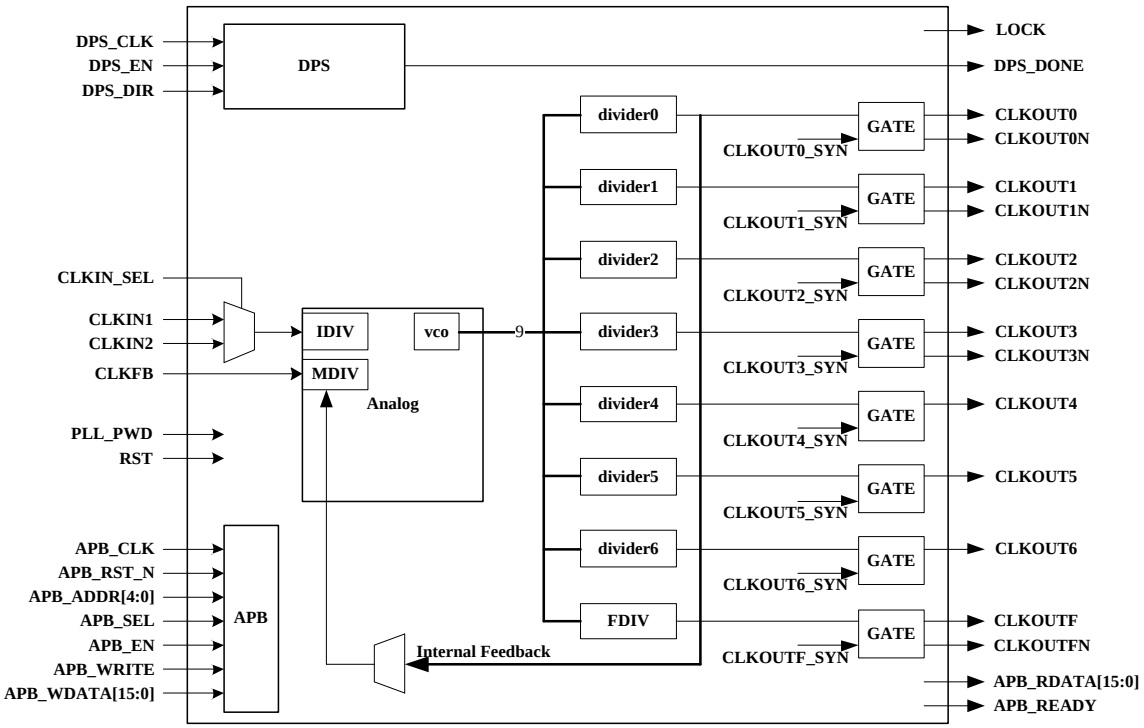

Figure 2-30 GPLL System Block Diagram

During use, the GTP_GPLL instance can be configured. Unused output ports can be disabled to reduce power consumption. Below is an introduction to the application of GTP_GPLL.

2.8.2 Top Layer Block Diagram of GTP_GPLL

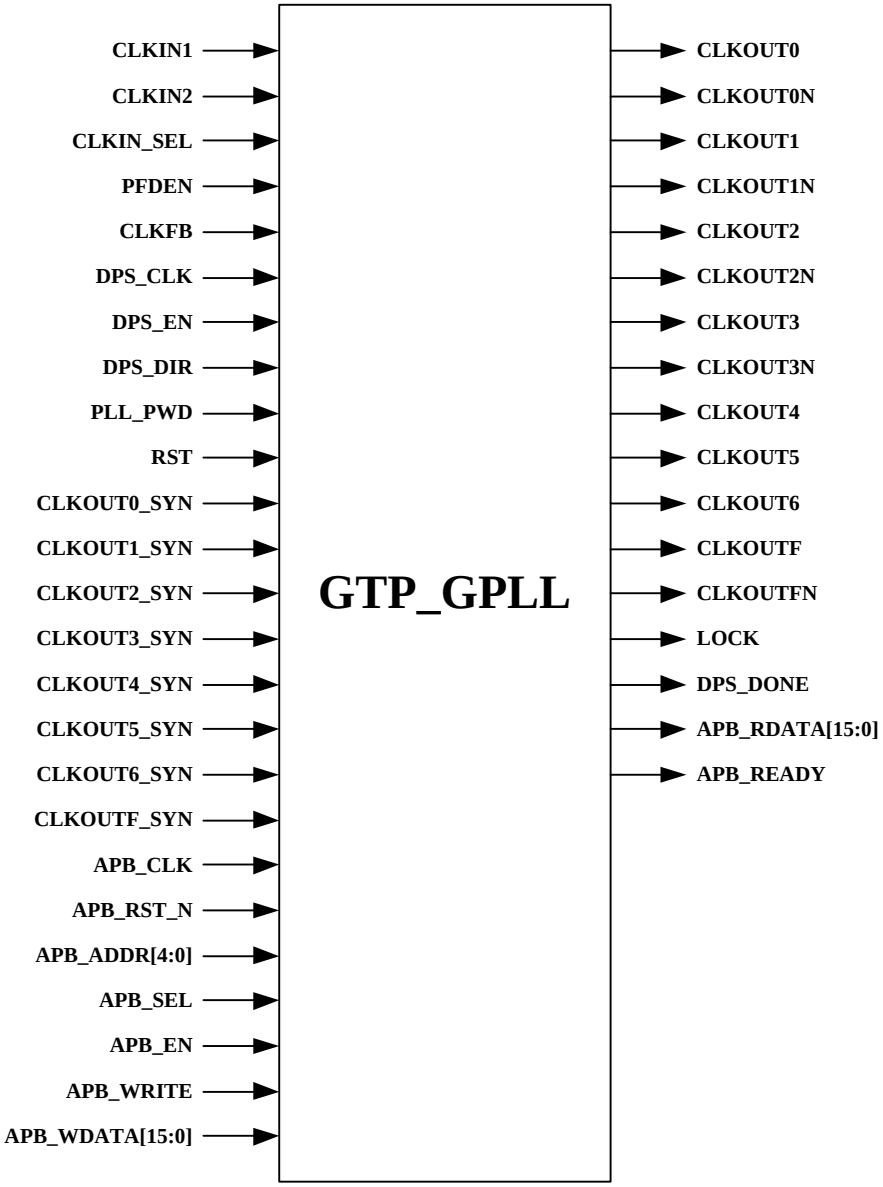

Figure 2-31 GTP_GPLL Block Diagram

2.8.3 GTP_GPLL Port List

Table 2-20 GTP_GPLL Port Description

Port	I/O	Function Description
CLKOUT0	O	PLL Channel 0 Output Clock;
CLKOUT0N	O	PLL Channel 0 Inverted Output Clock;
CLKOUT1	O	PLL Channel 1 Output Clock;
CLKOUT1N	O	PLL Channel 1 Inverted Output Clock;
CLKOUT2	O	PLL Channel 2 Output Clock;
CLKOUT2N	O	PLL Channel 2 Inverted Output Clock;
CLKOUT3	O	PLL Channel 3 Output Clock;
CLKOUT3N	O	PLL Channel 3 Inverted Output Clock;
CLKOUT4	O	PLL Channel 4 Output Clock;
CLKOUT5	O	PLL Channel 5 Output Clock;
CLKOUT6	O	PLL Channel 6 Output Clock;
CLKOUTF	O	PLL Feedback Output Clock;
CLKOUTFN	O	PLL Feedback Inverted Output Clock;
LOCK	O	PLL frequency lock indicator signal, asynchronous signal; When the signal is pulled high, it indicates that the PLL feedback clock signal is locked to the input clock signal;
DPS_DONE	O	Dynamic interpolation phase shift adjustment indicator signal;
APB_RDATA[15:0]	O	PLL APB interface data bus data output
APB_READY	O	PLL APB interface data bus handshake signal; indicates the end of a normal bus cycle;
CLKIN1	I	PLL reference input clock 1;
CLKIN2	I	PLL reference input clock 2;
CLKFB	I	PLL feedback clock;
CLKIN_SEL	I	Input clock selection signal;
DPS_CLK	I	Dynamic interpolation phase shift adjustment clock;
DPS_EN	I	Dynamic interpolation phase shift adjustment enable; active high;
DPS_DIR	I	Select the direction for dynamic phase shift adjustment; 1'b0: lag, 1'b1: lead;
PLL_PWD	I	PLL Power Down, active high;
RST	I	PLL reset signal, active high;
CLKOUT0_SYN	I	CLKOUT0/N output clock enable control; active high; high level disable, low level enable;
CLKOUT1_SYN	I	CLKOUT1/N output clock enable control; active high; high level disable, low level enable;
CLKOUT2_SYN	I	CLKOUT2/N output clock enable control; active high; high level disable, low level enable;
CLKOUT3_SYN	I	CLKOUT3/N output clock enable control; active high; high level disable, low level enable;
CLKOUT4_SYN	I	CLKOUT4 output clock enable control; active high; high level disable, low level enable;
CLKOUT5_SYN	I	CLKOUT5 output clock enable control; active high; high level disable, low level enable;
CLKOUT6_SYN	I	CLKOUT6 output clock enable control; active high; high level disable, low level

Port	I/O	Function Description
		enable;
CLKOUTF_SYN	I	CLKOUTF/N output clock enable control; active high; high level disable, low level enable;
APB_CLK	I	PLL APB interface data bus clock;
APB_RST_N	I	PLL APB interface data bus asynchronous reset signal, active low;
APB_ADDR	I	PLL APB interface data bus address;
APB_SEL	I	PLL APB interface data bus selection signal to select the slave device;
APB_EN	I	PLL APB interface data bus enable signal;
APB_WRITE	I	PLL APB interface data bus write enable signal; 1'b0: read operation, 1'b1: write operation;
APB_WDATA[15:0]	I	PLL APB interface data bus data input;

2.8.4 GTP_GPLL Parameter List

Table 2-21 GTP_GPLL Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
CLKIN_FREQ	real	10~800	Input clock frequency configuration, MHz;
LOCK_MODE	binary	1'b0, 1'b1	PLL frequency detection mode configuration; 1'b0: Real-time monitoring of PLL working state; 1'b1: The PLL lock remains after locking, unless reset or power-down;
STATIC_RATIOI	interger	1-80	Input divider ratio static configuration;
STATIC_RATIOM	interger	1-128	Feedback M divider ratio dynamic configuration;
STATIC_RATIO0	real	1-128 or 2.000~128.000, step 0.125	Output divider0 ratio static configuration; Integer division mode: supports 1~128; Fractional division mode, supports 2.000~128.000;
STATIC_RATIO1	interger	1-128	Output divider1 ratio static configuration;
STATIC_RATIO2	interger	1-128	Output divider2 ratio static configuration;
STATIC_RATIO3	interger	1-128	Output divider3 ratio static configuration;
STATIC_RATIO4	interger	1-128	Output divider4 ratio static configuration;
STATIC_RATIO5	interger	1-128	Output divider5 ratio static configuration;
STATIC_RATIO6	interger	1-128	Output divider6 ratio static configuration;
STATIC_RATIOF	real	1-128 or 2.000~128.000 step 0.125	Feedback F divider ratio static configuration; Integer division mode: supports 1~128; Fractional division mode, supports 2.000~128.000;
STATIC_DUTY0	interger	2~255	Output divider0 duty static configuration;
STATIC_DUTY1	interger	2~255	Output divider1 duty static configuration;
STATIC_DUTY2	interger	2~255	Output divider2 duty static configuration;
STATIC_DUTY3	interger	2~255	Output divider3 duty static configuration;

Parameter Name	Parameter Type	Valid Values	Function Description
STATIC_DUTY4	interger	2~255	Output divider4 duty static configuration;
STATIC_DUTY5	interger	2~255	Output divider5 duty static configuration;
STATIC_DUTY6	interger	2~255	Output divider6 duty static configuration;
STATIC_DUTYF	interger	2~255	Feedback F divider duty static configuration;
STATIC_PHASE	interger	0-63	Interpolation phase shift static configuration;
STATIC_PHASE0	interger	0-7	Output divider0 fine phase static configuration;
STATIC_PHASE1	interger	0-7	Output divider1 fine phase static configuration;
STATIC_PHASE2	interger	0-7	Output divider2 fine phase static configuration;
STATIC_PHASE3	interger	0-7	Output divider3 fine phase static configuration;
STATIC_PHASE4	interger	0-7	Output divider4 fine phase static configuration;
STATIC_PHASE5	interger	0-7	Output divider5 fine phase static configuration;
STATIC_PHASE6	interger	0-7	Output divider6 fine phase static configuration;
STATIC_PHASEF	interger	0-7	Feedback F divider fine phase static configuration;
STATIC_CPHASE0	interger	0-127	Output divider0 coarse phase static configuration;
STATIC_CPHASE1	interger	0-127	Output divider1 coarse phase static configuration;
STATIC_CPHASE2	interger	0-127	Output divider2 coarse phase static configuration;
STATIC_CPHASE3	interger	0-127	Output divider3 coarse phase static configuration;
STATIC_CPHASE4	interger	0-127	Output divider4 coarse phase static configuration;
STATIC_CPHASE5	interger	0-127	Output divider5 coarse phase static configuration;
STATIC_CPHASE6	interger	0-127	Output divider6 coarse phase static configuration;
STATIC_CPHASEF	interger	0-127	Feedback F divider coarse phase static configuration;
CLK_DPS0_EN	string	"FALSE", "TRUE"	Output divider0 interpolation phase shift enable;
CLK_DPS1_EN	string	"FALSE", "TRUE"	Output divider1 interpolation phase shift enable;
CLK_DPS2_EN	string	"FALSE", "TRUE"	Output divider2 interpolation phase shift enable;
CLK_DPS3_EN	string	"FALSE", "TRUE"	Output divider3 interpolation phase shift enable;
CLK_DPS4_EN	string	"FALSE", "TRUE"	Output divider4 interpolation phase shift enable;
CLK_DPS5_EN	string	"FALSE", "TRUE"	Output divider5 interpolation phase shift enable;
CLK_DPS6_EN	string	"FALSE", "TRUE"	Output divider6 interpolation phase shift enable;
CLK_DPSF_EN	string	"FALSE", "TRUE"	Feedback F divider interpolation phase

Parameter Name	Parameter Type	Valid Values	Function Description
			shift enable;
CLK_CAS5_EN	string	"FALSE", "TRUE"	Output divider5 clock cascade enable;
CLKOUT0_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT0_SYN signal enable;
CLKOUT1_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT1_SYN signal enable;
CLKOUT2_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT2_SYN signal enable;
CLKOUT3_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT3_SYN signal enable;
CLKOUT4_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT4_SYN signal enable;
CLKOUT5_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT5_SYN signal enable;
CLKOUT6_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT6_SYN signal enable;
CLKOUTF_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUTF_SYN signal enable;
SSC_MODE	string	"DOWN_LOW", "DOWN_HIGH", "CENTER_LOW", "CENTER_HIGH", "DISABLE"	SSC Mode Configuration;
SSC_FREQ	real	25~250	SSC modulation frequency configuration, KHz;
INTERNAL_FB	string	"CLKOUT0", "CLKOUT1", "CLKOUT2", "CLKOUT3", CLKOUT4, "CLKOUT5", "CLKOUT6", "CLKOUTF", "DISABLE"	Internal feedback path selection, choose one of the output clocks as the internal feedback clock, e.g., INTERNAL_FB = "CLKOUT0", then the output clock CLKOUT0 is used as the internal feedback clock;
EXTERNAL_FB	string	"CLKOUT0", "CLKOUT1" "CLKOUT2", "CLKOUT3", CLKOUT4, "CLKOUT5" "CLKOUT6", "CLKOUTF", "DISABLE"	External feedback path selection, choose one of the output clocks as the external feedback clock, e.g., EXTERNAL_FB = "CLKOUT0", then the output clock CLKOUT0 is used as the external feedback clock;
BANDWIDTH	string	"LOW", "HIGH" "OPTIMIZED"	Bandwidth selection configuration: BANDWIDTH = "LOW" configured as "LOW", BANDWIDTH = "HIGH" configured as "HIGH" BANDWIDTH = "OPTIMIZED" configured as "OPTIMIZED";

Note:

1. The parameters CLK_DPS5_EN and CLK_CAS5_EN cannot be configured as "TRUE" simultaneously.
2. The parameters INTERNAL_FB and EXTERNAL_FB cannot be configured as "DISABLE" simultaneously.

2.8.5 GTP_GPLL APB Interface Configuration

The user logic dynamically modifies GTP_GPLL operating parameters through the APB interface. The timing for APB interface register read and write is as shown in the following figures:

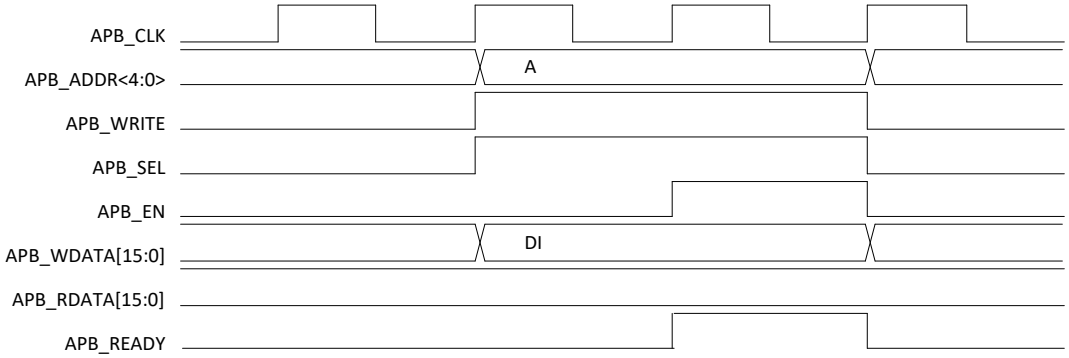

Figure 2-32 GTP_GPLL_APB Write Timing

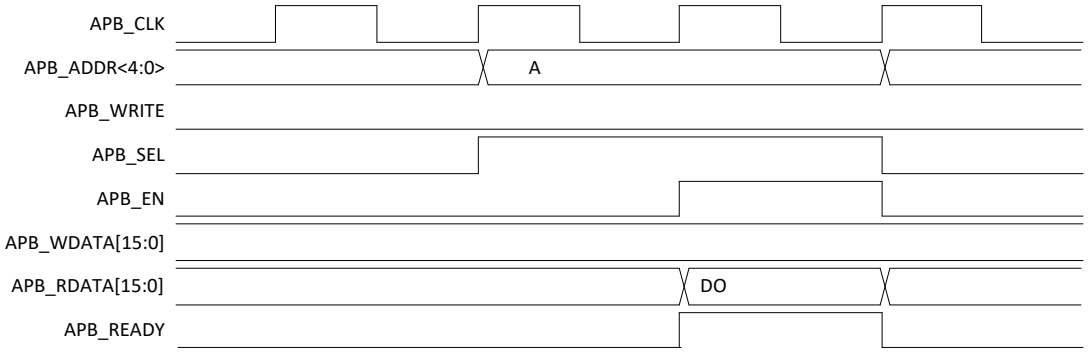

Figure 2-33 GTP_GPLL_APB Read Timing

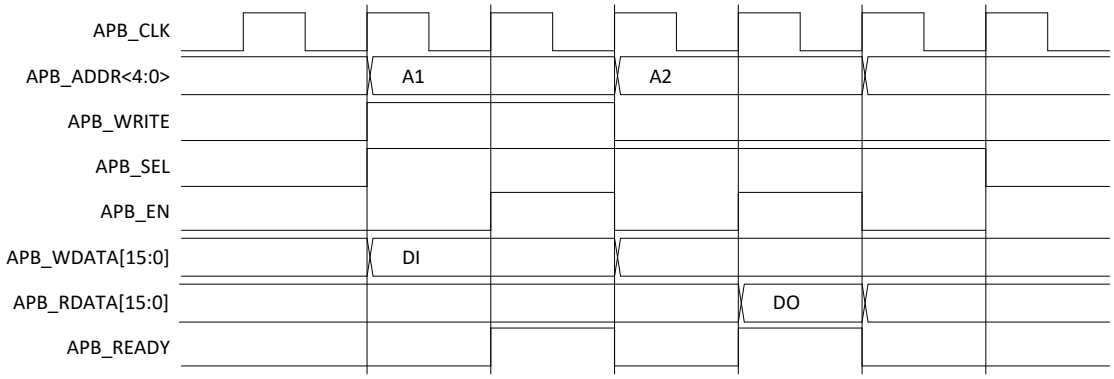

Figure 2-34 Timing of GTP_GPLL_APB Write before Read

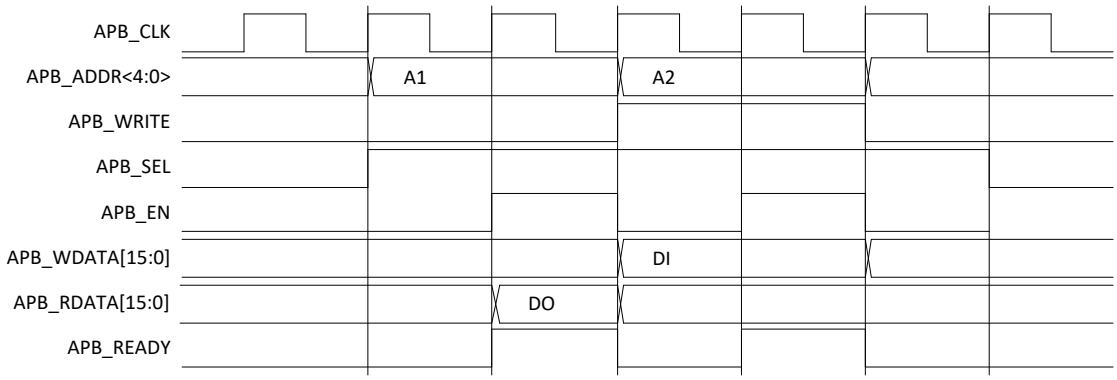

Figure 2-35 GTP_GPLL_APB Interface Read before Write Timing

Table 2-22 GTP_GPLL_APB Port Description

Series Number	Port	I/O	Description
1	APB_CLK	I	Clock, sampled on the rising edge;
2	APB_RST_N	I	Asynchronous reset, active low; resets only the data bus (does not reset register);
3	APB_ADDR[4:0]	I	Address Bus;
4	APB_SEL	I	Selection, indicating that the slave device has been selected;
5	APB_EN	I	Enable, bus enable signal;
6	APB_WRITE	I	Direction, 0: read, 1: write;
7	APB_WDATA[15:0]	I	Data bus input;
8	APB_RDATA[15:0]	O	Data bus output;
9	APB_READY	O	Flag signal, active high;

System application requirements for writing internal registers via the APB interface:

- After rewriting the internal registers via the APB interface, the PLL needs to be reset to ensure it operates properly
- T_{RST} minimum pulse width performance metrics can be found in "***DS04001_Logos2 Family FPGAs Device Data Sheet***"

Table 2-23 GTP_GPLL APB Interface Register Description

APB_ADDR[4:0]	Bit	Register	Description
0	[15:8]	REG_ODIV0_RATIO[7:0]	ODIV0 Register1: Division ratio settings;
	[7:0]	REG_ODIV0_DUTY[7:0]	ODIV0 Register1: Duty cycle settings;
1	[15:13]	REG_ODIV0_FRACDIV_RATIO[2:0]	ODIV0 Register2: Fractional setting for fractional division, range;
	[12:10]	REG_ODIV0_FRACDIV_PSOFFSET[2:0]	ODIV0 Register2: Fractional division falling edge phase settings;
	[9:7]	REG_ODIV0_FPHASE[2:0]	ODIV0 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV0_CPHASE[6:0]	ODIV0 Register2: Phase coarse adjustment settings;
2	[15:6]	RESERVED	ODIV0 Register3
	[5:4]	REG_ODIV0_ADJUST[1:0]	ODIV0 Register3: Fractional division timing adjustment settings;
	[3]	REG_ODIV0_FRACDIV_EN	ODIV0 Register3: Fractional division enable;
	[2:1]	REG_ODIV0_DPSORCAS_SEL[1:0]	ODIV0 Register3: Input clock selection;
	[0]	REG_ODIV0_MUXSEL_EN	ODIV0 Register3: Input clock MUX enable;
3	[15:8]	REG_ODIV1_RATIO[7:0]	ODIV1 Register1: Division ratio settings;
	[7:0]	REG_ODIV1_DUTY[7:0]	ODIV1 Register1: Duty cycle settings;
4	[15:13]	RESERVED	
	[12:11]	REG_ODIV1_DPSORCAS_SEL[1:0]	ODIV1 Register2: Input clock selection;
	[10]	REG_ODIV1_MUXSEL_EN	ODIV1 Register2: Input clock MUX enable;
	[9:7]	REG_ODIV1_FPHASE[2:0]	ODIV1 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV1_CPHASE[6:0]	ODIV1 Register2: Phase coarse adjustment settings;
5	[15:8]	REG_ODIV2_RATIO[7:0]	ODIV2 Register1: Division ratio settings;
	[7:0]	REG_ODIV2_DUTY[7:0]	ODIV2 Register1: Duty cycle settings;
6	[15:13]	RESERVED	
	[12:11]	REG_ODIV2_DPSORCAS_SEL[1:0]	ODIV2 Register2: Input clock selection;
	[10]	REG_ODIV2_MUXSEL_EN	ODIV2 Register2: Input clock MUX enable;
	[9:7]	REG_ODIV2_FPHASE[2:0]	ODIV2 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV2_CPHASE[6:0]	ODIV2 Register2: Phase coarse adjustment settings;
7	[15:8]	REG_ODIV3_RATIO[7:0]	ODIV3 Register1: Division ratio settings;
	[7:0]	REG_ODIV3_DUTY[7:0]	ODIV3 Register1: Duty cycle settings;
8	[15:13]	RESERVED	
	[12:11]	REG_ODIV3_DPSORCAS_SEL[1:0]	ODIV3 Register2: Input clock

APB_ADDR[4:0]	Bit	Register	Description
			selection;
	[10]	REG_ODIV3_MUXSEL_EN	ODIV3 Register2: Input clock MUX enable;
	[9:7]	REG_ODIV3_FPHASE[2:0]	ODIV3 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV3_CPHASE[6:0]	ODIV3 Register2: Phase coarse adjustment settings;
9	[15:8]	REG_ODIV4_RATIO[7:0]	ODIV4 Register1: Division ratio settings;
	[7:0]	REG_ODIV4_DUTY[7:0]	ODIV4 Register1: Duty cycle settings;
A	[15:13]	RESERVED	
	[12:11]	REG_ODIV4_DPSORCAS_SEL[1:0]	ODIV4 Register2: Input clock selection;
	[10]	REG_ODIV4_MUXSEL_EN	ODIV4 Register2: Input clock MUX enable;
	[9:7]	REG_ODIV4_FPHASE[2:0]	ODIV4 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV4_CPHASE[6:0]	ODIV4 Register2: Phase coarse adjustment settings;
B	[15:8]	REG_ODIV5_RATIO[7:0]	ODIV5 Register1: Division ratio settings;
	[7:0]	REG_ODIV5_DUTY[7:0]	ODIV5 Register1: Duty cycle settings;
C	[15:13]	RESERVED	
	[12:11]	REG_ODIV5_DPSORCAS_SEL[1:0]	ODIV5 Register2: Input clock selection;
	[10]	REG_ODIV5_MUXSEL_EN	ODIV5 Register2: Input clock MUX enable;
	[9:7]	REG_ODIV5_FPHASE[2:0]	ODIV5 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV5_CPHASE[6:0]	ODIV5 Register2: Phase coarse adjustment settings;
D	[15:8]	REG_ODIV6_RATIO[7:0]	ODIV6 Register1: Division ratio settings;
	[7:0]	REG_ODIV6_DUTY[7:0]	ODIV6 Register1: Duty cycle settings;
E	[15:13]	RESERVED	
	[12:11]	REG_ODIV6_DPSORCAS_SEL[1:0]	ODIV6 Register2: Input clock selection;
	[10]	REG_ODIV6_MUXSEL_EN	ODIV6 Register2: Input clock MUX enable;
	[9:7]	REG_ODIV6_FPHASE[2:0]	ODIV6 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV6_CPHASE[6:0]	ODIV6 Register2: Phase coarse adjustment settings;
F	[15:8]	REG_FDIV_RATIO[7:0]	FDIV Register1: Division ratio settings;
	[7:0]	REG_FDIV_DUTY[7:0]	FDIV Register1: Duty cycle settings;
10	[15:13]	REG_FDIV_FRACDIV_RATIO[2:0]	FDIV Register2: Fractional setting for fractional division;
	[12:10]	REG_FDIV_FRACDIV_PSOFFSET[2:0]	FDIV Register2: Fractional division falling edge phase settings;
	[9:7]	REG_FDIV_FPHASE[2:0]	FDIV Register2: Phase fine

APB_ADDR[4:0]	Bit	Register	Description
			adjustment settings;
	[6:0]	REG_FDIV_CPHASE[6:0]	FDIV Register2: Phase coarse adjustment settings;
11	[15:6]	RESERVED	
	[5:4]	REG_FDIV_ADJUST[1:0]	FDIV Register3: Fractional division timing adjustment settings;
	[3]	REG_FDIV_FRACDIV_EN	FDIV Register3: Fractional division enable;
	[2:1]	REG_FDIV_DPSORCAS_SEL[1:0]	FDIV Register3: Input clock selection;
	[0]	REG_FDIV_MUXSEL_EN	FDIV Register3: Input clock MUX enable;
12	[15:8]	RESERVED	
	[7:0]	REG_IDIV_RATIO[7:0]	IDIV Register: Division ratio settings;
13	[15:8]	RESERVED	
	[7:0]	REG_MDIV_RATIO[7:0]	MDIV Register: Division ratio settings;
14	[15:14]	RESERVED	BANDWIDTH Register
	[13:12]	REG_VCTRL_INIT[1:0]	
	[11:10]	REG_CP_SELFBIAS_SEL[1:0]	
	[9:8]	REG_ICP_BASE_SEL[1:0]	
	[7:4]	REG_CP_CUR_SEL<3:0>	
	[3:1]	REG_LPF_R[2:0]	
	[0]	REG_LPF_C	
15	[15:6]	RESERVED	LOCK Register
	[5]	REG_LOCK_FILTER_PD	
	[4:0]	REG_FREQ_LOCKDET_SET<4:0>	

2.8.6 GTP_GPLL Function Description

2.8.6.1 Clock Input

When CLKIN_SEL is 0, select CLKIN1; when CLKIN_SEL is 1, select CLKIN2. The reference clock dynamically switches between CLKIN1 and CLKIN2, and PLL needs to be reset after switching.

The following points should be noted regarding the GPLL input clock:

- When the input clock is lost or unstable, the GPLL needs to be reset after the input clock stabilizes.
- Upon power-up and without a reference clock, the GPLL will output a low-frequency clock signal, with the LOCK signal at a low level. To set the output clock to 0, users can use the Power-down mode or clock output gating; for details, please refer to sections 2.8.6.3 and 2.8.6.12.

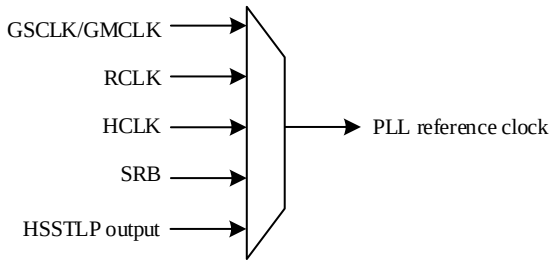

Figure 2-36 GTP_GPLL Reference Clock Source

2.8.6.2 GPLL Reset

After the RST reset signal is released, the PLL starts to enter the lock state, and the PLL frequency lock is completed after T_{LOCK} (PLL lock time). Before the LOCK signal transitions from low to high, CLKOUT will gradually begin to toggle from low level. During this time, CLKOUT is unstable. CLKOUT stabilizes only after the LOCK signal transitions to high. The timing of the RST reset signal is shown in the figure below; active high.

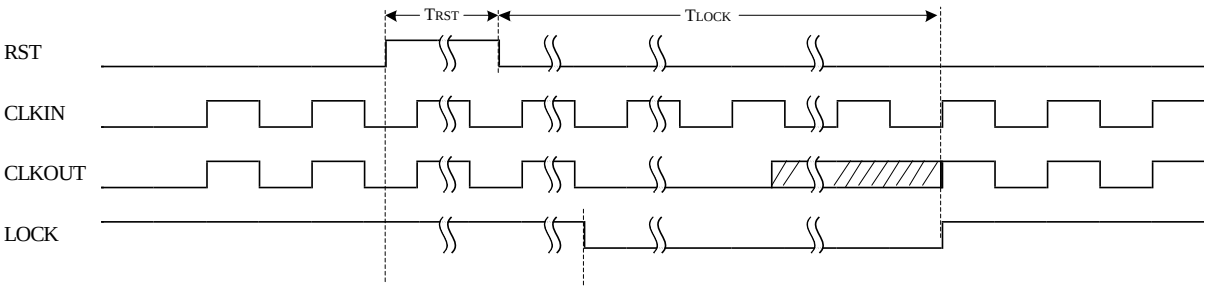

Figure 2-37 GTP_GPLL Reset Timing

For T_{RST} and T_{LOCK} performance specification, please refer to "DS04001_Logos2 Family FPGAs Device Datasheet".

2.8.6.3 GPLL Power Down

When the PLL is not in use, the PLL power can be turned off by setting the PLL_PWD signal to a high level, thus saving power consumption. If the PLL is to be used again, set the PLL_PWD signal to a low level. After T_{LOCK} time, the PLL will relock. Before the LOCK signal transitions from low to high, CLKOUT will gradually begin to toggle from low level. During this time, CLKOUT is unstable. CLKOUT stabilizes only after the LOCK signal transitions to high.

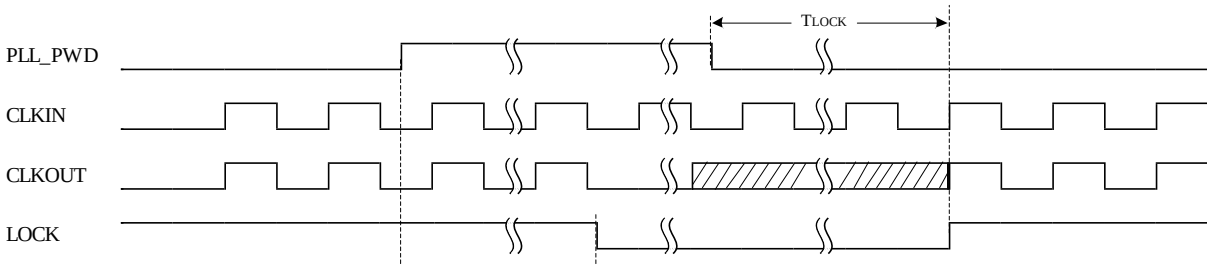

Figure 2-38 GTP_GPLL Power Down Timing

2.8.6.4 Feedback Clock Selection

The feedback clock input source of the GPLL can be divided into GPLL internal feedback and GPLL external feedback. The feedback sources support CLKOUT0~ CLKOUT6, CLKOUTF.

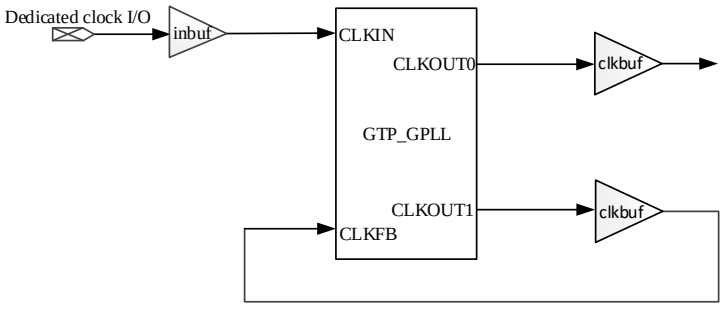

Figure 2-39 GTP_GPLL External Feedback Diagram

As shown in the figure, when external feedback is selected, the feedback clock reaches the feedback clock input through the global clock or horizontal clock buffer along a dedicated clock path. In internal feedback mode, the feedback clock output directly reaches the feedback clock input within the PLL, receiving less interference compared to external feedback.

Table 2-24 Feedback Clock Selection

INTERNAL_FB	EXTERNAL_FB	Feedback Mode
"CLKOUT0"	"DISABLE"	Internal feedback mode, select output divider0;
"CLKOUT1"	"DISABLE"	Internal feedback mode, select output divider1;
"CLKOUT2"	"DISABLE"	Internal feedback mode, select output divider2;
"CLKOUT3"	"DISABLE"	Internal feedback mode, select output divider3;
"CLKOUT4"	"DISABLE"	Internal feedback mode, select output divider4;
"CLKOUT5"	"DISABLE"	Internal feedback mode, select output divider5;
"CLKOUT6"	"DISABLE"	Internal feedback mode, select output divider6;
"CLKOUTF"	"DISABLE"	Internal feedback mode, select feedback F divider;
"DISABLE"	"CLKOUT0"	External feedback mode, select output divider0;
"DISABLE"	"CLKOUT1"	External feedback mode, select output divider1;
"DISABLE"	"CLKOUT2"	External feedback mode, select output divider2;
"DISABLE"	"CLKOUT3"	External feedback mode, select output divider3;
"DISABLE"	"CLKOUT4"	External feedback mode, select output divider4;
"DISABLE"	"CLKOUT5"	External feedback mode, select output divider5;
"DISABLE"	"CLKOUT6"	External feedback mode, select output divider6;
"DISABLE"	"CLKOUTF"	External feedback mode, select feedback F divider;

2.8.6.5 Output Frequency Programming

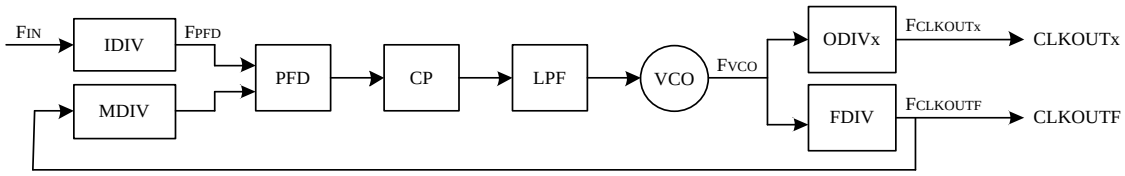

Figure 2-40 GTP_GPLL Output Frequency Path Diagram

The reference clock (Fin) passes through a programmable input divider (IDIV) to obtain a reference clock for the phase frequency detector (PFD). The feedback clock passes through programmable feedback dividers (FDIV) and (MDIV) to obtain another reference clock for the PFD. The PFD compares the phase and frequency of these two clocks and then generates a signal to drive the charge pump (CP). The current signal generated by the CP passes through the loop filter (LPF), and the LPF produces a reference voltage for the voltage-controlled oscillator (VCO). The PFD provides phase lead or lag signals to the CP and LPF to continuously adjust the VCO operating frequency, thus regulating the frequency and phase. For example, if the VCO remains higher than the reference frequency after passing through the feedback divider, the PFD generates a downward adjustment signal, causing the CP and LPF to decrease the voltage and control the VCO to lower the output frequency. If the VCO remains lower than the reference frequency after passing through the

feedback divider, the PFD generates an upward adjustment signal, causing the CP and LPF to increase the voltage and control the VCO to raise the output frequency. The VCO generates 8 phase output clocks. Using these 8 phase clocks, one variable phase shift clock can be generated to achieve coarse phase adjustment, fine phase adjustment, and interpolation phase shift. Each output phase shift clock can serve as an input for the FDIV. There are 8 output dividers in total: 7 ODIV and 1 FDIV. Each divider is independent. The final output clock frequency is obtained by VCO output clock through these dividers.

Table 2-25 Descriptions for Output Frequency Programming Parameters

Parameter Name	**Function Description**
F_{IN}	Input Clock Frequency
F_{PFD}	Input reference clock frequency of PFD
F_{VCO}	Output clock frequency of VCO
$F_{CLKOUTx}$	Output clock frequency of CLKOUT0-6
$F_{CLKOUTF}$	Output clock frequency of CLKOUTF
IDIV	The division ratio of the input divider
MDIV	The division ratio of the feedback divider M
ODIVx	The division ratio of the CLKOUT0-6 divider
FDIV	The division ratio of the feedback divider F

Note: IDIV corresponds to the parameter STATIC_RATIOI, MDIV corresponds to the parameter STATIC_RATIOM, ODIV0~6 corresponds to the parameter STATIC_RATIO0~6, FDIV corresponds to the parameter STATIC_RATIOF

If the division ratio of the feedback divider selected for internal or external feedback is FBDIV, the clock frequency calculation formulas are as follows:

$$F_{PFD} = \frac{F_{IN}}{IDIV}$$

$$F_{VCO} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV}$$

$$F_{CLKOUTx} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times ODIVx}$$

$$F_{CLKFBOUT} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times FDIV}$$

Where FBDIV is the division ratio selected for the feedback loop, FBDIV∈[ODIV0~6, FDIV]. For example, when the feedback clock is CLKOUT0, FBDIV = ODIV0.

The output clocks CLKOUT0 and CLKOUTF support both integer division mode and fractional division mode.

- ODIV0 Division Ratio

$$\text{ODIV0} = \text{CLKOUT0 Integer Division Ratio} + \text{CLKOUT0 Fractional Division Ratio}$$

The division ratio of ODIV0 corresponds to the value of the parameter STATIC_RATIO0.

- FDIV Division Ratio

$$\text{FDIV} = \text{CLKOUTF Integer Division Ratio} + \text{CLKOUTF Fractional Division Ratio}$$

The division ratio of FDIV corresponds to the value of the parameter STATIC_RATIOF.

2.8.6.6 Loop bandwidth

The GPLL loop bandwidth can be configured to low bandwidth (LOW), medium bandwidth (OPTIMIZED) and high bandwidth (HIGH). The parameters for low and medium bandwidth configurations are identical.

Considering that in actual applications the input clock is not ideal, different bandwidth configurations affect the PLL differently:

- If a smaller jitter is desired for PLL output clock, it can be configured to low bandwidth or medium bandwidth, resulting in a longer locking time
- If a shorter locking time is desired for PLL, it can be configured to high bandwidth, at the cost of increased output clock jitter

2.8.6.7 Fractional Division

ODIV0 and FDIV support both integer division and fractional division modes.

- Fractional division (accuracy: 0.125)
- Fractional division mode does not support interpolative phase shift in static phase shift mode or dynamic phase shift mode
- The duty cycle in fractional division mode is not programmable

If the fractional division ratio is N.f, the calculation formula for the duty cycle is as follows:

$$\text{DutyCycle} = 50\% + \frac{\alpha}{2\left(8\text{N} + \frac{\text{f}}{0.125}\right)}$$

Where $\frac{f}{0.125} = \text{Odd}$, $\alpha = 1$, $\frac{f}{0.125} = \text{Even}$, $\alpha = 0$;

Example: With the integer part of the division factor ODIV0 STATIC VALUE = 24 and the fractional part of the division factor ODIV0 FRACTION VALUE = 1/8, it can be calculated that N = 24, f = 0.125, $\alpha = 1$, DutyCycle = 50% + 1/2 (8*24 + 1) = 50.259%.

Only the output clocks CLKOUT0 and CLKOUTF support fractional division. Fractional division for CLKOUT0 is configured via the parameter STATIC_RATIO0, and for CLKOUTF via the parameter STATIC_RATIOF. For instance, to set the division ratio for CLKOUT0 to 2.125, assign 2.125 to the parameter STATIC_RATIO0. The same applies to the configuration of CLKOUTF. It should be noted that the output clock frequency must be within the configurable range.

2.8.6.8 Phase Adjustment

Phase adjustment includes three methods: phase coarse adjustment, phase fine adjustment, and interpolative phase shift. Both phase coarse and fine adjustments can be made in the static configuration mode or through the APB interface. These two adjustment methods are independent for each output clock. The interpolative phase shift can be configured statically or dynamically via the DPS interface, affecting all output clocks that choose this mode. It should be noted that the output clock used as feedback cannot have its phase adjusted.

- Phase adjustment method:
  - Phase coarse adjustment

    Phase coarse adjustment for the output clock CLKOUT0/1/2/3/4/5/6/F can be achieved through configuration parameters STATIC_CPHASE0/1/2/3/4/5/6/F.

    With respect to the input VCO clock, the step for CLKOUT0/1/2/3/4/5/6/F phase coarse adjustment of the output clock is Tvco, with an adjustment range of [0-Ndiv-1]*Tvco and a step for adjustment degree of 360 °/Ndiv.

    Ndiv is the output division ratio ODIVx or the feedback division ratio FDIV.

  - Phase fine adjustment

    Phase fine adjustment for the output clock CLKOUT0/1/2/3/4/5/6/F can be achieved through configuration parameters STATIC_PHASE0/1/2/3/4/5/6/F.

    With respect to the input VCO clock, the minimum step for CLKOUT0/1/2/3/4/5/6/F phase fine adjustment of the output clock is Tvco/8 (the adjustment range is (0-7/8)Tvco) with a step for adjustment degree of 45 °/Ndiv and an adjustment range of (0 °-45 °*7)/Ndiv.

- Interpolative phase shift

  Static interpolative phase shift for CLKOUT0/1/2/3/4/5/6/F can be achieved through configuration parameter STATIC_PHASE and enable signal CLK_DPS0/1/2/3/4/5/6/F_EN. All output clocks share the parameter STATIC_PHASE. If you need to configure the static interpolative phase shift function for CLKOUT0, it is required to set CLK_DPS0_EN to "TRUE" and set the value of STATIC_PHASE.

  Dynamic interpolative phase shift for CLKOUT0/1/2/3/4/5/6/F can be achieved through enable signal CLK_DPS0/1/2/3/4/5/6/F_EN and the DPS port. All output clocks share one DPS interface. If you need to configure the static interpolative phase shift function for CLKOUT0, it is required to set CLK_DPS0_EN to "TRUE", and then dynamically adjust the output clock phase of CLKOUT0 through the DPS interface.

  With respect to the input VCO clock, the interpolative phase shift precision for output CLKOUT0/1/2/3/4/5/6/F is Tvco/64, with a step for adjustment degree of 360 °/(64*Ndiv).

  Dynamic phase adjustment uses interpolative phase shift, where the output clock can achieve 360-degree cyclic rotation. For details, please refer to the section "Dynamic Adjustment".

  Notes:

  1. Ndiv∈{STATIC_RATIO0~6, STATIC_RATIOF}, is the division factor for output clock CLKOUT0/1/2/3/4/5/6/F

  2. During phase adjustment, only one method (phase fine adjustment or interpolative phase shift) can be selected to use with phase coarse adjustment to achieve output clock phase adjustment.

➢ Phase adjustment mode

- Static configuration

  The static configuration for phase fine adjustment of the output clock CLKOUT0/1/2/3/4/5/6/F is controlled by the parameter STATIC_PHASE0/1/2/3/4/5/6/F respectively.

  The static configuration for phase coarse adjustment of the output clock CLKOUT0/1/2/3/4/

  5/6/F is controlled by the parameter STATIC_CPHASE0/1/2/3/4/5/6/F respectively.

  The static configuration of the interpolative phase shift of the output clock CLKOUT0/1/2/3/

  4/5/6/F is controlled by the parameter STATIC_PHASE.

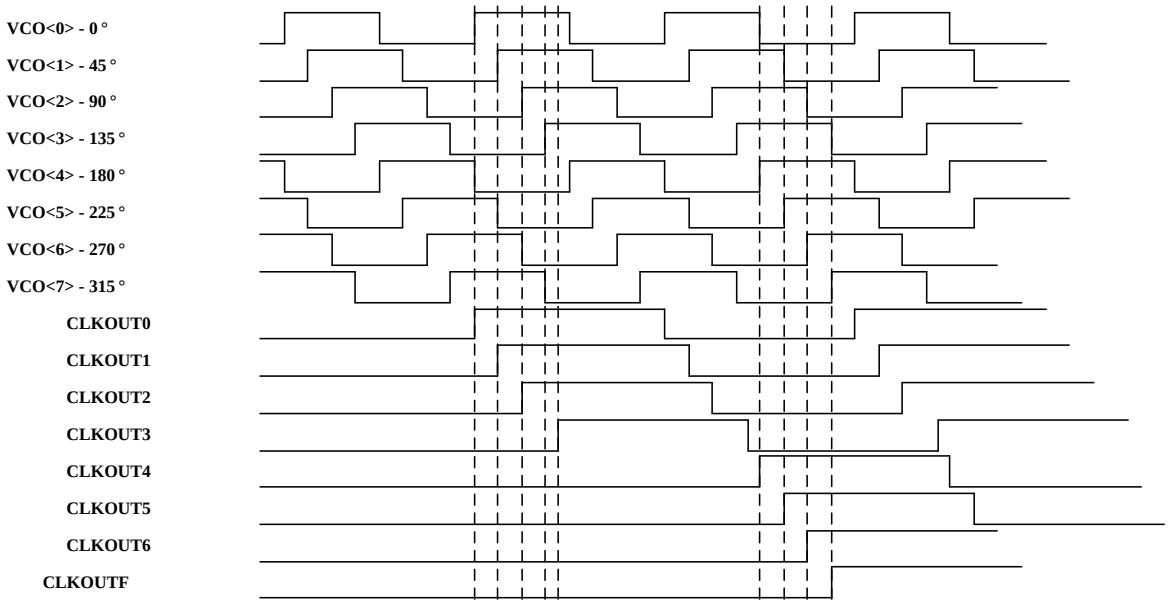

Figure 2-41 GTP_GPLL Static Phase Adjustment Configuration

As shown in the table below, CLKOUT0 is generated by VCO<0> divide-by-two, with a phase fine adjustment of 0 and a phase coarse adjustment of 0. With CLKOUT0 as the reference, the phase relationship of each output clock is as follows:

Table 2-26 The Phase Relationship of the Output Clock

Output clock	Phase Fine Adjustment	Phase Coarse Adjustment	Interpolative phase shift	Phase Relationship
CLKOUT0	0	0	---	0
CLKOUT1	1*Tvco/8	0	---	22.5 °
CLKOUT2	2*Tvco/8	0	---	45 °
CLKOUT3	0	0	28*Tvco/64	78.75 °
CLKOUT4	4*Tvco/8	Tvco	---	270 °
CLKOUT5	5*Tvco/8	Tvco	---	292.5 °
CLKOUT6	6*Tvco/8	Tvco	---	315 °
CLKOUTF	7*Tvco/8	Tvco	---	337.5 °

- Dynamic adjustment

  The GTP_GPLL module of the LOGOS2 family devices supports dynamic phase adjustment and the interface for dynamic phase shift adjustment. Dynamic phase adjustment allows the phase of PLL output clock to be dynamically adjusted relative to the reference clock. The dynamic phase adjustment function is achieved through four signals: DPS_CLK, DPS_EN, DPS_DIR and DPS_DONE. With DPS_DIR set, the phase can be increased or decreased. Each adjustment changes the output clock phase of GPLL by

1/64*Tvco. There is no maximum phase adjustment value; any clock frequency can achieve 360 °phase adjustment. After one cycle ends, the phase adjustment will start again. The dynamic phase adjustment process is shown in the figure below, where DPS_EN, DPS_DIR and DPS_DONE are synchronised to DPS_CLK clock domain. When DPS_EN is high (for one DPS_CLK clock cycle), phase adjustment is initialised. The phase is increased when DPS_DIR is low, and the phase is decreased when DPS_DIR is high. When phase adjustment is complete, DPS_DONE remains high for one DPS_CLK cycle. The entire adjustment process lasts for 15 clock cycles.

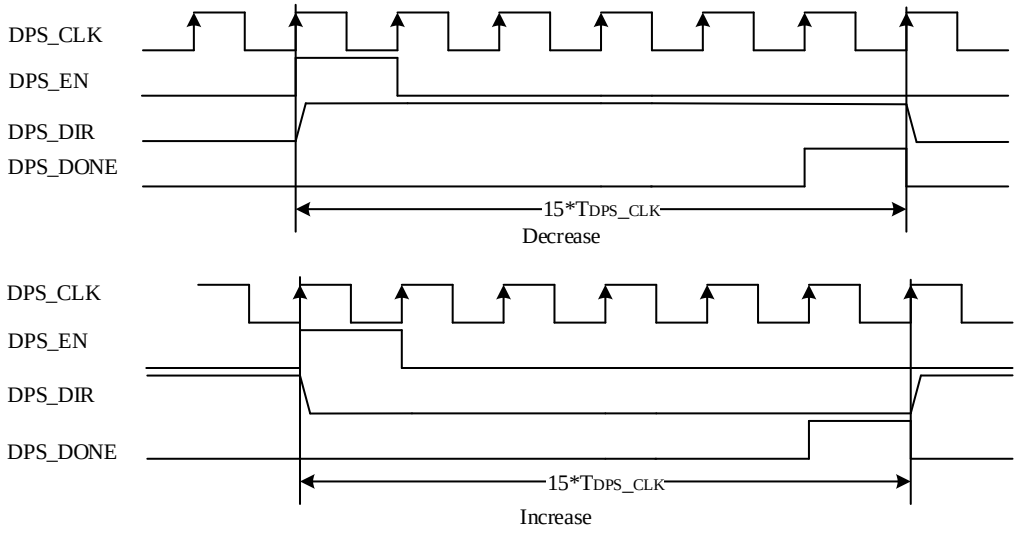

Figure 2-42 GTP_GPLL Dynamic Phase Shift Mode Interface Timing

The dynamic phase shift interface is shown in the table below:

Table 2-27 Dynamic Phase Shift Port Description

Series Number	Port	I/O	Description	Initial Value
1	DPS_CLK	I	Dynamic Phase Adjustment Clock Signal;	
2	DPS_EN	I	Dynamic Phase Adjustment Enable Signal;	
3	DPS_DIR	I	Direction control for dynamic phase adjustment; 1'b0: increase, 1'b1: decrease	
4	DPS_DONE	O	Indication signal for the completion of dynamic phase adjustment;	1'b0

Notes: For DPS_CLK performance specifications, please refer to the "***DS04001_Logos2 Family FPGA Device Datasheet***"

2.8.6.9 Programmable Duty Cycle

The output divider supports a programmable duty cycle with a minimum step of 50%/odiv, where odiv is the division factor of the output clock divider. STATIC_DUTY0/1/2/3/4/5/6/F determines the duty cycle after division, the expression is as follows, where duty is the duty cycle configuration value.

duty cycle = (50%/odiv)*duty.

For example, if odiv is 24, then according to the formula, the configurable range for duty is 2-47, and the duty cycle range is 4.17%-97.92%.

Attention:

1. The duty value is restricted by the odiv value (output division): when odiv > 1, 2 <= duty <= 2*odiv-1; when odiv = 1, duty is invalid and does not work, and the default output is 50%.

2. Fractional division does not support duty cycle programming.

2.8.6.10 Spread Spectrum Clock Generation and Input

- Supports spread spectrum clock input with modulation frequency less than GPLL bandwidth
- Supports local spread spectrum clock generation, with support for both centre spread and down spread modes
- The maximum values of CENTER_HIGH, CENTER_LOW, DOWN_HIGH and DOWN_LOW are ±2%, ±1%, -2% and -1%.

The centre spread spectrum is shown in the figure below, where the solid line with greater amplitude represents high centre spread spectrum modulation, and the solid line with lower amplitude represents low centre spread spectrum modulation.

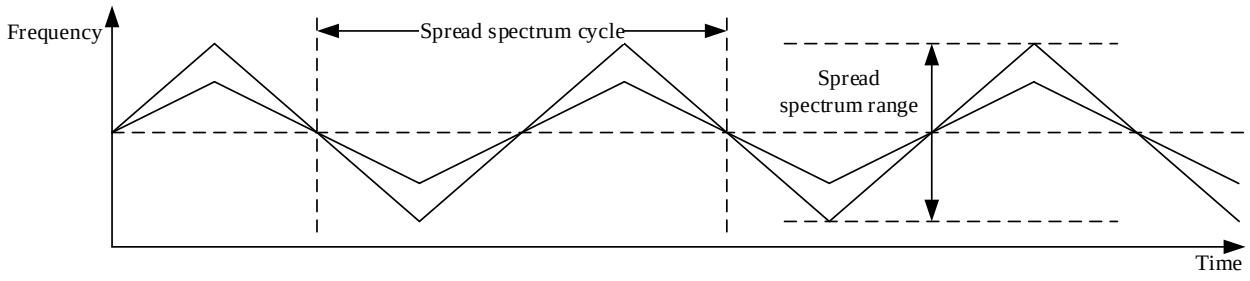

Figure 2-43 Diagram of GPLL Centre Spread Spectrum

The down spread spectrum is shown in the figure below, where the solid line with greater amplitude represents high down spread spectrum modulation, and the solid line with lower amplitude represents low down spread spectrum modulation.

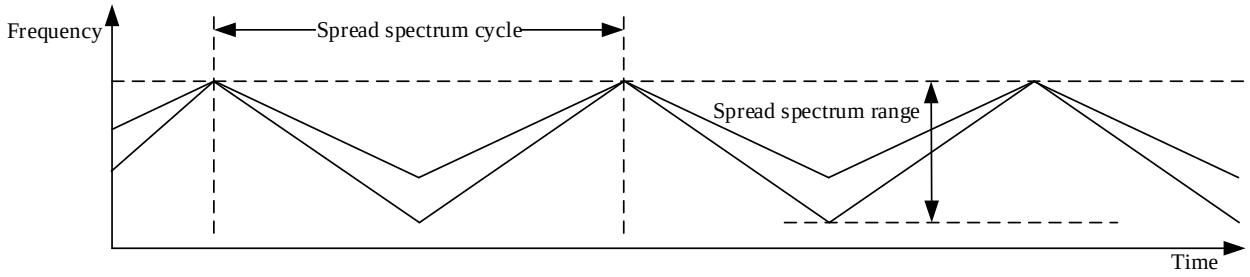

Figure 2-44 Diagram of GPLL Down Spread Spectrum

When GPLL operates in SSC mode, the original clock resources are needed to generate the spread spectrum clock, therefore:

- CLKOUT2/N and CLKOUT3/N are no longer used independently
- The dynamic phase shift mode is no longer used

2.8.6.11 Clock Output Cascading

When CLK_CAS5_EN is configured as "TRUE", output divider 5 and output divider 6 can achieve clock cascading.

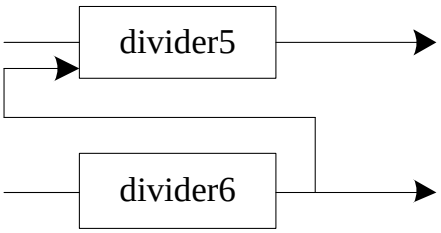

Figure 2-45 GTP_GPLL OUTPUT Divider Output Cascading

After cascading, the output clock CLKOUT5 has a fixed phase shift with other output clocks.

2.8.6.12 Clock Output Gating

The GTP_GPLL input signal CLKOUT0_SYN is used to enable and disable CLKOUT0 output clock; when the CLKOUT0 clock is not required, it can be turned off to reduce the power consumption of Clock Tree and Fabric.

The CLKOUT0_SYN signal is optional and is active when the user sets CLKOUT0_SYN_EN to "TRUE."

Similarly, the input signals CLKOUT1~6/F_SYN respectively work in conjunction with the configuration bits CLKOUT1~6/F_SYN_EN, enabling and disabling the CLKOUT1~6/F clocks.

Taking the output clock CLKOUT0 as an example, when the CLKOUT0_SYN level is in transition from 0 to 1, after 3 CLKIN falling edges CLKOUT0 outputs a low level, and when the CLKOUT0_SYN level is in transition from 1 to 0, after 3 CLKIN falling edges the CLKOUT0 output is valid. The functional diagram is shown in the following figure:

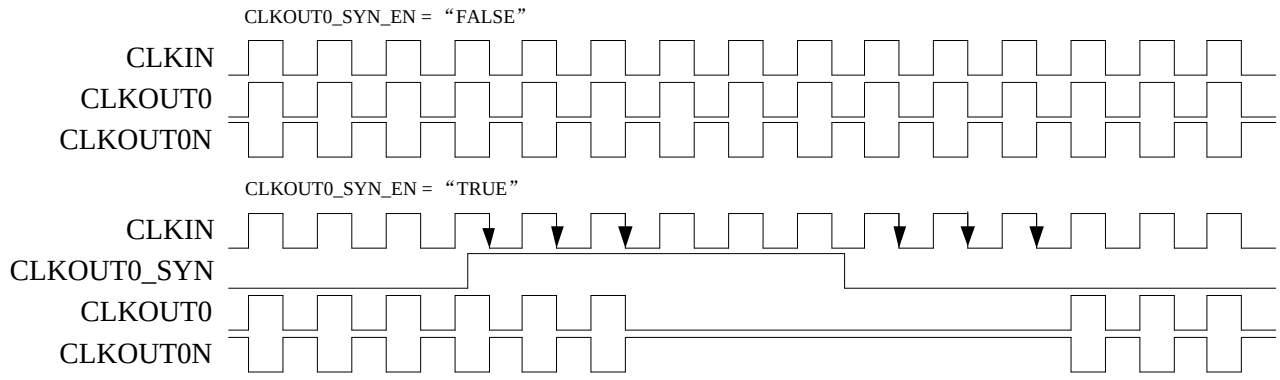

Figure 2-46 The Timing Diagram of GTP_GPLL Output Clock GATE

2.8.6.13 LOCK Indication

GPLL supports two types of LOCK modes, which are selected by the configuration parameter LOCK_MODE.

Table 2-28 GPLL LOCK Indication Modes

Parameter	**Parameter Value**	**Function Description**
LOCK_MODE	0	PLL LOCK status is monitored in real time, if it enters an abnormal state, LOCK will be pulled down
	1	LOCK does not monitor (indicate) PLL operating state in real time; once LOCK is pulled high it will not be pulled down again until LOCK reset or Power Down

2.8.7 GTP_GPLL Configuration Constraints

In actual application, to achieve certain functions, it is necessary to configure the relevant parameters. The configurable ranges of these parameters affect each other. Once a parameter is determined, the configurable ranges of the other parameters will be constrained, rather than being configurable within their entire ranges. If the parameters are not configured correctly, it may lead to abnormal GPLL operation. Therefore, when configuring these parameters, it should be noted that the constraints and configurable ranges of the relevant parameters.

GPLL can be configured in two ways: one is implemented through the GUI (IP compiler in the development tool), please refer to "***UG041001_28nm_PLL_IP_UserGuide***" for detailed usage, available in the IP configuration interface; the other way is to configure relevant parameters according to instantiate GTP, combined with the GPLL Advanced mode in the IP compiler to understand configuration constraints, for example, if some parameter settings are out of range, an error will be reported when the IP is generated, with the configurable range indicated.

For the configurable ranges of the parameters, please refer to Table 2-21 and "***DS04001_Logos2 Series FPGA Device Datasheet***".

Output Clock Frequency Constraints:

One of the most common functions of GPLL is to configure the desired output frequency, the following factors need to be considered:

- The selected input frequency must be within the configurable range
- The output clock frequency must be within the configurable range
- The PFD frequency must be within the configurable range
- The input division parameter IDIV, the output division parameter ODIV, the feedback division parameters MDIV and FBDIV must be within the configurable range
- The VCO frequency range must be within the specified range

Suppose the desired output clock frequency is 100 MHz, the input clock frequency selected is 50 MHz;

The PFD frequency should be considered first. According to the formula, since the input clock frequency is 50 MHz and the PFD frequency range is from 10 MHz to 450 MHz, the configurable range for IDIV is from 1 to 5. Suppose that 1 is chosen, and the internal feedback mode is selected, the feedback output clock frequency is 50 MHz, maintaining consistency with the input clock frequency. At this time, FBDIV = FDIV, and according to the formula, MDIV = 1.

The parameters determined from the above two steps are: CLKIN1 = 50 MHz, PFD frequency = 50 MHz, CLKOUT0 = 100 MHz, IDIV = MDIV = 1.

Then, according to the VCO formula and the VCO frequency range, the configurable range for FBDIV is obtained as 12 to 24. If 24 is chosen, according to the output clock frequency formula, ODIV0 = 6, and the VCO frequency is 1200 MHz.

Through these steps, we can obtain a valid output clock frequency.

2.8.8 GTP_GPLL Application Mode

2.8.8.1 Internal Feedback Mode

Internal feedback mode mainly targets certain application scenarios where high performance of GPLL output clock is required, such as frequency synthesis, low jitter clock output, etc.

In the internal feedback mode, the feedback clock is directly connected to the input of GPLL without passing through any other circuitry, thus eliminating noises introduced by other circuits and achieving better jitter performance.

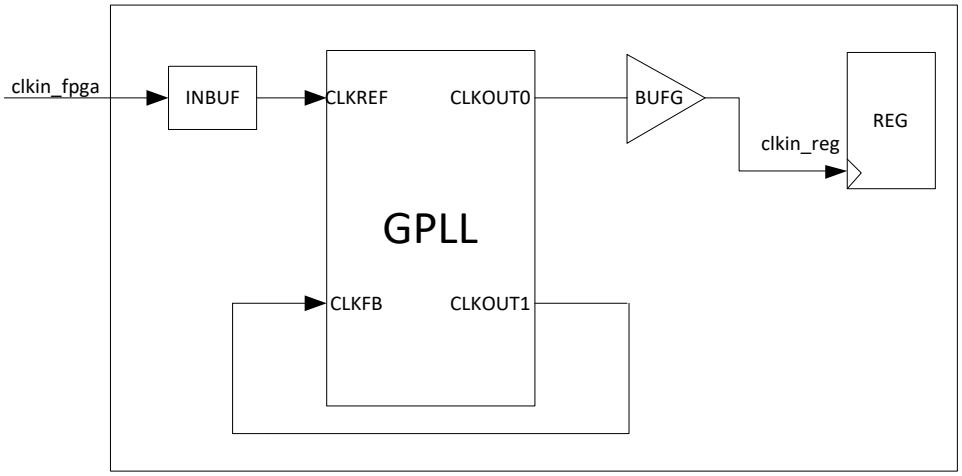

Figure 2-47 GPLL Internal Feedback Mode Diagram

2.8.8.2 Source Synchronization Mode

Source synchronization mode is achieved by using external feedback. This mode mainly targets situations where the GPLL output clock drives internal registers and maintains a certain phase relationship between the input clock and the data, as shown in the figure below. When GPLL is locked, the phases at points b/e are aligned. In the source synchronization mode, the path of the GPLL output clock clkout0 sent to the register must be symmetrically balanced with the path of the feedback clock clkout1, and the same regional buffer must be used, ensuring that the clock phases at points c and e are aligned, and hence b and c are aligned. Additionally, the GPLL phase adjustment function can compensate for the skew (offset) between the data pin to the data input of the register

and the clock pin to the GPLL input reference clock, i.e., the offset from point d to f and point a to b. This allows phase edge or centre alignment between data and clock within the FPGA internal REG, whether it is 0° or 90° alignment depends on user requirements, and specific phase shift requirements can be achieved through the phase shift function of the output clock divider.

For example, if the rising edge of the input pin clock is aligned with the centre of the data entering FPGA, the phase shift function of the GPLL output can be used to adjust the phase of clkout0. This can align the rising edge of the clock with the centre of the data through the internal registers of FPGA. At this point, if there is no skew between the reference input of the input clock clkin_fpga entering GPLL and the data entering the register, such as through a dedicated clock path where the skew is minimal, GPLL can automatically align the rising edge of the clock with the centre of the data without any phase shift adjustment.

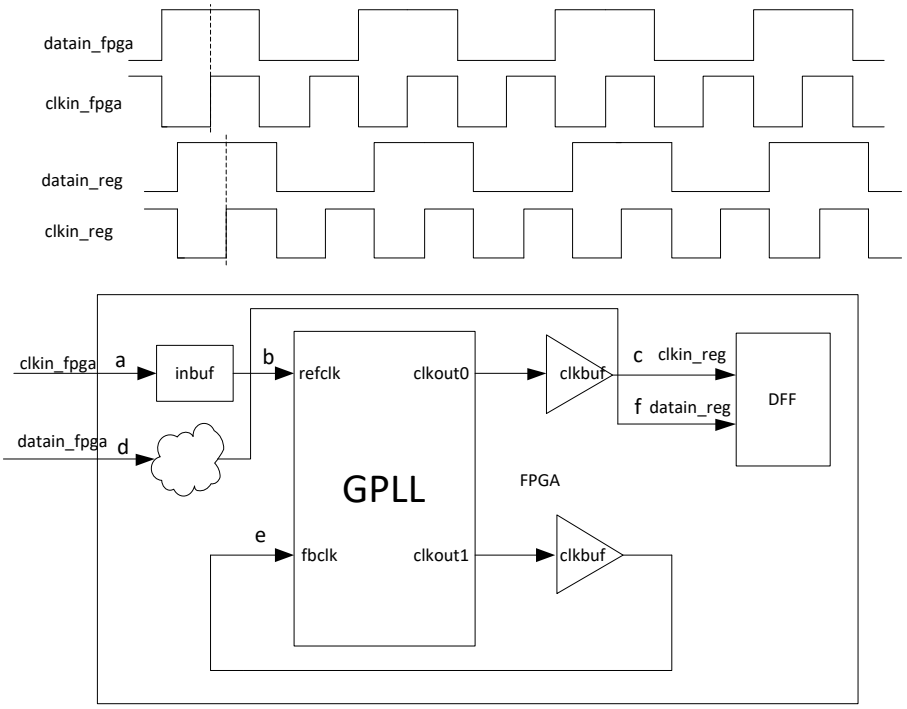

Figure 2-48 GPLL Source Synchronization Mode Diagram

2.8.8.3 Zero Delay Mode

The zero delay mode is implemented by using the external pin feedback, mainly for situations where there is only one input reference clock and FPGA drives multiple external devices. It can ensure that the input clock of the external devices aligns with the FPGA input pin clock, as shown in the figure below.

In zero delay mode, the input clock and the feedback clock need to use the same IO standard to ensure phase alignment at points a and d, as well as points b and e. Meanwhile, if the feedback clock trace on the board and the clock trace driving the external devices are matched in length, the clock phases at points d and c will be aligned, thereby aligning the clocks at points a and c, achieving the zero delay buffering function.

In actual scenarios, since the load parasitic capacitance of external devices is different from the parasitic capacitance of the FPGA input pin, the rising or falling edge timing at points c and d may be inconsistent, resulting in slight variations in delay. Therefore, customers must take this skew difference between the a/c clocks during timing closure into consideration, thus leaving a margin.

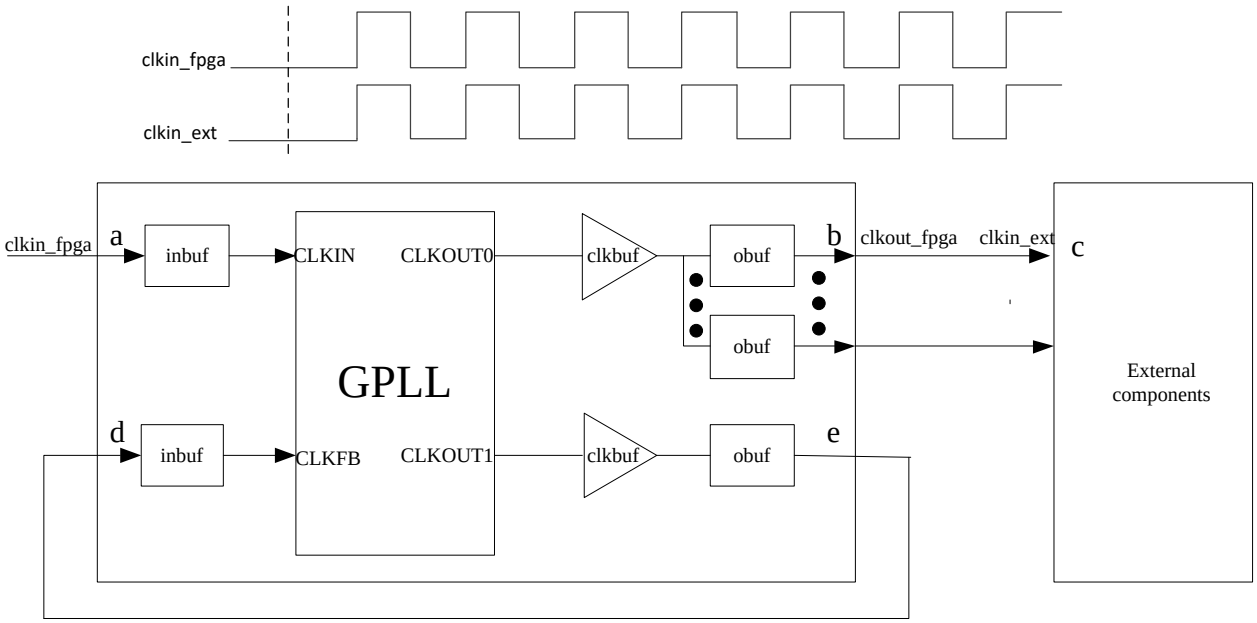

Figure 2-49 GPLL Zero Delay Mode Diagram

2.9 Usage Instructions for PPLL

2.9.1 PPLL Overview

PPLL is a core subsystem providing clock resources for FPGA. PGL2G100H contains six PPLL modules. The main functions provided by PPLL for FPGA include: clock frequency synthesis, clock deskew, phase adjustment, output clock gating, and APB dynamic reconfiguration.

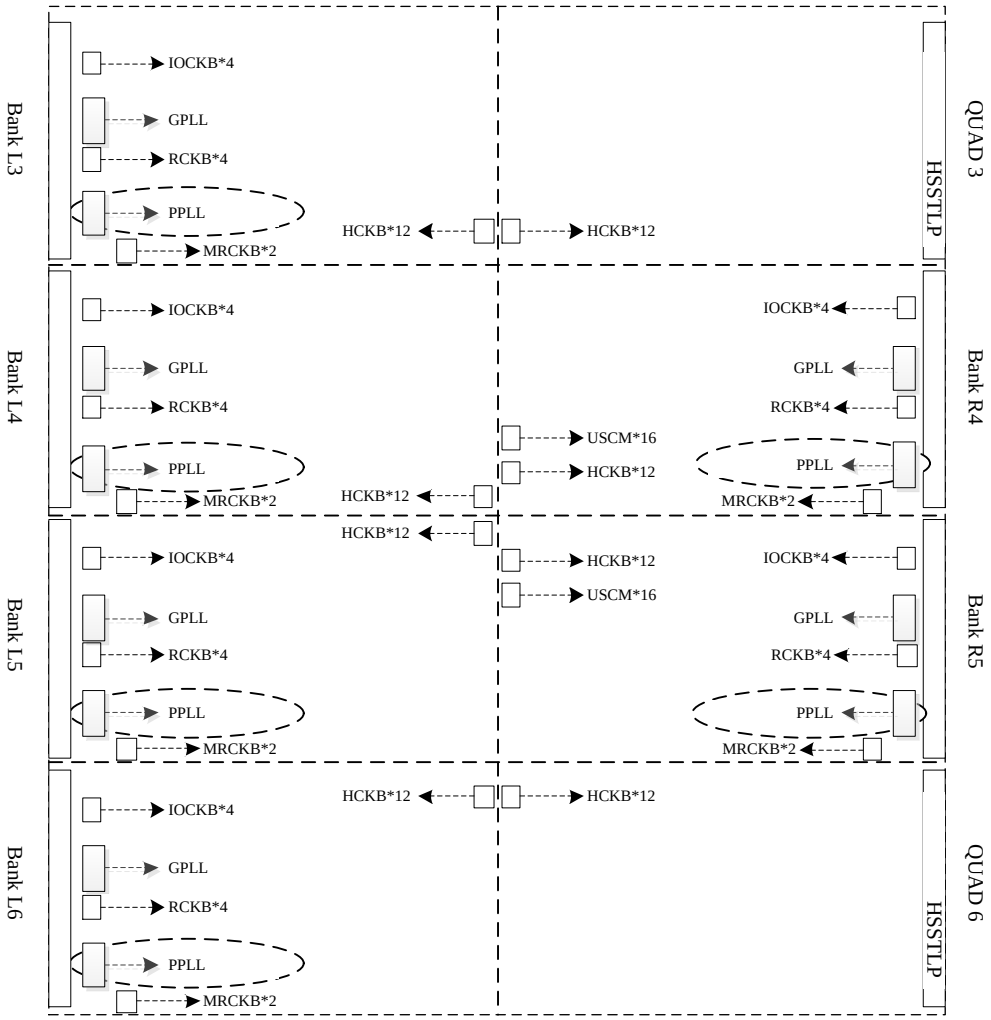

Figure 2-50 PLL Resource Distribution Diagram

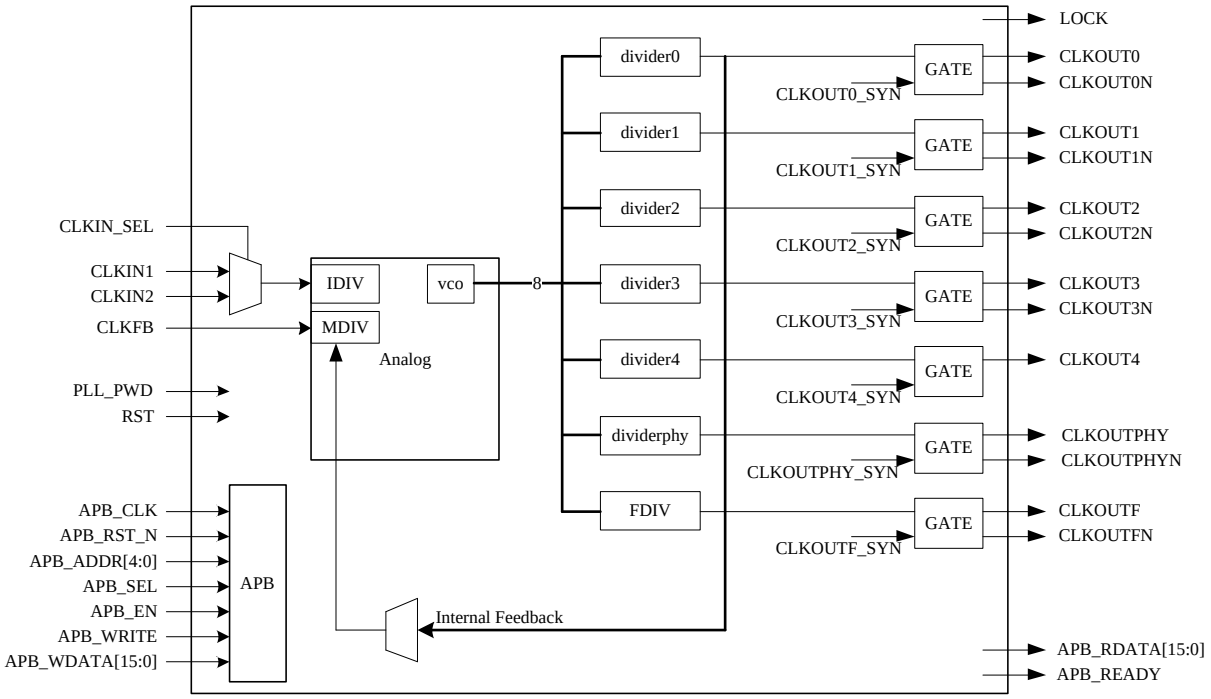

Figure 2-51 PPLL System Block Diagram

In the application, GTP_PPLL instance can be configured, and unused clock output ports can be shut down to reduce power consumption. The CLKOUTPHY clock output in the GTP_PPLL is dedicated to the DDR PHY clock and should not be used for user logic. The following describes the applications of GTP_PPLL.

2.9.2 Top Layer Block Diagram of GTP_PPLL

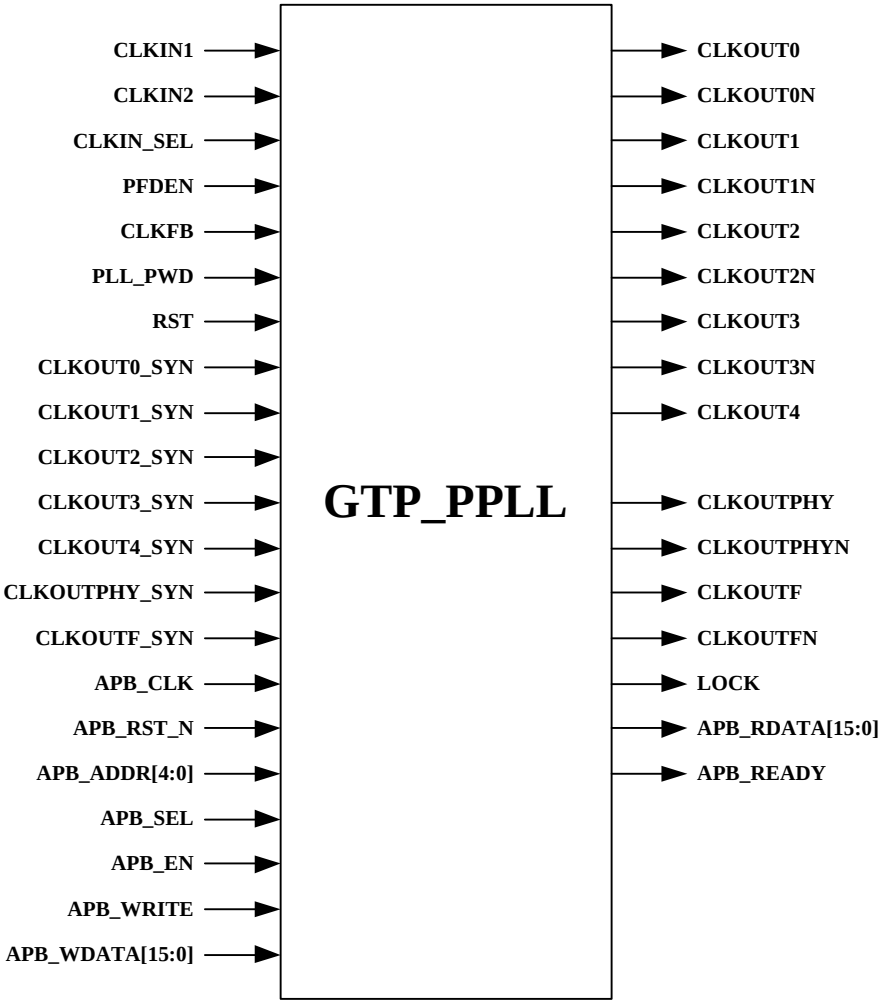

Figure 2-52 GTP_PPLL Block Diagram

2.9.3 GTP_PPLL Port List

Table 2-29 GTP_PPLL Port List

Port	I/O	Function Description
CLKOUT0	O	PLL Channel 0 Output Clock;
CLKOUT0N	O	PLL Channel 0 Inverted Output Clock;
CLKOUT1	O	PLL Channel 1 Output Clock;
CLKOUT1N	O	PLL Channel 1 Inverted Output Clock;
CLKOUT2	O	PLL Channel 2 Output Clock;
CLKOUT2N	O	PLL Channel 2 Inverted Output Clock;
CLKOUT3	O	PLL Channel 3 Output Clock;
CLKOUT3N	O	PLL Channel 3 Inverted Output Clock;
CLKOUT4	O	PLL output clock 4;
CLKOUTPHY	O	PLL provides a output clock for DDR PHY;

Port	I/O	Function Description
CLKOUTPHYN	O	PLL provides an inverting output clock for DDR PHY;
CLKOUTF	O	PLL Feedback Output Clock;
CLKOUTFN	O	PLL Feedback Inverted Output Clock;
LOCK	O	PLL frequency lock indicator signal, asynchronous signal; When the signal is pulled high, it indicates that the PLL feedback clock signal is locked to the input clock signal;
APB_RDATA[15:0]	O	PLL APB interface data bus data output
APB_READY	O	PLL APB interface data bus handshake signal; indicates the end of a normal bus cycle;
CLKIN1	I	PLL reference input clock 1;
CLKIN2	I	PLL reference input clock 2;
CLKFB	I	PLL feedback clock;
CLKIN_SEL	I	Input clock selection signal;
PLL_PWD	I	PLL Power Down, active high;
RST	I	PLL reset signal, active high;
CLKOUT0_SYN	I	CLKOUT0/N output clock enable control; active high; high level disable, low level enable;
CLKOUT1_SYN	I	CLKOUT1/N output clock enable control; active high; high level disable, low level enable;
CLKOUT2_SYN	I	CLKOUT2/N output clock enable control; active high; high level disable, low level enable;
CLKOUT3_SYN	I	CLKOUT3/N output clock enable control; active high; high level disable, low level enable;
CLKOUT4_SYN	I	CLKOUT4 output clock enable control; active high; high level disable, low level enable;
CLKOUTPHY_SYN	I	CLKOUTPHY output clock enable control; active high; high level turns off; low level enable;
CLKOUTF_SYN	I	CLKOUTF/N output clock enable control; active high; high level disable, low level enable;
APB_CLK	I	PLL APB interface data bus clock;
APB_RST_N	I	PLL APB interface data bus asynchronous reset signal, active low;
APB_ADDR	I	PLL APB interface data bus address;
APB_SEL	I	PLL APB interface data bus selection signal to select the slave device;
APB_EN	I	PLL APB interface data bus enable signal;
APB_WRITE	I	PLL APB interface data bus write enable signal; 1'b0: read operation, 1'b1: write operation;
APB_WDATA[15:0]	I	PLL APB interface data bus data input;

2.9.4 GTP_PLL Parameter List

Table 2-30 GTP_PLL Parameter List

Parameter Name	Parameter Type	Valid Values	Function Description
CLKIN_FREQ	real	19~800	Input clock frequency configuration, MHz;
LOCK_MODE	binary	1'b0, 1'b1	PLL frequency detection mode configuration; 1'b0: Real-time monitoring of PLL working state; 1'b1: The PLL lock remains after locking, unless reset or power-down;
STATIC_RATIOI	interger	1-40	Input divider ratio static configuration;
STATIC_RATIOM	interger	1-128	Feedback M divider ratio dynamic configuration;
STATIC_RATIO0	interger	1-128	Output divider0 ratio static configuration;
STATIC_RATIO1	interger	1-128	Output divider1 ratio static configuration;
STATIC_RATIO2	interger	1-128	Output divider2 ratio static configuration;
STATIC_RATIO3	interger	1-128	Output divider3 ratio static configuration;
STATIC_RATIO4	interger	1-128	Output divider4 ratio static configuration;
STATIC_RATIOPHY	interger	1-128	Output divider PHY ratio static configuration;
STATIC_RATIOF	interger	1-128	Feedback F divider ratio static configuration;
STATIC_DUTY0	interger	2~255	Output divider0 duty static configuration;
STATIC_DUTY1	interger	2~255	Output divider1 duty static configuration;
STATIC_DUTY2	interger	2~255	Output divider2 duty static configuration;
STATIC_DUTY3	interger	2~255	Output divider3 duty static configuration;
STATIC_DUTY4	interger	2~255	Output divider4 duty static configuration;
STATIC_DUTYPHY	interger	2~255	Output divider PHY duty static configuration;
STATIC_DUTYF	interger	2~255	Feedback F divider duty static configuration;
STATIC_PHASE0	interger	0-7	Output divider0 fine phase static configuration;
STATIC_PHASE1	interger	0-7	Output divider1 fine phase static configuration;
STATIC_PHASE2	interger	0-7	Output divider2 fine phase static configuration;
STATIC_PHASE3	interger	0-7	Output divider3 fine phase static configuration;
STATIC_PHASE4	interger	0-7	Output divider4 fine phase static configuration;
STATIC_PHASEPHY	interger	0-7	Output divider PHY fine phase static configuration;

Parameter Name	Parameter Type	Valid Values	Function Description
STATIC_PHASEF	interger	0-7	Feedback F divider fine phase static configuration;
STATIC_CPHASE0	interger	0-127	Output divider0 coarse phase static configuration;
STATIC_CPHASE1	interger	0-127	Output divider1 coarse phase static configuration;
STATIC_CPHASE2	interger	0-127	Output divider2 coarse phase static configuration;
STATIC_CPHASE3	interger	0-127	Output divider3 coarse phase static configuration;
STATIC_CPHASE4	interger	0-127	Output divider4 coarse phase static configuration;
STATIC_CPHASEPHY	interger	0-127	Output divider PHY coarse phase static configuration;
STATIC_CPHASEF	interger	0-127	Feedback F divider coarse phase static configuration;
CLKOUT0_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT0_SYN signal enable;
CLKOUT1_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT1_SYN signal enable;
CLKOUT2_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT2_SYN signal enable;
CLKOUT3_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT3_SYN signal enable;
CLKOUT4_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUT4_SYN signal enable;
CLKOUTPHY_SYN_EN	string	"FALSE", "TRUE"	CLKOUTPHY_SYN signal enable configuration;
CLKOUTF_SYN_EN	string	"FALSE", "TRUE"	Configuration for CLKOUTF_SYN signal enable;
INTERNAL_FB	string	"CLKOUT0", "CLKOUT1", "CLKOUT2", "CLKOUT3", CLKOUT4, "CLKOUTF", "DISABLE"	Internal feedback path selection, choose one of the output clocks as the internal feedback clock, e.g., INTERNAL_FB = "CLKOUT0", then the output clock CLKOUT0 is used as the internal feedback clock;
EXTERNAL_FB	string	"CLKOUT0", "CLKOUT1" "CLKOUT2", "CLKOUT3", CLKOUT4, "CLKOUTF", "DISABLE"	External feedback path selection, choose one of the output clocks as the external feedback clock, e.g., EXTERNAL_FB = "CLKOUT0", then the output clock CLKOUT0 is used as the external feedback clock;
BANDWIDTH	string	"LOW", "HIGH" "OPTIMIZED"	Bandwidth selection configuration: BANDWIDTH = "LOW" configured as "LOW", Configure BANDWIDTH as "HIGH" when set to "HIGH" and as "OPTIMIZED" when set to "OPTIMIZED";

Note:

1. The parameters INTERNAL_FB and EXTERNAL_FB cannot be configured as "DISABLE" simultaneously.

2. BANDWIDTH configuration is limited by PFD frequency

2.9.5 GTP_PPLL APB Interface Configuration

Allows user logic to change the GTP_PPLL's operating parameters dynamically via the APB port. The timing for APB interface register read and write is as shown in the following figures:

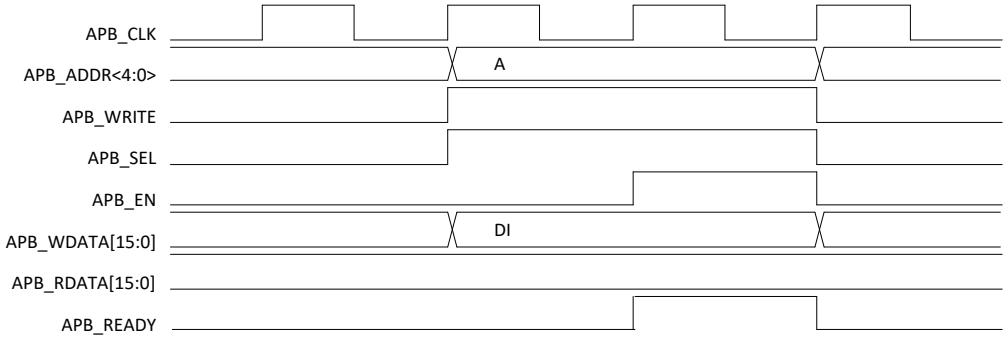

Figure 2-53 GTP_PPLL_APB Write Timing

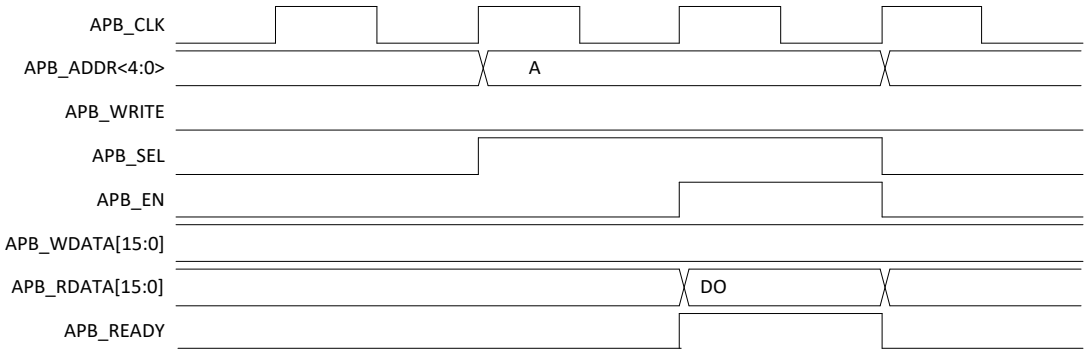

Figure 2-54 GTP_PPLL_APB Read Timing

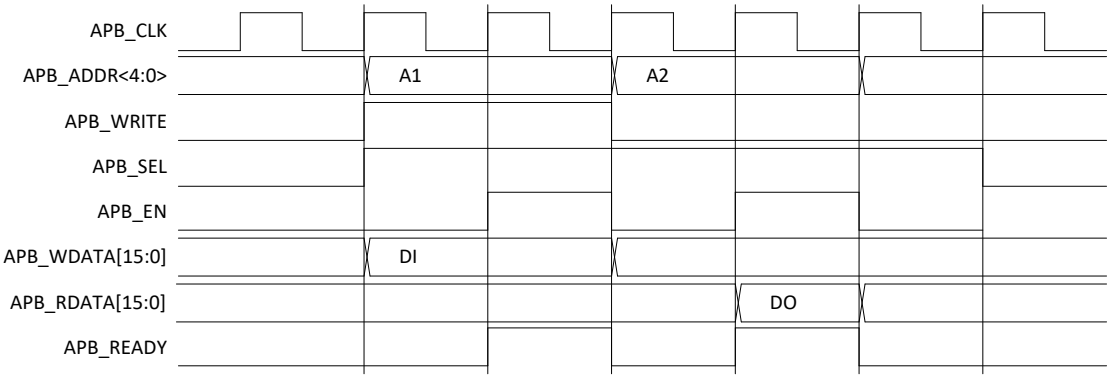

Figure 2-55 Timing of GTP_PPLL_APB Write before Read

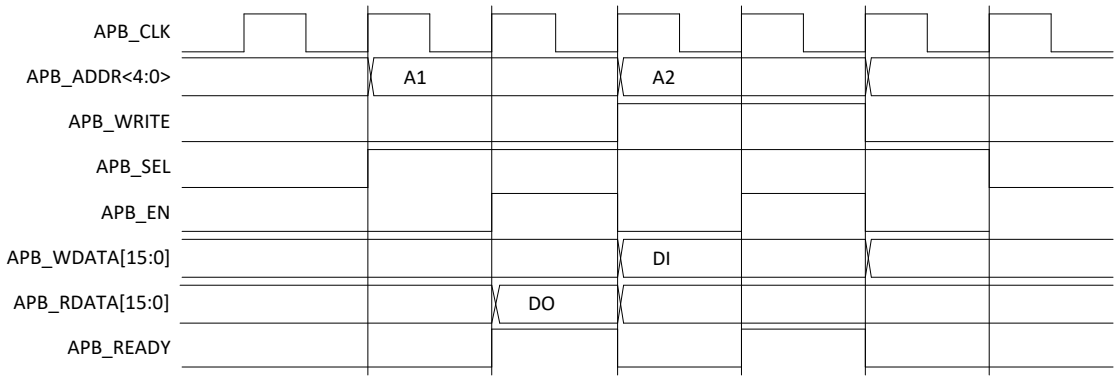

Figure 2-56 Timing of GTP_PPLL_APB Interface Read before Write

Table 2-31 GTP_PPLL_APB Port List

Series Number	Port	I/O	Description
1	APB_CLK	I	Clock, sampled on the rising edge;
2	APB_RST_N	I	Asynchronous reset, active low; resets only the data bus (does not reset register);
3	APB_ADDR[4:0]	I	Address Bus;
4	APB_SEL	I	Selection, indicating that the slave device has been selected;
5	APB_EN	I	Enable, bus enable signal;
6	APB_WRITE	I	Direction, 0: read, 1: write;
7	APB_WDATA[15:0]	I	Data bus input;
8	APB_RDATA[15:0]	O	Data bus output;
9	APB_READY	O	Flag Signals;

System application requirements for writing internal registers via the APB interface:

- After rewriting the internal registers via the APB interface, the PLL needs to be reset to ensure it operates properly
- For the performance specification for the minimum pulse width of RST, please refer to the "***DS04001_Logos2 Family FPGA Device Datasheet***"

Table 2-32 GTP_PPLL_APB Interface Register List

Address	Bit	Register	Description
0	[15:8]	REG_ODIV0_RATIO<7:0>,	ODIV0 Register1: Division ratio settings;
	[7:0]	REG_ODIV0_DUTY<7:0>	ODIV0 Register1: Duty cycle settings;
1	[15:11]	RESERVED	
	[10]	REG_ODIV0_MUXSEL_EN	ODIV0 Register 2: Input clock MUX enable;
	[9:7]	REG_ODIV0_FPHASE<2:0>	ODIV0 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV0_CPHASE<6:0>	ODIV0 Register2: Phase coarse adjustment settings;
2	[15:8]	REG_ODIV1_RATIO<7:0>	ODIV1 Register1: Division ratio settings;
	[7:0]	REG_ODIV1_DUTY<7:0>	ODIV1 Register1: Duty cycle settings;
3	[15:11]	RESERVED	
	[10]	REG_ODIV1_MUXSEL_EN	ODIV1 Register2: Input clock MUX enable;
	[9:7]	REG_ODIV1_FPHASE<2:0>	ODIV1 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV1_CPHASE<6:0>	ODIV1 Register2: Phase coarse adjustment settings;
4	[15:8]	REG_ODIV2_RATIO<7:0>	ODIV2 Register1: Division ratio settings;
	[7:0]	REG_ODIV2_DUTY<7:0>	ODIV2 Register1: Duty cycle settings;
5	[15:11]	RESERVED	
	[10]	REG_ODIV2_MUXSEL_EN	ODIV2 Register2: Input clock MUX enable;
	[9:7]	REG_ODIV2_FPHASE<2:0>	ODIV2 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV2_CPHASE<6:0>	ODIV2 Register2: Phase coarse adjustment settings;
6	[15:8]	REG_ODIV3_RATIO<7:0>	ODIV3 Register1: Division ratio settings;
	[7:0]	REG_ODIV3_DUTY<7:0>	ODIV3 Register1: Duty cycle settings;
7	[15:11]	RESERVED	
	[10]	REG_ODIV3_MUXSEL_EN	ODIV3 Register2: Input clock MUX enable;
	[9:7]	REG_ODIV3_FPHASE<2:0>	ODIV3 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV3_CPHASE<6:0>	ODIV3 Register2: Phase coarse adjustment settings;
8	[15:8]	REG_ODIV4_RATIO<7:0>	ODIV4 Register1: Division ratio settings;
	[7:0]	REG_ODIV4_DUTY<7:0>	ODIV4 Register1: Duty cycle settings;
9	[15:11]	RESERVED	
	[10]	REG_ODIV4_MUXSEL_EN	ODIV4 Register2: Input clock MUX enable;
	[9:7]	REG_ODIV4_FPHASE<2:0>	ODIV4 Register2: Phase fine adjustment settings;
	[6:0]	REG_ODIV4_CPHASE<6:0>	ODIV4 Register2: Phase coarse adjustment settings;
A	[15:8]	REG_ODIVPHY_RATIO<7:0>	ODIVPHY Register 1: Division ratio setting;
	[7:0]	REG_ODIVPHY_DUTY<7:0>	ODIVPHY Register 1: Duty cycle setting;

Address	Bit	Register	Description
B	[15:11]	RESERVED	
	[10]	REG_ODIVPHY_MUXSEL_EN	ODIVPHY Register 2: Input clock MUX enable;
	[9:7]	REG_ODIVPHY_FPHASE<2:0>	ODIVPHY Register 2: Phase fine adjustment setting;
	[6:0]	REG_ODIVPHY_CPHASE<6:0>	ODIVPHY Register 2: Phase coarse adjustment setting;
C	[15:8]	REG_FDIV_RATIO<7:0>	FDIV Register1: Division ratio settings;
	[7:0]	REG_FDIV_DUTY<7:0>	FDIV Register1: Duty cycle settings;
D	[15:11]	RESERVED	
	[10]	REG_FDIV_MUXSEL_EN	FDIV Register 2: Input clock MUX enable;
	[9:7]	REG_FDIV_FPHASE<2:0>	FDIV Register2: Phase fine adjustment settings;
	[6:0]	REG_FDIV_CPHASE<6:0>	FDIV Register2: Phase coarse adjustment settings;
E	[15:7]	RESERVED	
	[6:0]	REG_IDIV_RATIO<7:0>	IDIV Register: Division ratio settings;
F	[15:7]	RESERVED	
	[6:0]	REG_MDIV_RATIO<7:0>	MDIV Register: Division ratio settings;
10	[15:14]	RESERVED	BANDWIDTH Register
	[13:12]	REG_VCTRL_INIT<1:0>	
	[11:10]	REG_CP_SELFBIAS_SEL<1:0>	
	[9:8]	REG_ICP_BASE_SEL<1:0>	
	[7:4]	REG_CP_CUR_SEL<3:0>	
	[3:1]	REG_LPF_R<2:0>	
	[0]	REG_LPF_C	
11	[15:6]	RESERVED	LOCK Register1
	[5]	REG_LOCK_FILTER_PD	
	[4:0]	REG_FREQ_LOCKDET_SET<4:0>	

2.9.6 GTP_PPLL Function Description

2.9.6.1 Clock Input

When CLKIN_SEL is 0, select CLKIN1; when CLKIN_SEL is 1, select CLKIN2. The reference clock dynamically switches between CLKIN1 and CLKIN2, and PLL needs to be reset after switching.

The following points should be noted regarding the PPLL input clock:

- If the input clock is lost or unstable, the PPLL needs to be reset after the input clock recovers stability
- During power-up and when there is no input clock after power-up, the PPLL will output a low-frequency clock signal; at this time, the LOCK signal is at a low level. If you wish to set the output clock to 0, it is needed to use the power-down mode or clock output gating, for details, please refer to Section 2.9.6.3 and 2.9.6.10

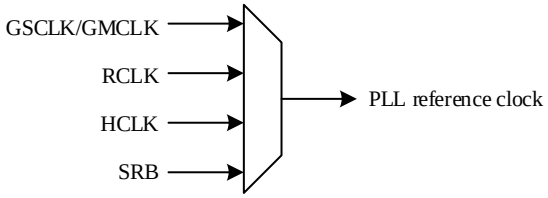

Figure 2-57 GTP_PPLL Reference Clock Source

2.9.6.2 PPLL Reset

After the RST reset signal is released, the PLL starts to enter the lock state, and the PLL frequency lock is completed after T_{LOCK} (PLL lock time). Before the LOCK signal transitions from low to high, CLKOUT will gradually begin to toggle from low level. During this time, CLKOUT is unstable. CLKOUT stabilizes only after the LOCK signal transitions to high. The timing of the RST reset signal is shown in the figure below; active high.

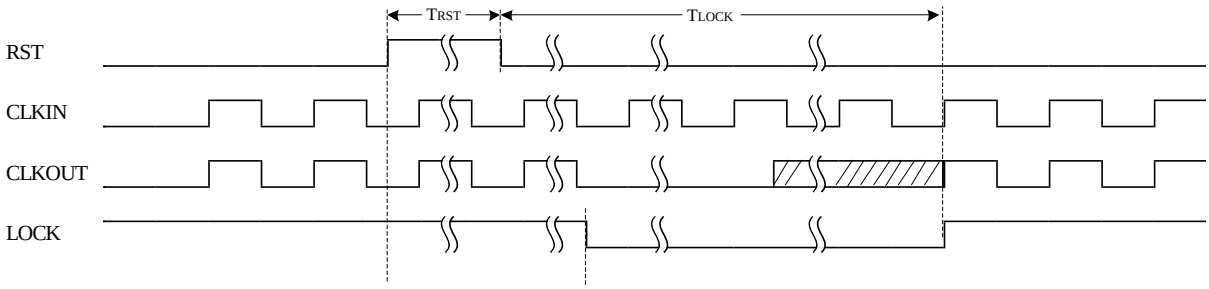

Figure 2-58 GTP_PPLL Reset Timing

For T_{RST} and T_{LOCK} performance specification, please refer to "DS04001_Logos2 Family FPGAs Device Datasheet".

2.9.6.3 PPLL Power-down

When the PLL is not in use, the PLL power can be turned off by setting the PLL_PWD signal to a high level, thus saving power consumption. If the PLL is to be used again, set the PLL_PWD signal to a low level. After T_{LOCK} time, the PLL will relock. Before the LOCK signal transitions from low to high, CLKOUT will gradually begin to toggle from low level. During this time, CLKOUT is unstable. CLKOUT stabilizes only after the LOCK signal transitions to high.

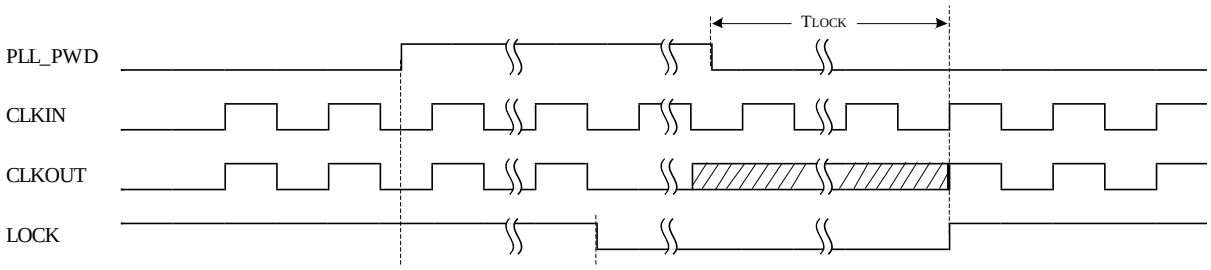

Figure 2-59 GTP_PPLL Power Down Timing

2.9.6.4 Feedback Clock Selection

The PPLL feedback clock input source can be divided into two types: PPLL internal feedback and PPLL external feedback, with feedback sources supporting CLKOUT[0]-CLKOUT[4], CLKOUTF.

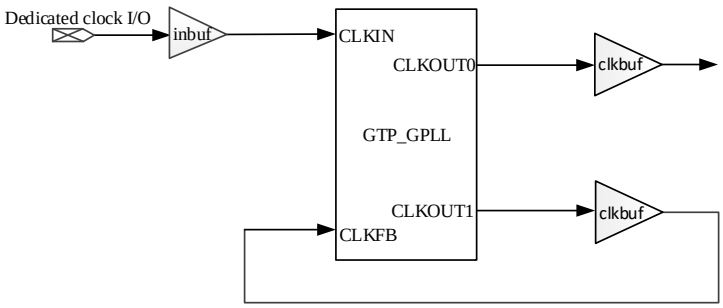

Figure 2-60 GTP_PPLL External Feedback Diagram

As shown in the figure, when external feedback is selected, the feedback clock reaches the feedback clock input through the global clock or horizontal clock buffer along a dedicated clock path. In internal feedback mode, the feedback clock output directly reaches the feedback clock input within the PLL, receiving less interference compared to external feedback.

Table 2-33 Feedback Clock Selection List

INTERNAL_FB	EXTERNAL_FB	Feedback Mode
"CLKOUT0"	"DISABLE"	Internal feedback mode, select output divider0;
"CLKOUT1"	"DISABLE"	Internal feedback mode, select output divider1;
"CLKOUT2"	"DISABLE"	Internal feedback mode, select output divider2;
"CLKOUT3"	"DISABLE"	Internal feedback mode, select output divider3;
"CLKOUT4"	"DISABLE"	Internal feedback mode, select output divider4;
"CLKOUTF"	"DISABLE"	Internal feedback mode, select feedback F divider;
"DISABLE"	"CLKOUT0"	External feedback mode, select output divider0;
"DISABLE"	"CLKOUT1"	External feedback mode, select output divider1;
"DISABLE"	"CLKOUT2"	External feedback mode, select output divider2;
"DISABLE"	"CLKOUT3"	External feedback mode, select output divider3;
"DISABLE"	"CLKOUT4"	External feedback mode, select output divider4;
"DISABLE"	"CLKOUTF"	External feedback mode, select feedback F divider;

2.9.6.5 Output Frequency Programming

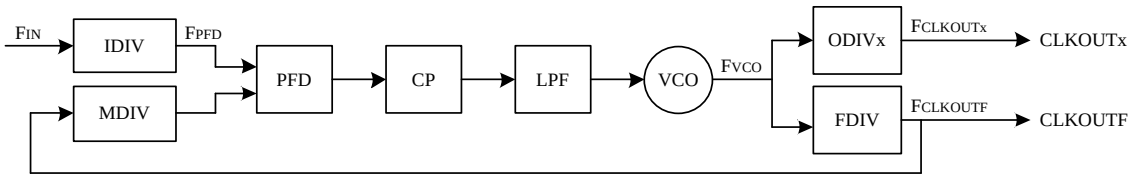

Figure 2-61 GTP_PPLL Output Frequency Programming Diagram

The reference clock (Fin) passes through a programmable input divider (IDIV) to obtain a reference clock for the phase frequency detector (PFD). The feedback clock passes through programmable feedback dividers (FDIV) and (MDIV) to obtain another reference clock for the PFD. The PFD compares the phase and frequency of these two clocks and then generates a signal to drive the charge pump (CP). The current signal generated by the CP passes through the loop filter (LPF), and the LPF produces a reference voltage for the voltage-controlled oscillator (VCO). The PFD provides phase lead or lag signals to the CP and LPF to continuously adjust the VCO operating frequency, thus regulating the frequency and phase. For example, if the VCO remains higher than the reference frequency after passing through the feedback divider, the PFD generates a downward adjustment signal, causing the CP and LPF to decrease the voltage and control the VCO to lower the output frequency. If the VCO remains lower than the reference frequency after passing through the feedback divider, the PFD generates an upward adjustment signal, causing the CP and LPF to increase the voltage and control the VCO to raise the output frequency. The VCO generates 8-phase output clocks, which can achieve phase coarse and fine adjustments. Each output phase-shifted

clock can be used as the input for FDIV. There are 7 output dividers in total, 6 ODIVs and 1 FDIV. Each divider is independent of each other. The final output clock frequency is obtained by VCO output clock through these dividers.

Table 2-34 Descriptions for PPLL Output Frequency Programming Parameters

Function Name	**Description**
FIN	Input Clock Frequency
FPFD	Input reference clock frequency of PFD
FVCO	Output clock frequency of VCO
FCLKOUTx	CLKOUT0~4/CLKOUTPHY Output Clock Frequency
FCLKOUTF	Output clock frequency of CLKOUTF
IDIV	The division ratio of the input divider
MDIV	The division ratio of the feedback divider M
ODIVx	The division ratio of output divider, x represents 0~4/PHY, STATIC_RATIO0-4 corresponds to CLKOUT0~4, STATIC_RATIOPHY corresponds to CLKOUTPHY
FDIV	The division ratio of the feedback divider F

Note: IDIV corresponds to the parameter STATIC_RATIOI, MDIV corresponds to the parameter STATIC_RATIOM, ODIV0-4 corresponds to the parameter STATIC_RATIO0-4, ODIVphy corresponds to the parameter STATIC_RATIOPHY, and FDIV corresponds to the parameter STATIC_RATIOF

If the division ratio of the feedback divider selected for internal or external feedback is FBDIV, the clock frequency calculation formulas are as follows:

$$F_{PFD} = \frac{F_{IN}}{IDIV}$$

$$F_{VCO} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV}$$

$$F_{CLKOUTx} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times ODIVx}$$

$$F_{CLKFBOUT} = \frac{F_{IN} \times MDIV \times FBDIV}{IDIV \times FDIV}$$

FBDIV is the division ratio of the divider selected for the feedback loop. By configuring INTERNAL_FB or EXTERNAL_FB, users can select one of the dividers in FDIV or ODIVx.

2.9.6.6 Loop bandwidth

The PPLL loop bandwidth can be configured to low bandwidth (LOW), medium bandwidth (OPTIMIZED) and high bandwidth (HIGH). The parameters for low and medium bandwidth configurations are same.

Considering that in actual applications the input clock is not ideal, different bandwidth configurations affect the PLL differently:

- If a smaller jitter is desired for PLL output clock, it can be configured to low bandwidth or medium bandwidth, resulting in a longer locking time
- If a shorter locking time is desired for PLL, it can be configured to high bandwidth, at the cost of increased output clock jitter

2.9.6.7 Phase Adjustment

Phase adjustment includes two methods: phase coarse adjustment and phase fine adjustment. Both phase coarse adjustment and phase fine adjustment can be accomplished through static configuration or via the APB interface.

- Phase adjustment method:
  - Phase coarse adjustment

    Phase coarse adjustment for the output clocks CLKOUT0/1/2/3/4/F and CLKOUTPHY can be achieved through configuration parameters STATIC_CPHASE0/1/2/3/4/F and STATIC_CPHASEPHY.

    With respect to the input VCO clock, the step for phase coarse adjustment of the output clock is Tvco, with an adjustment range of [0-Ndiv-1]*Tvco and a step for adjustment degree of 360 °/Ndiv.

    Ndiv is the output division ratio ODIVx and the feedback division ratio FDIV.
  - Phase fine adjustment

    By configuring the parameters STATIC_PHASE0/1/2/3/4/F and STATIC_PHASEPHY, the phase fine adjustment of the output clocks CLKOUT0/1/2/3/4/F and CLKOUTPHY can be achieved.

    With respect to the input VCO clock, the minimum step for phase fine adjustment of the output clock is Tvco/8 (the adjustment range is (0-7/8)Tvco) with a step for adjustment degree of 45 °/Ndiv and an adjustment range of (0 °-45 °*7)/Ndiv.

    Note: Ndiv∈{STATIC_RATIO0-4, STATIC_RATIOPHY, STATIC_RATIOF}, is the division factor of the output clocks CLKOUT0/1/2/3/4/PHY/F.

- Phase adjustment mode
  - Static configuration

    The static configuration for phase fine adjustment of the output clocks CLKOUT0/1/2/3/4/ PHY/F is controlled by STATIC_PHASE0/1/2/3/4/PHY/F respectively;

    The static configuration for phase coarse adjustment of the output clocks CLKOUT0/1/2/3/4/

    PHY/F is controlled by STATIC_CPHASE0/1/2/3/4/PHY/F respectively;

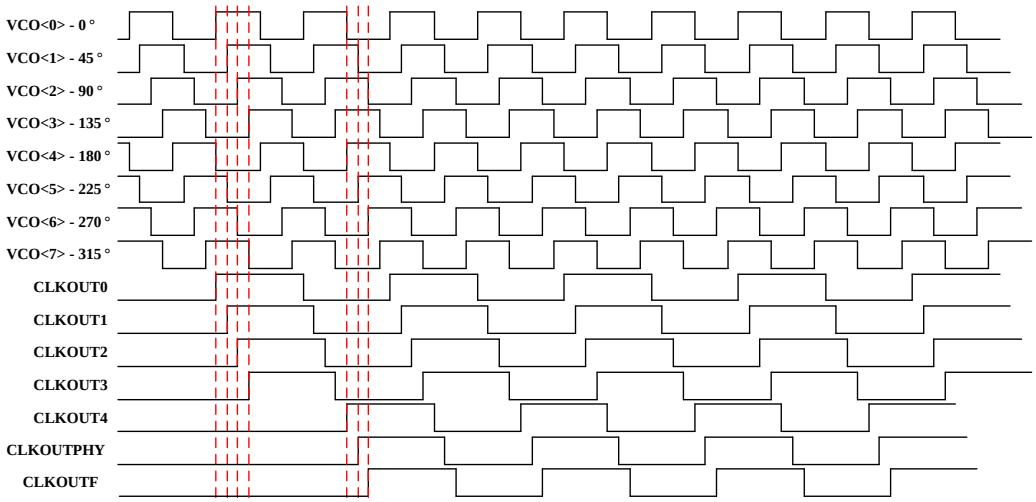

Figure 2-62 GTP_PPLL Static Phase Adjustment Configuration

As shown in the table below, CLKOUT0 is generated by VCO<0> divide-by-two, with a phase fine adjustment of 0 and a phase coarse adjustment of 0. With CLKOUT0 as the reference, the phase relationship of each output clock is as follows:

According to the formula, since ODIV0 = 2, the minimum step for phase fine adjustment is 45 °/2 = 22.5 °, and the minimum step for phase coarse adjustment is 180 °.

Table 2-35 The Phase Relationship of the Output Clock

Output clock	**Fine Adjustment Configuration**	**Coarse Adjustment Configuration**	**Phase Relationship**
CLKOUT0	0	0	0
CLKOUT1	1*Tvco/8	0	22.5 °
CLKOUT2	2*Tvco/8	0	45 °
CLKOUT3	3*Tvco/8	0	67.5 °
CLKOUT4	4*Tvco/8	Tvco	270 °
CLKOUTPHY	5*Tvco/8	Tvco	292.5 °
CLKOUTF	6*Tvco/8	Tvco	315 °

2.9.6.8 Programmable Duty Cycle

The PLL supports a programmable duty cycle with a minimum step of 50%/odiv, where odiv is the division factor. STATIC_DUTY0/1/2/3/4/PHY/F determines the duty cycle after division. The expression is as follows: duty is the configured value of the duty cycle, duty cycle = (50%/odiv) * duty.

Attention:

1. The duty value is restricted by the odiv value (output division): when odiv > 1, 2 <= duty <= 2*odiv-1; when odiv = 1, duty is invalid and does not function, and the default output is 50%.

2. Fractional division does not support duty cycle programming.

2.9.6.9 Spread Spectrum Clock Input

Supports spread spectrum clock input with modulation frequency less than PPLL bandwidth.

2.9.6.10 Clock Output Gating

The GTP_PPLL input signal CLKOUT0_SYN is used to enable and disable CLKOUT0 output clock; when the CLKOUT0 clock is not required, it can be turned off to reduce the power consumption of Clock Tree and Fabric.

The CLKOUT0_SYN signal is optional and is active when the user sets CLKOUT0_SYN_EN to "TRUE."

Similarly, the input signals CLKOUT1-4/PHY/F_SYN respectively work in conjunction with the configuration bits CLKOUT1-4/PHY/F_SYN_EN, enabling and disabling the CLKOUT1-4/PHY/F clocks.

Taking the output clock CLKOUT0 as an example, when the CLKOUT0_SYN level is in transition from 0 to 1, after 3 CLKIN falling edges CLKOUT0 outputs a low level, and when the CLKOUT0_SYN level is in transition from 1 to 0, after 3 CLKIN falling edges the CLKOUT0 output is valid. The functional diagram is shown in the following figure:

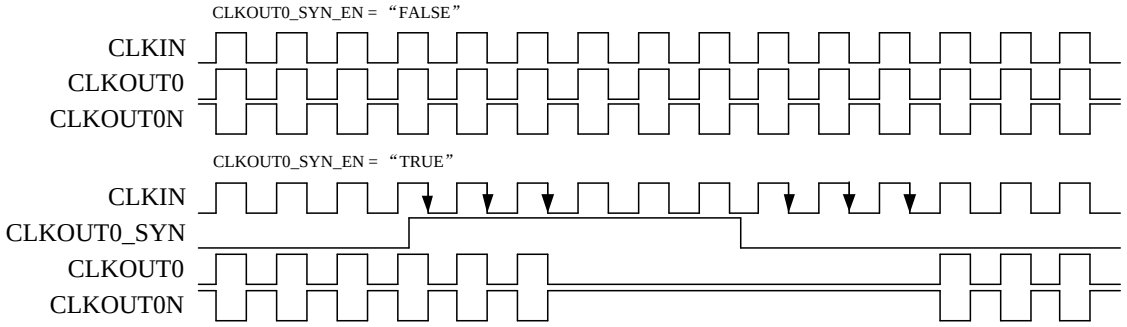

Figure 2-63 The Timing Diagram of GTP_PPLL Output Clock GATE

2.9.6.11 LOCK Indication

PPLL supports two LOCK modes, which are selected by the configuration parameter LOCK_MODE. When PLL is operating, it needs to be reset when LOCK is pulled down.

Table 2-36 PPLL LOCK Indication Modes

Parameter	**Parameter Value**	**Function Description**
LOCK_MODE	0	PLL LOCK status is monitored in real time, if it enters an abnormal state, LOCK will be pulled down.
	1	LOCK does not monitor (indicate) PLL operating state in real time; once LOCK is pulled high it will not be pulled down again until LOCK reset or Power Down.

2.9.7 GTP_PPLL Application Mode

2.9.7.1 Internal Feedback Mode

Internal feedback mode mainly targets certain application scenarios where high performance of PPLL output clock is required, such as frequency synthesis, low jitter clock output, etc.

In the internal feedback mode, the feedback clock is directly connected to the input of PPLL without passing through any other circuitry, thus eliminating noises introduced by other circuits and achieving better jitter performance.

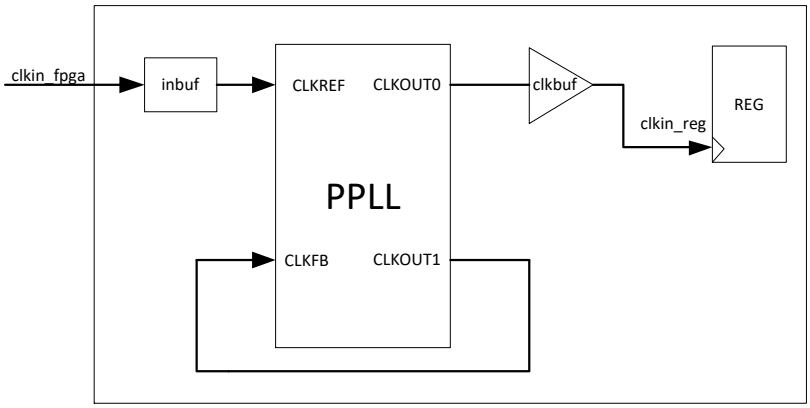

Figure 2-64 PPLL Internal Feedback Mode Diagram

2.9.7.2 Source Synchronization Mode

Source synchronization mode is achieved by using external feedback. This mode mainly targets situations where the PPLL output clock drives internal registers and maintains a certain phase relationship between the input clock and the data, as shown in the figure below. When PPLL is locked, the phases at points b/e are aligned. In the source synchronization mode, the path of the PPLL output clock clkout0 sent to the register must be symmetrically balanced with the path of the feedback clock clkout1, and the same regional buffer must be used, ensuring that the clock phases at points c and e are aligned, and hence b and c are aligned. Additionally, the PPLL phase adjustment function can compensate for the skew (offset) between the data pin to the data input of the register and the clock pin to the PPLL input reference clock, i.e., the offset from point d to f and point a to b. This allows phase edge or centre alignment between data and clock within the FPGA internal REG, whether it is 0° or 90° alignment depends on user requirements, and specific phase shift requirements can be achieved through the phase shift function of the output clock divider.

For example, if the rising edge of the input pin clock is aligned with the centre of the data entering FPGA, the phase shift function of the PPLL output can be used to adjust the phase of clkout0. This can align the rising edge of the clock with the centre of the data through the internal registers of FPGA. At this point, if there is no skew between the reference input of the input clock clkin_fpga entering PPLL and the data entering the register, such as through a dedicated clock path where the skew is minimal, PPLL can automatically align the rising edge of the clock with the centre of the data without any phase shift adjustment.

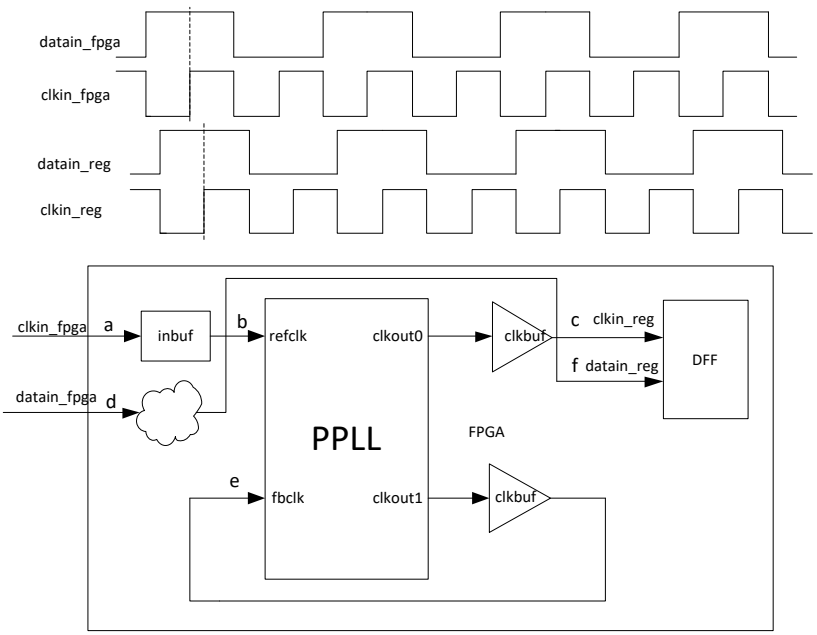

Figure 2-65 PPLL Source Synchronization Mode Diagram

2.9.7.3 Zero Delay Mode

The zero delay mode is implemented by using the external pin feedback, mainly for situations where there is only one input reference clock and FPGA drives multiple external devices. It can ensure that the input clock of the external devices aligns with the FPGA input pin clock, as shown in the figure below.

In zero delay mode, the input clock and the feedback clock need to use the same IO standard to ensure phase alignment at points a and d, as well as points b and e. Meanwhile, if the feedback clock trace on the board and the clock trace driving the external devices are matched in length, the clock phases at points d and c will be aligned, thereby aligning the clocks at points a and c, achieving the zero delay buffering function.

In actual scenarios, since the load parasitic capacitance of external devices is different from the parasitic capacitance of the FPGA input pin, the rising or falling edge timing at points c and d may be inconsistent, resulting in slight variations in delay. Therefore, customers must take this skew difference between the a/c clocks during timing closure into consideration, thus leaving a margin.

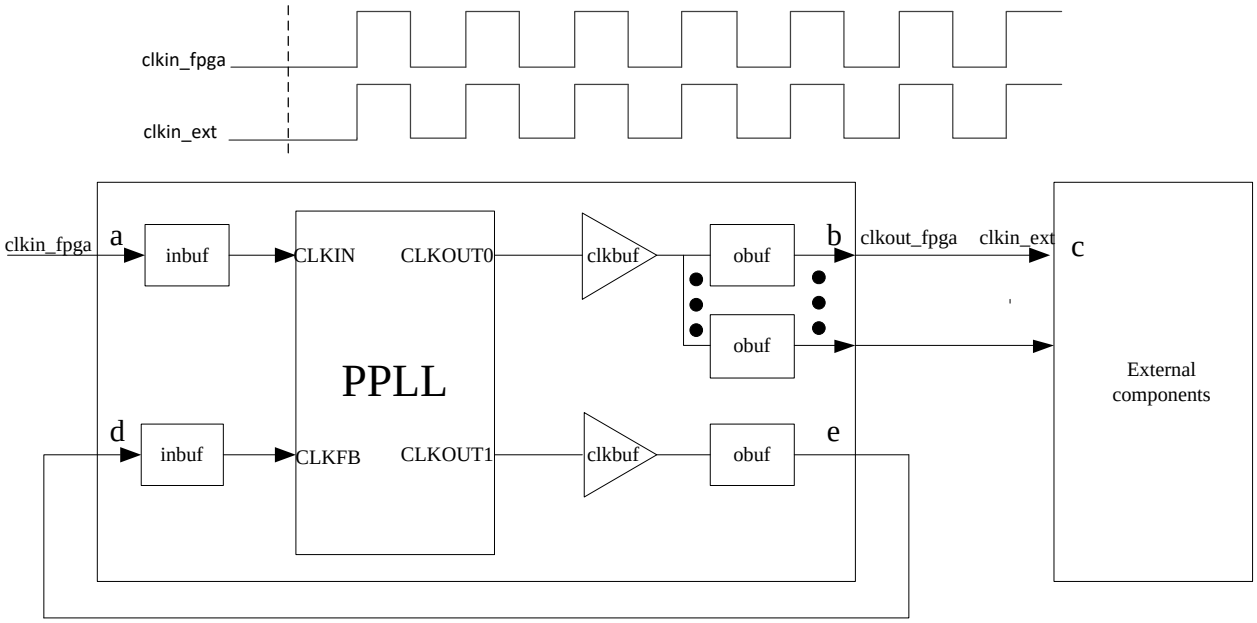

Figure 2-66 PPLL Zero Delay Mode Diagram

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