PK02004_PGL22GS_LPG176

(V1.4)

(11.01.2020)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.4	11.01.2020	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

PGL22GS_LPG176 uses wire bond to encapsulate SDRAM, with an EPAD Quad Flat Package (QFP) form factor. Its package size is 20x20mm, with 176 pins, a pin pitch of 0.4mm, and a maximum package thickness of 1.60mm.

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Values

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
D	21.80	22.0	22.20	A	n/a	n/a	1.60
D1	19.90	20.0	20.10	A1	0.05	n/a	0.15
D2	n/a	6.5	n/a	A2	1.35	1.40	1.45
E	21.80	22.0	22.20	A3	0.59	0.64	0.69
E1	19.90	20.0	20.10	b	0.14	n/a	0.23
E2	n/a	6.5	n/a	b1	0.13	0.16	0.19
e	0.35	0.40	0.45	c	0.13	n/a	0.18
L	0.45	0.60	0.75	c1	0.12	0.13	0.14

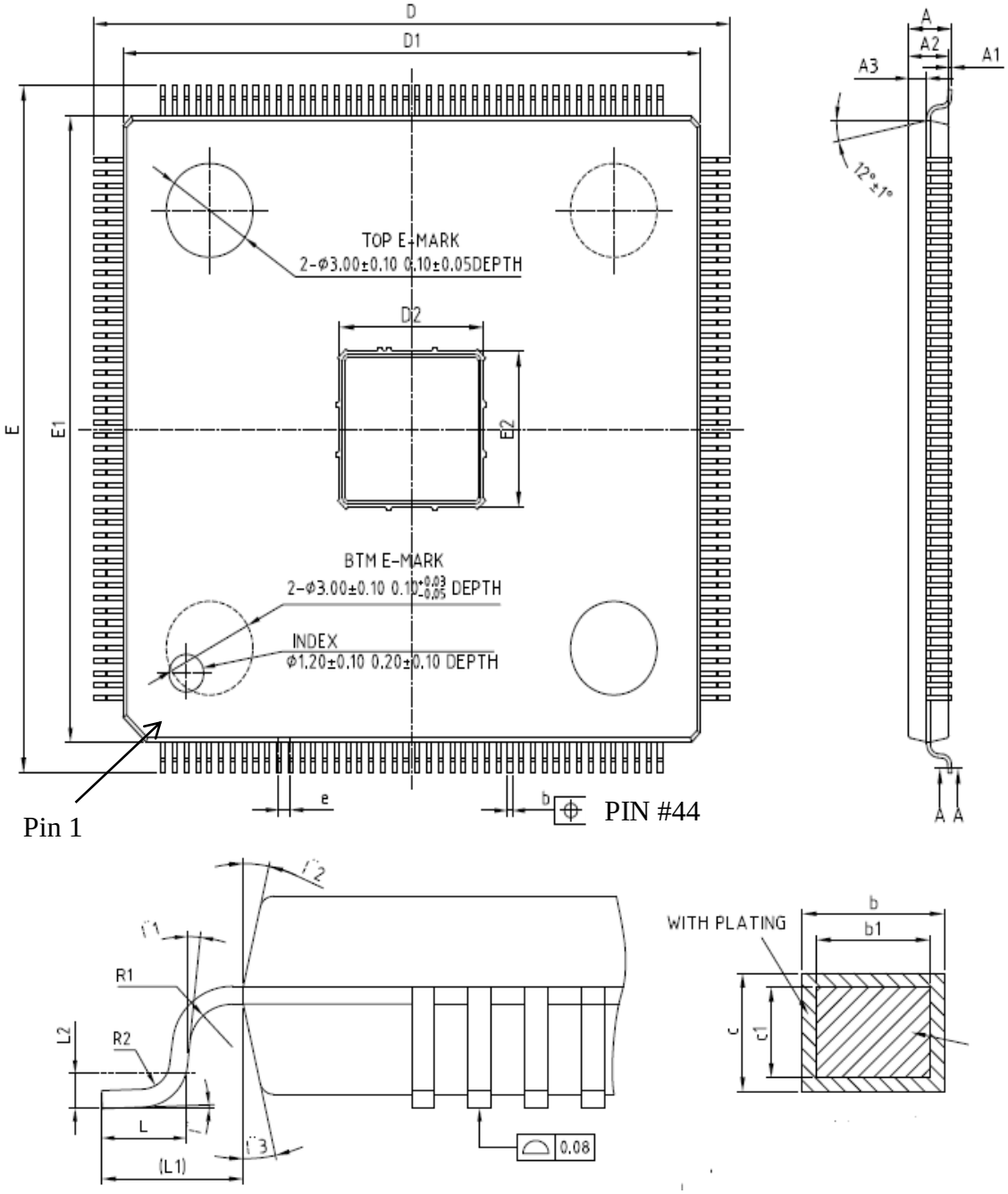

Figure 2-1 Package Outline Dimension (POD)

Note: PIN #1 indicates the position of the first pin

2.2 Pin Description

Table 2-2 Product Pin Definitions

PIN name	PIN type	PIN description
General PIN		
DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]	input/output	All general IOs are marked as DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]. DIFFIO: indicates that all general IOs support differential input/output, such as LVDS;

PIN name	PIN type	PIN description
		[L0, L1, L2, R0, R1, R2]: indicates BANK names [0…n]: indicates the unique differential pair number in the BANK; [N, P]: N indicates the negative end of the differential pair and P represents the positive end.
Multiplexed Pin		
DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]/XXX		Multiplexed pins are marked as DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]/XXX, where XXX indicates one or more of the functions described below. When the multiplexed pin is not used for special applications, it can serve as a general IO
--Configuration Pin		
MODE_2, MODE_1, MODE_0	input	They are used for configuration mode selection during configuration, as follows: 000: JTAG 001: Master SPI (X1, X2, X4, X8) 010: Master BPI (X8, X16) 011: Slave Serial (X1) 100: Slave Parallel (X8, X16, X32) 101: Slave SPI (X1) 111: Internal Master SPI (X1, X2, X4)
INIT_FLAG_N	Bidirectional (open-drain)	When the FPGA powers up completion during configuration, the pin is driven to a low level. Once the FPGA completes initialization, the pin is released. During configuration, this pin serves as an output for the configuration error indication state. During the configuration or initialization process, this pin can also accept an external low-level input to indicate an error or delay the configuration.
CFG_CLK	input/output	Configuration Clock Pin. In the slave mode, the pin serves as a clock input to obtain configuration data from external sources; In the master mode, the pin serves as a clock output to obtain configuration data from external sources;
D[31, 30…1, 0]	input/output	32-bit configuration data bus input/output pins: (1) In the Master SPI X1 configuration mode, pin D[0], as command output, is connected to the data input of the SPI flash, and pin D[1], as data input, is connected to the data output of the SPI flash. (2) In the Master SPI X2 configuration mode, pins D[1:0] serve as the data bus. (3) In the Master SPI X4 configuration mode, pins D[3:0] serve as the data bus. (4) In the Master SPI X8 configuration mode, pins D[3:0] serve as the data bus for the first SPI FLASH, and pins D[7:4] serve as the data bus for the second SPI FLASH. (5) In the Slave Serial configuration mode, pin D[1] serves as the data bus. (6) In the Slave SPI configuration mode, pin D[0] is for the master device output and slave device

PIN name	PIN type	PIN description
		input, pin D[1] is for the master device input and slave device output, and pin D[3] is for chip hold. (7) In the Master BPI configuration X8 asynchronous mode, pins D[7:0] serve as an 8-bit data bus. (8) In the Master BPI configuration X16 asynchronous/synchronous mode, pins D[15:0] serve as a 16-bit data bus. (9) In the Slave Parallel X8 configuration mode, pins D[7:0] are an 8-bit data bus. (10) In the Slave Parallel X16 configuration mode, pins D[15:0] are a 16-bit data bus. (11) In the Slave Parallel X32 configuration mode, pins D[31:0] are a 32-bit data bus.
CS_N	input	Multi-function Configuration Pin. for chip select input. Active low. (1) When it is low level, this pin enables the Slave Parallel mode configuration interface. (2) In other configuration modes, this pin is high-z. (3) To make this pin continue playing its configuration function after configuration is complete, users need to set the configuration register to preserve its configuration function.
RWSEL	input	Multi-function Configuration Pin. For selecting the read/write input in the Slave Parallel configuration mode (high for read and low for write). (1) When it is high level, the Slave Parallel configuration mode reads data from the data bus; (2) When it is low level, the Slave Parallel configuration mode writes data to the data bus; (3) Read and write can be switched only when CS_N is high level. (4) To make this pin continue playing its configuration function after configuration is complete, users need to set the configuration register to preserve its configuration function. (5) In other configuration modes, this pin is high-z.
BUSY	output	Multi-function Configuration Pin. (1) During readback in the Slave Parallel mode, a high level output indicates that the data read from the bus is invalid. (2)To make this pin continue playing its configuration function in the user mode, users need to set the configuration register to preserve its configuration function. (3) In other configuration modes, this pin is in the high-z state.
CSO_DOUT	output	Multi-function Configuration Pin. Needed for cascade. (1) In the Master SPI and X1 mode, this pin serves as cascaded data output; (2) In the Slave Serial configuration mode, this pin serves as cascaded data output; (3) In the Slave Parallel configuration mode, this

PIN name	PIN type	PIN description
		pin serves as a chip select signal output;
FCS_N	output	Multi-function configuration pin, used for the external Master SPI configuration mode. (1) In the Master SPI mode, this pin outputs a chip select signal to external flash, active-low;
VS1, VS0	input	Multi-function configuration pins, used in the Master SPI or internal Master SPI mode. (1) It is used for selecting the bitstream version: 00 for the first set of bitstreams, 01 for the second set, 10 for the third set, 11 for the fourth set; (2) Enable the internal pull-down resistors during configuration.
IO_STATUS_C	input	Multi-function pin, used for inputting signals and controlling the state of all general IOs during the configuration process. (1) "1" keeps all general IOs in a pull-up state during configuration. (2) "0" keeps all general IOs in a tri-state during configuration.
ADR[25:0]	output	Multi-function configuration pins, used for outputting addresses in the BPI configuration mode.
BFOE_N	output	Multi-function configuration pin, used for providing a low-level output enable control signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, this pin should be connected to the flash's output enable input and to VCCIO via a 4.7K resistor.
BADRVO_N	output	Multi-function configuration pin, used for providing a low-level address valid control signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, if the external FLASH supports address valid signal input, then this pin should be connected to the FLASH's address valid input pin and to VCCIO via a 4.7K resistor. If the external flash does not support address valid signal input, then there is no need to connect this pin.
BFWE_N	output	Multi-function configuration pin, used for providing a low-level write enable signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, this pin should be connected to the flash's write enable input and to VCCIO via a 4.7K resistor;
BFCE_N	output	Multi-function configuration pin, used for providing a low-level chip select control signal for parallel NOR FLASH in the BPI configuration mode; (1) In the BPI configuration mode, should be connected to the flash's chip select input and to VCCIO via a 4.7K resistor.
FCS2_N	output	Multi-function configuration pin, used for the

PIN name	PIN type	PIN description
		external Master SPI X8 configuration mode. (1) In the Master SPI X8 mode, this pin outputs a chip select signal to the external flash, active-low. The pin should be connected to VCCIO via an external pull-up resistor not more than 4.7K.
ECCLKIN	input	Multi-function configuration pin, used for inputting signals and serves as clock input for the Master configuration mode.
-- Clock, PLL, Crystal Oscillator Multi-function Pin		
CLK[0,1,2,3]_[L0,L1,L2,R0,R1,R2]	input	Dedicated global clock input pins, 4 pins for each bank
DIFFCLK[0,1]_[L0,L1,L2,R0,R1,R2]_[N, P]	input	Dedicated global differential clock input pins, 2 pairs for each bank
PLL[0,1,2,…10]_CLKOUT_[P,N]	output	Direct selection of PLL[0, 1, …, 19] output to these pins are possible
PLL[0,1,2,…10]_CLKIN[0,1,2,3]	input	Optional PLL input, PLL can select directly the input clock from these pins
PLL[0,1,2,…10]_CLKFB_[P,N]	input	Optional PLL feedback clock input, PLL can input external feedback clock from these pins
XTALA_[L0,L1,L2,R0,R1,R2]	input	Dedicated external crystal input at port A. Input for the on-die inverter, 1 pin for each bank
XTALB_[L0,L1,L2,R0,R1,R2]	output	Dedicated external crystal output at port B. Output for the on-die inverter, 1 pin for each bank
-- External Memory Interface Pin		
DQS[0,1,2][#]_[L0,L1,L2,R0,R1,R2]	input/output	Used to connect to the DQS/DQS# signal pins of external memory
DQ[0,1,2]_[L0,L1,L2,R0,R1,R2]	input/output	Can connect to the DQ signal pins of external memory
--HMEMC Memory Interface Pin		
[R,L]_A[0,..,15]	output	DDR memory address
[R,L]_CS_N	output	DDR memory chip selection signal, active-low, depends on whether the memory is in use.
[R,L]_RAS_N	output	RAS, active-low
[R,L]_CAS_N	output	CAS, active-low
[R,L]_WE_N	output	Write enable, active-low
[R,L]_BA[0,1,2]	output	DDR BANK address
[R,L]_ODT	output	ODT, on-die terminal
[R,L]_CK	output	Clock P side of DDR memory
[R,L]_CK_N	output	Clock N side of DDR memory
[R,L]_CKE	output	DDR memory clock enable signal, active-high
[R,L]_RESET_N	output	DDR memory reset, active-low
[R,L]_DML	output	Write data mask signals of DQ0-DQ7
[R,L]_DQSL	input/output	DQS signals related to DQ0-DQ7
[R,L]_DQSL_N	input/output	DQS# signals related to DQ0-DQ7
[R,L]_DQ[0,…,15]	input/output	Memory data bus
[R,L]_DMU	output	Write data mask signals of DQ8-DQ15

PIN name	PIN type	PIN description
[R,L]_DQSU	input/output	DQS signals related to DQ8-DQ15
[R,L]_DQSU_N	input/output	DQS# signals related to DQ8-DQ15
[R,L]_DQSL_GATE_IN	input	DQS gate window signal feedback (low bit) after compensating for read command path delay
[R,L]_DQSL_GATE_OUT	output	DQS gate window signal output (low bit) after compensating for read command path delay
[R,L]_DQSU_GATE_IN	input	DQS gate window signal feedback (high bit) after compensating for read command path delay
[R,L]_DQSU_GATE_OUT	output	DQS gate window signal output (high bit) after compensating for read command path delay
--Reference Pin		
RRP_[L0,L1,L2,R0,R1,R2]	input	External reference resistor pins, one for each bank. Provides a reference resistor to the power supply for on-die terminal resistor adjustment.
RRN_[L0,L1,L2,R0,R1,R2]	input	External reference resistor pins, one for each bank. Provides a reference resistor to the ground for on-die terminal resistor adjustment.
VREF_[L0,L1,L2,R0,R1,R2]	input	External reference voltage pins, one for each bank. Provides reference voltage input for each BANK
--ADC Pin		
VAUX[9,8,7,..0]	input	Input analog signals
Dedicated Pin		
--Configuration Pin, JTAG Pin		
CFG_DONE	Bidirectional (open-drain)	Dedicated pin for configuration state. Serves as a status output, this pin is driven to low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.
RST_N	input	Dedicated configuration input pin, internally weak pull-up, for restarting the configuration process, active-low. It is recommended that users externally pull up the RST_N with a resistor when using this pin. When this pin is low level, the FPGA enters a reset state, and all IOs are in the high-z state.
TCK	input	Dedicated JTAG test clock input pin
TMS	input	Dedicated JTAG test mode selection input pin
TDI	input	Dedicated JTAG test data input pin.
TDO	output	Dedicated JTAG test data output pin.
--Reference Pin		
REXT	input	Dedicated external high-precision resistor pin, with a resistance of 10k and an accuracy of 1%. Provides resistance for the bandgap.
--ADC Pin		
VA[1,0]	input	Dedicated analog input signals
VREF_EXT	input	Dedicated external reference 2.5V voltage.
Power Pin, Ground Pin		

PIN name	PIN type	PIN description
VCC	POWER	Core power, 1.1V. Power supply for core logic
VCCAUX	POWER	3.3V auxiliary power supply for IOB, LDO, and other modules as well as SDRAM
VCCIO[L0,L1,L2,R0,R1,R2]	POWER	IO BANK power, the banks on the left are BANKL0, BANKL1, BANKL2, and so on from top to down; the banks on the right side are BANKR0, BANKR1, BANKR2, and so on from top to down
VCCAUX_A	POWER	Power supply for ADC, BANDGAP, POR and SDRAM
VSS	GROUND	GND relative to VCC&VCCAUX
VSSA	GROUND	GND relative to VCCAUX_A
VCCEFUSE	POWER	Efuse programming voltage
VCCIOCFG	POWER	BANKCFG power supply
SDRAM Power Supply	POWER	Supply power to the VDD and VDDQ of the packaged SDRAM in the device

Note: PGL22GS_LPG176 has 140 user IOs.

2.2.1 Pin Name list

Table 2-3 Pin Name List

Pin Number	Pin(Function)Name
1	VCCIOR0
2	DIFFIO_R0_4_N/BFCE_N
3	DIFFIO_R0_4_P/FCS2_N
4	DIFFIO_R0_2_N/VAUX0
5	DIFFIO_R0_2_P/VAUX1
6	DIFFIO_R0_5_N/BADRVO_N
7	DIFFIO_R0_5_P/BFOE_N
8	DIFFIO_R0_3_N/ECCLKIN
9	DIFFIO_R0_3_P
10	DIFFIO_R0_1_N/VAUX2
11	DIFFIO_R0_1_P/VAUX3
12	DIFFIO_R0_0_P/VAUX5
13	DIFFIO_R0_0_N/VAUX4
14	VCC
15	VCC
16	VCCAUX_A
17	VCCEFUSE
18	TCK
19	TMS
20	TDO
21	TDI
22	VCCIOCFG

Pin Number	Pin(Function)Name
23	RST_N
24	CFG_DONE
25	REXT
26	VCCAUX_A
27	SDRAM Power Supply (VDDQ+VDD)
28	DIFFIO_L0_0_N
29	DIFFIO_L0_0_P/BUSY
30	DIFFIO_L0_1_N/VAUX8
31	DIFFIO_L0_1_P/VAUX9
32	VSS
33	VSS
34	DIFFIO_L0_3_N/CFG_CLK
35	DIFFIO_L0_3_P/IO_STATUS_C
36	DIFFIO_L0_5_P/MODE_0
37	DIFFIO_L0_4_P/FCS_N
38	DIFFIO_L0_4_N/CS_N
39	VCCIOL0
40	DIFFIO_L0_7_N/INIT_FLAG_N
41	DIFFIO_L0_9_P/CLK0_L0/DIFFCLK0_L0_P/PLL0_CLKFB_P/XTALA_L0
42	DIFFIO_L0_8_P/PLL0_CLKOUT_P
43	DIFFIO_L0_8_N/PLL0_CLKOUT_N
44	DIFFIO_L0_9_N/CLK1_L0/DIFFCLK0_L0_N/PLL0_CLKFB_N/XTALB_L0
45	DIFFIO_L0_10_P/CLK2_L0/DIFFCLK1_L0_P/PLL1_CLKIN0
46	DIFFIO_L0_10_N/CLK3_L0/DIFFCLK1_L0_N/PLL1_CLKIN1
47	DIFFIO_L0_11_P/PLL1_CLKIN2
48	DIFFIO_L0_11_N/PLL1_CLKIN3
49	DIFFIO_L0_12_P/D0
50	DIFFIO_L0_12_N/RRN_L0/D1
51	DIFFIO_L0_13_P/RRP_L0/D2
52	DIFFIO_L0_13_N/D3
53	DIFFIO_L0_14_P/D4
54	DIFFIO_L0_14_N/D5
55	DIFFIO_L0_15_P/D6
56	DIFFIO_L0_15_N/D7
57	DIFFIO_L0_16_P/D8
58	VCCIOL0
59	DIFFIO_L0_16_N/D9
60	DIFFIO_L0_17_P/D10
61	DIFFIO_L0_17_N/D11
62	DIFFIO_L0_18_P/D12
63	DIFFIO_L0_18_N/D13
64	DIFFIO_L0_19_P/D14

Pin Number	Pin(Function)Name
65	DIFFIO_L0_19_N/D15
66	VCC
67	VCCAUX
68	VCCIOL1
69	DIFFIO_L2_0_P
70	DIFFIO_L2_0_N
71	DIFFIO_L2_1_P
72	DIFFIO_L2_1_N
73	DIFFIO_L2_2_P
74	DIFFIO_L2_2_N
75	DIFFIO_L2_3_P
76	VCCIOL2
77	DIFFIO_L2_3_N
78	DIFFIO_L2_4_P
79	DIFFIO_L2_4_N
80	DIFFIO_L2_5_P
81	DIFFIO_L2_5_N
82	DIFFIO_L2_6_P
83	DIFFIO_L2_6_N/VREF_L2
84	DIFFIO_L2_7_P
85	DIFFIO_L2_8_P/PLL4_CLKOUT_P
86	DIFFIO_L2_7_N
87	DIFFIO_L2_8_N/PLL4_CLKOUT_N
88	DIFFIO_L2_9_P/CLK0_L2/DIFFCLK0_L2_P/PLL4_CLKFB_P/XTALA_L2
89	DIFFIO_L2_9_N/CLK1_L2/DIFFCLK0_L2_N/PLL4_CLKFB_N/XTALB_L2
90	DIFFIO_L2_10_P/CLK2_L2/DIFFCLK1_L2_P/PLL5_CLKIN0
91	DIFFIO_L2_11_P/PLL5_CLKIN2
92	DIFFIO_L2_11_N/PLL5_CLKIN3
93	DIFFIO_L2_10_N/CLK3_L2/DIFFCLK1_L2_N/PLL5_CLKIN1
94	DIFFIO_L2_13_P/RRP_L2
95	DIFFIO_L2_13_N
96	VCCIOL2
97	DIFFIO_L2_15_P
98	DIFFIO_L2_15_N
99	DIFFIO_L2_17_N
100	DIFFIO_L2_18_N
101	DIFFIO_L2_18_P
102	DIFFIO_L2_16_N
103	DIFFIO_L2_16_P
104	DIFFIO_L2_19_N
105	DIFFIO_L2_14_N
106	DIFFIO_L2_14_P

Pin Number	Pin(Function)Name
107	DIFFIO_L2_19_P
108	DIFFIO_L2_12_N/RRN_L2
109	DIFFIO_L2_12_P
110	SDRAM Power Supply (VDDQ+VDD)
111	VCC
112	VCC
113	VCCAUX_A
114	DIFFIO_R2_19_P
115	DIFFIO_R2_19_N
116	DIFFIO_R2_14_P
117	DIFFIO_R2_14_N
118	DIFFIO_R2_16_P
119	DIFFIO_R2_16_N
120	DIFFIO_R2_18_P
121	DIFFIO_R2_18_N
122	DIFFIO_R2_17_N
123	DIFFIO_R2_17_P
124	DIFFIO_R2_15_N
125	DIFFIO_R2_12_N/RRN_R2
126	DIFFIO_R2_12_P
127	VCCIOR2
128	DIFFIO_R2_13_N
129	DIFFIO_R2_13_P/RRP_R2
130	DIFFIO_R2_10_N/CLK3_R2/DIFFCLK1_R2_N/PLL5_CLKFB_N
131	DIFFIO_R2_11_N/PLL5_CLKOUT_N
132	DIFFIO_R2_11_P/PLL5_CLKOUT_P
133	DIFFIO_R2_10_P/CLK2_R2/DIFFCLK1_R2_P/PLL5_CLKFB_P
134	DIFFIO_R2_9_N/CLK1_R2/DIFFCLK0_R2_N/PLL4_CLKIN3/XTALB_R2
135	DIFFIO_R2_9_P/CLK0_R2/DIFFCLK0_R2_P/PLL4_CLKIN2/XTALA_R2
136	DIFFIO_R2_8_N/PLL4_CLKIN1
137	DIFFIO_R2_7_N
138	DIFFIO_R2_8_P/PLL4_CLKIN0
139	DIFFIO_R2_7_P
140	DIFFIO_R2_6_N/VREF_R2
141	DIFFIO_R2_6_P
142	DIFFIO_R2_5_N
143	DIFFIO_R2_5_P
144	DIFFIO_R2_4_N
145	DIFFIO_R2_4_P
146	DIFFIO_R2_3_N
147	VCCIOR2
148	DIFFIO_R2_3_P

Pin Number	Pin(Function)Name
149	DIFFIO_R2_2_N
150	DIFFIO_R2_2_P
151	DIFFIO_R2_1_N
152	DIFFIO_R2_1_P
153	DIFFIO_R2_0_N
154	DIFFIO_R2_0_P
155	VCCIOR1
156	VCCAUX
157	VCC
158	VCCAUX
159	VCCIOR0
160	VCCAUX
161	DIFFIO_R0_13_N/D19/ADR3
162	DIFFIO_R0_13_P/RRP_R0/D18/ADR2
163	DIFFIO_R0_12_N/RRN_R0/D17/ADR1
164	DIFFIO_R0_12_P/D16/ADR0
165	DIFFIO_R0_11_N/PLL1_CLKOUT_N
166	DIFFIO_R0_11_P/PLL1_CLKOUT_P
167	DIFFIO_R0_10_N/CLK3_R0/DIFFCLK1_R0_N/PLL1_CLKFB_N
168	DIFFIO_R0_10_P/CLK2_R0/DIFFCLK1_R0_P/PLL1_CLKFB_P
169	DIFFIO_R0_9_N/CLK1_R0/DIFFCLK0_R0_N/PLL0_CLKIN3/XTALB_R0
170	DIFFIO_R0_9_P/CLK0_R0/DIFFCLK0_R0_P/PLL0_CLKIN2/XTALA_R0
171	DIFFIO_R0_8_N/PLL0_CLKIN1
172	DIFFIO_R0_8_P/PLL0_CLKIN0
173	DIFFIO_R0_7_N/VS0
174	DIFFIO_R0_6_N/VREF_R0
175	DIFFIO_R0_7_P/VS1
176	DIFFIO_R0_6_P/BFWE_N
Ground Wire	VSS
Ground Wire	VSS
Ground Wire	VSS
Ground Wire	VSS
Ground Wire	VSS
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Pin Number	Pin(Function)Name
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2.2.2 SDRAM Wire Bonding List

Table 2-4 SDRAM Wire Bonding List

SDRAM Chip		FPGA Chip		
PAD#	**Pad Name**	**Pad#**	**Pad Name**	**Function Name**
1	NC	#N/A	#N/A	#N/A
2	VSS	491	VSSA_PLL1	VSS
3	DQ31	216	R1_PAD39	DIFFIO_R1_19_N
4	DQ30	215	R1_PAD38	DIFFIO_R1_19_P
5	VSSQ	441	VSS	VSS
6	VDDQ	Pin113	#N/A	SDRAM Power Supply
7	DQ29	214	R1_PAD37	DIFFIO_R1_18_N
8	DQ28	213	R1_PAD36	DIFFIO_R1_18_P
9	DQ27	212	R1_PAD35	DIFFI0_R1_17_N
10	DQ26	211	R1_PAD34	DIFFI0_R1_17_P
11	VSSQ	442	VSS	VSS
12	VDDQ	Pin156	#N/A	SDRAM Power Supply
13	DQ25	209	R1_PAD32	DIFFIO_R1_16_P
14	DQ24	208	R1_PAD31	DIFFI0_R1_15_N
15	NC	#N/A	#N/A	#N/A
16	DQM3	207	R1_PAD30	DIFFI0_R1_15_P
17	A3	206	R1_PAD29	DIFFIO_R1_14_N
18	A2	205	R1_PAD28	DIFFIO_R1_14_P
19	A1	204	R1_PAD27	DIFFI0_R1_13_N
20	A0	203	R1_PAD26	DIFFI0_R1_13_P/RRP_R1
21	A10	202	R1_PAD25	DIFFI0_R1_12_N/RRN_R1
22	BA0	201	R1_PAD24	DIFFIO_R1_12_P
23	BA1	200	R1_PAD23	DIFFIO_R1_11_N/PLL3_CLKOUT_N
24	VSS	445	VSS	VSS
25	NC	#N/A	#N/A	#N/A
26	CLK	199	R1_PAD22	DIFFIO_R1_11_P/PLL3_CLKOUT_P
27	NC	#N/A	#N/A	#N/A
28	VDD	Pin158	#N/A	SDRAM Power Supply
29	NC	#N/A	#N/A	#N/A
30	DQM1	197	R1_PAD20	DIFFIO_R1_10_P/CLK2_R1/DIFFCLK1_R1_P/PLL3_CLKFB_P
31	NC	#N/A	#N/A	#N/A
32	DQ8	196	R1_PAD19	DIFFIO_R1_9_N/CLK1_R1/DIFFCLK0_R1_N/PLL2_CLKIN3/XTALB_R1
33	DQ9	195	R1_PAD18	DIFFIO_R1_9_P/CLK0_R1/DIFFCLK0_R1_P/PLL2_CLKIN2/XTALA_R1
34	VDDQ	Pin158	#N/A	SDRAM Power Supply

SDRAM Chip		FPGA Chip		
PAD#	**Pad Name**	**Pad#**	**Pad Name**	**Function Name**
35	VSSQ	447	VSS	VSS
36	DQ10	188	R1_PAD11	DIFFI0_R1_5_N
37	DQ11	187	R1_PAD10	DIFFI0_R1_5_P/ADR25
38	DQ12	186	R1_PAD9	DIFFIO_R1_4_N/ADR24
39	DQ13	185	R1_PAD8	DIFFIO_R1_4_P/ADR23
40	VSSQ	449	VSS	VSS
41	VDDQ	Pin160	#N/A	SDRAM Power Supply
42	DQ14	180	R1_PAD3	DIFFI0_R1_1_N/ADR18
43	DQ15	179	R1_PAD2	DIFFI0_R1_1_P/ADR17
44	VSS	428	VSS	VSS
45	NC	#N/A	#N/A	#N/A
46	NC	#N/A	#N/A	#N/A
47	VDD	Pin110	#N/A	SDRAM Power Supply
48	DQ16	94	L1_PAD37	DIFFIO_L1_18_N
49	DQ17	93	L1_PAD36	DIFFIO_L1_18_P
50	VDDQ	Pin110	#N/A	SDRAM Power Supply
51	VSSQ	404	VSS	VSS
52	DQ18	90	L1_PAD33	DIFFIO_L1_16_N
53	DQ19	89	L1_PAD32	DIFFIO_L1_16_P
54	DQ20	88	L1_PAD31	DIFFI0_L1_15_N
55	DQ21	87	L1_PAD30	DIFFI0_L1_15_P
56	VSSQ	405	VSS	VSS
57	VDDQ	Pin110	#N/A	SDRAM Power Supply
58	DQ22	84	L1_PAD27	DIFFI0_L1_13_N
59	DQ23	83	L1_PAD26	DIFFI0_L1_13_P/RRP_L1
60	NC	#N/A	#N/A	#N/A
61	DQM2	82	L1_PAD25	DIFFI0_L1_12_N/RRN_L1
62	A4	81	L1_PAD24	DIFFIO_L1_12_P
63	A5	80	L1_PAD23	DIFFIO_L1_11_N/PLL3_CLKIN3
64	A6	79	L1_PAD22	DIFFIO_L1_11_P/PLL3_CLKIN2
65	A7	78	L1_PAD21	DIFFIO_L1_10_N/CLK3_L1/DIFFCLK1_L1_N/PLL3_CLKIN1
66	A8	77	L1_PAD20	DIFFIO_L1_10_P/CLK2_L1/DIFFCLK1_L1_P/PLL3_CLKIN0
67	A9	76	L1_PAD19	DIFFIO_L1_9_N/CLK1_L1/DIFFCLK0_L1_N/PLL2_CLKFB_N/XTALB_L1
68	CS	75	L1_PAD18	DIFFIO_L1_9_P/CLK0_L1/DIFFCLK0_L1_P/PLL2_CLKFB_P/XTALA_L1
69	RAS	74	L1_PAD17	DIFFIO_L1_8_N/PLL2_CLKOUT_N
70	CAS	73	L1_PAD16	DIFFIO_L1_8_P/PLL2_CLKOUT_P
71	WE	72	L1_PAD15	DIFFIO_L1_7_N
72	CKE	71	L1_PAD14	DIFFIO_L1_7_P

SDRAM Chip		FPGA Chip		
PAD#	**Pad Name**	**Pad#**	**Pad Name**	**Function Name**
73	VSS	409	VSS	VSS
74	VDD	Pin67	#N/A	SDRAM Power Supply
75	DQM0	67	L1_PAD10	DIFFI0_L1_5_P
76	NC	#N/A	#N/A	#N/A
77	DQ7	66	L1_PAD9	DIFFIO_L1_4_N
78	DQ6	65	L1_PAD8	DIFFIO_L1_4_P
79	VDDQ	Pin67	#N/A	SDRAM Power Supply
80	VSSQ	411	VSS	VSS
81	DQ5	62	L1_PAD5	DIFFIO_L1_2_N
82	DQ4	61	L1_PAD4	DIFFIO_L1_2_P
83	DQ3	60	L1_PAD3	DIFFI0_L1_1_N
84	DQ2	59	L1_PAD2	DIFFI0_L1_1_P
85	VSSQ	488	VSSA_PLL4	VSS
86	VDDQ	Pin27	#N/A	SDRAM Power Supply
87	DQ1	58	L1_PAD1	DIFFIO_L1_0_N
88	DQ0	57	L1_PAD0	DIFFIO_L1_0_P
89	VDD	Pin27	#N/A	SDRAM Power Supply
90	NC	#N/A	#N/A	#N/A

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