PG2L200H_FBB676

(PK04008, V1.0)

(10.14.2023)

Shenzhen Pango Microsystems Co., Ltd.

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	10.14.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Full Spelling
POD	Package Outline Drawing

Table of Contents

Tables

Figures

Chapter 1 Introduction to Packaging

PG2L200H_FBB676 uses a Bare Die Flip chip BGA type of packaging. Package size: 27x27mm; Number of balls: 676; Ball pitch: 1.0mm; Maximum package thickness: 2.310mm.

Chapter 2 Package Dimension and Pin

2.1 Package Dimension

Table 2-1 Dimensional Values

Unit: Millimeter

Dimension Symbol	Value			Dimension Symbol	Value		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	2.146	2.310	2.474	e	-	1.00	-
A1	0.40	0.50	0.60	b	0.50	0.60	0.70
A2	0.584	0.634	0.684	aaa	-	0.20	-
C	1.056	1.176	1.296	ccc	-	0.35	-
D	26.80	27.00	27.20	ddd	-	0.15	-
E	26.80	27.00	27.20	eee	-	0.25	-
D1	-	25.00	-	fff	-	0.10	-
E1	-	25.00	-	Ball Diam	-	0.60	-

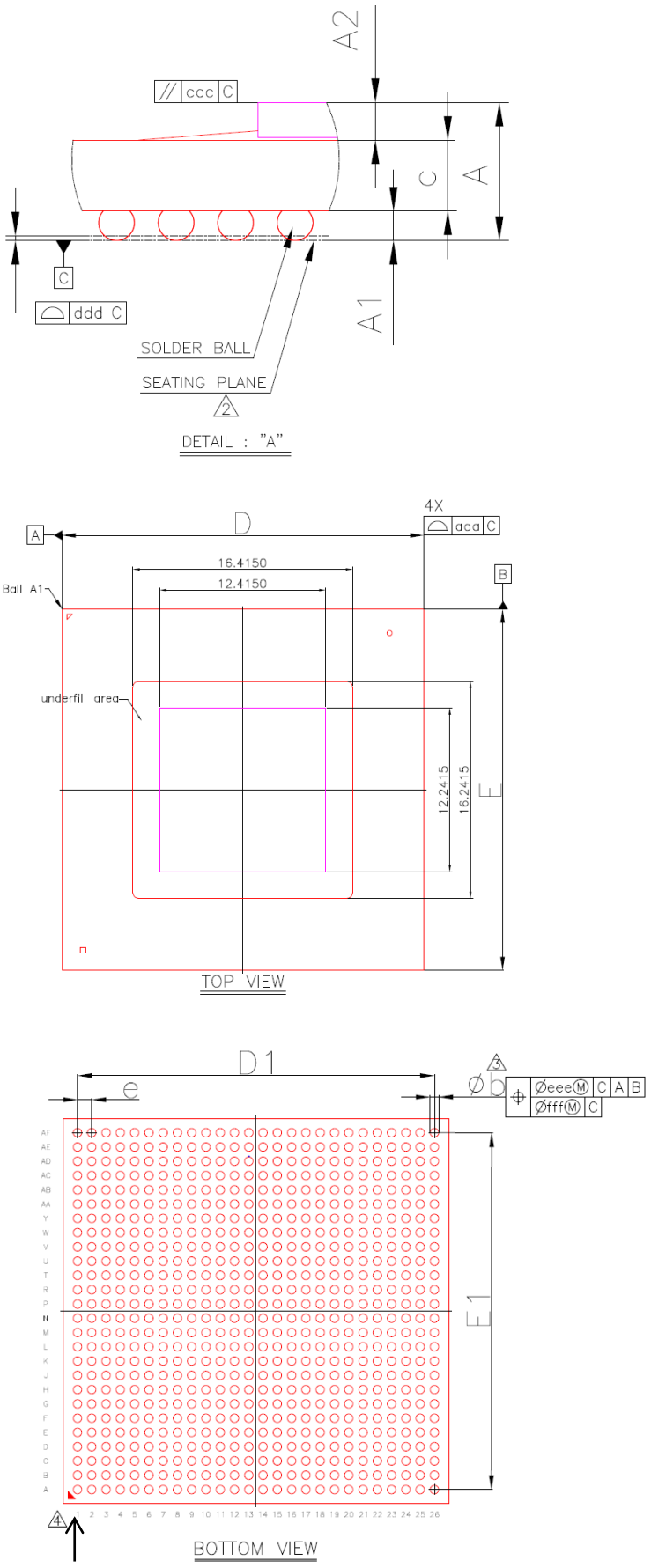

Figure 2-1 Package Outline Dimension (POD)

2.2 Pin Definitions

PG2L200H _ FBB676 has 400 user IOs.

Table 2-1 Product Pin Definitions

PIN Name	PIN Type	PIN Direction	PIN Description
General PIN			
DIFFIO_XX_GY_NN[P,N]	General	Input/Output	General pin; (1) "DIFFIO" indicates the pin supports differential input/output and can be used for transmitting and receiving LVDS signals; (2) " XX " indicates bank numbers, which can be L3, L4, L5, L6, L7, R4, R5, R6; (3) " G " indicates belonging to a memory group; (4) " Y " indicates the group number in a bank, each of which contains four groups; (5) "NN" indicates the sequence number of programmable IO pairs in a bank, increasing from 0, a bank contains 24 difference pairs; (6) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end。 During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri-state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.
SIO_XX_NN	General	Input/Output	General pin; (1) " SIO " indicates the pin only supports single ended input/output; (2) " XX " indicates bank numbers, which can be L3, L4, L5, L6, L7, R4, R5, R6; (3) "NN" indicates the sequence number of programmable IO in a bank, increasing from 0, a bank contains 2 single ended IOs; During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri- state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.
Configuration PIN			
INIT_FLAG_N	Dedicated	Bidirectional (open-drain)	Initialization and configuration status dedicated pin:

PIN Name	PIN Type	PIN Direction	PIN Description
			When it is low, it indicates that the FPGA is being initialized (clear configuration memory) or a configuration error has occurred. The pin has an internal weak pull-up resistor that is enabled during configuration; When the FPGA powers up completion, the pin is driven to low level. Once the FPGA completes initialization, the pin is released. During the power up and initialization process, this pin can accept an external low level input to delay the configuration process. When the FPGA detects high level input on this pin after initialization, the FPGA starts the configuration process.During configuration, this pin serves as an output for the configuration error indication state, and low level indicates that an error occurred. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. After the configuration is complete, user can configure weak pull-up or float state for this pin.
CFG_DONE	Dedicated	Bidirectional (open-drain)	Dedicated configuration status pin, built in weak pull-up resistor about 10K. Output as the configuration completion indicator, high level indicates that the configuration is complete. This pin is an open-drain output. When the FPGA powers up completion, the pin is driven to low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released. After the configuration is complete, the pin can be driven externally to low level, Once the internal start-up timing finds that the external DONE pin is low and the internal start-up circuit stops until the external pin is high. After the configuration is complete, user can configure weak pull-up or float state for this pin.
RSTN	Dedicated	Input	Dedicated configuration reset pin, built in weak pull-up resistor and always effective. For restarting configuration logic and configuration memory, active-low. When this pin is low, the FPGA configuration memory is emptied and a new configuration process begins. The configuration logic reset begins with the falling edge of the pin, and the configuration process begins with the

PIN Name	PIN Type	PIN Direction	PIN Description
			rising edge of the pin. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. Keeping this pin low during power up does not put the FPGA configuration logic in a reset state. After the configuration is complete, user can configure weak pull-up or float state for this pin.
CFG_CLK	Dedicated	Input/Output	Configuration clock pin. Except for the JTAG configuration mode, the configuration process of the FPGA is synchronizing by this clock in other modes. In the slave serial and slave parallel configuration modes, the pin serves as a clock input to obtain configuration data from external sources. In the master SPI configuration mode, the pin serves as a clock output to obtain configuration data from external sources and an external pull-up resistor of 1K is required. When the clock is not needed (such as in the JTAG mode), this pin is in the High-Z state. After the configuration is complete, user can configure weak pull-up or float state for this pin.
TCK	Dedicated	Input	Test clock input pin compliant with IEEE STD 1149.1 and provides a clock for the JTAG chain of the FPGA. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TMS	Dedicated	Input	Dedicated JTAG test mode selection input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDI	Dedicated	Input	Dedicated JTAG test data input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDO	Dedicated	Iutput	Dedicated JTAG test data output pin Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
MODE_2	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_1	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to

PIN Name	PIN Type	PIN Direction	PIN Description
			VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_0	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
SCBV	Dedicated	Input	The pin is always effective on BANKCFG, but only on BANK which the multiplexing configuration pins is located during configuration. When the voltage of VCCIOCFG is 2.5V or 3.3V, the pin must be connected to high level and can be connected directly to the VCCIOCFG. When the voltage of VCCIOCFG is 1.8V or lower, the pin must be connected to low level and can be connected directly to the ground. Note: The pin must be used in conjunction with the software, and the SCBV selection in the bitstream setting must be consistent with the hardware setting. For details about the SCBV pin pull-up/pull-down level corresponds to the configured BANK power, see "UG040012_Logos2 Family Hardware Design Guide".
FCS_N	Multiplexed	Output	Multi-function configuration pin, used for the Master SPI configuration mode. (1) In the Master SPI X1, X2 and X4 modes, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
MOSI_D0	Multiplexed	Input/Output	Multi-function configuration data pin. (1) "MOSI", in the master SPI X1 mode; this pin used for serial data output and connects to the data input pin of the external SPI flash (such as DQ0, D, SI, IO0, etc). After the command and address are sent to the external SPI flash, the pin output high-Z or weak pull-up, depending on the state of the IO_STATUS_C pin. (2) In the master SPI X2, X4 and X8 modes, the pin is bidirectional data port, as command and address output to the

PIN Name	PIN Type	PIN Direction	PIN Description
			external SPI flash. Receive the lowest bit data from the external SPI flash. The pin connects to the bidirectional data pin of the external SPI flash (such as DQ0, D, SI, IO0, etc). (3) “ D0” , in the slave parallel mode, this pin serves as the D[0] bit of the data bus. (4) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (5) After the configuration is complete, the pin serves as a general pin.
MISO_D1_DI	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X1 mode, “ MISO” serves as data input and connects to the data output pin of the external SPI flash (such as DQ1, Q, SO, IO1, etc). (2) In the master SPI X2, X4 and X8 modes, “D1” connects to the second serial data output pin of the external SPI flash (such as DQ1, Q, SO, IO1, etc). (3) In the slave parallel mode, this pin serves as the D[1] bit of the data bus. (4) In the slave serial mode, “D1” serves as data input pin. (5) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. In the other configuration modes(such as JTAG), the state on the pin is ignored (6) After the configuration is complete, the pin serves as a general pin.
D[2, 3]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X4 and X8 modes, serve as data input and connects to the data output pin of the external SPI flash. “D2” connects to the third bit data output pin of the external SPI flash (such as DQ2, W#, WP#, IO2, etc). “D3” connects to the fourth bit data output pin of the external SPI flash (such as DQ3, HOLD#, IO3, etc). These pins should be connected to VCCIO via an external weak pull-up resistor of 4.7K. (2) In the slave parallel mode, these pins serve as the D[3:2] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[4, 5, 6, 7]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X8 mode, connect to the second flash in the same way as

PIN Name	PIN Type	PIN Direction	PIN Description
			D[3:0]. (2) In the slave parallel mode, these pins serve as the D[7:4] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[8,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1)In the slave parallel X16 and X32 modes, serve as the D[15:8] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
D[16,…,31]_A[0,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the slave parallel X32 mode, serve as the D[31:16] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
A[16,…,28]	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (2) After the configuration is complete, these pins serve as general pins.
CS_N	Multiplexed	Input	Multi-function configuration pin. For chip select input. Active low. (1) When it is low level, this pin enables the slave parallel mode configuration interface. In the slave parallel configuration mode, the external controller can select the slave parallel bus of the FPGA by controlling this pin. Or this pin connected to the previous FPGA CSO_DOUT pin in the slave parallel configuration chain. (2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
RWSEL	Multiplexed	Input	Multi-function configuration pin. For selecting the read/write input in the slave parallel configuration mode (high for read and low for write). (1) When it is high level, the slave parallel configuration mode reads data from the data bus. (2) When it is low level, the slave parallel

PIN Name	PIN Type	PIN Direction	PIN Description
			configuration mode writes data to the data bus. (3) Read and write can be switched only when CS_N is high level. (4) After the configuration is complete, the pin serves as a general pin. (5) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state.
CSO_DOUT	Multiplexed	Output(OD），Output	Multi-function configuration pin. Needed for cascade. (1) In the master SPI X1 mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2) In the slave serial configuration mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (3) In the slave parallel cascade configuration mode, this pin serves as a chip select signal open-drain output, connects to downstream chip CS_N pin and should be connected to VCCIO via an external pull-up resistor of 330Ω. (4) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state.
VS[0, 1]	Multiplexed	Output	Multi-function configuration pin. After the configuration is complete, these pins as general pins.
IO_STATUS_C	Multiplexed	Input	Multi-function configuration pin, used for controlling whether the weak pull-up resistors for all general pins are enabled during the configuration process. (1) When it is set to "0", the internal pull-up resistors for all general pins are enabled. (2) When it is set to "1", the internal pull-up resistors for all general pins are disabled. (3)It is recommended that the pin connects to VCCIO via an external weak pull-up resistor. (4)The pin can connect to VCCIO or VSS, either directly or via an external resistor of no more than 1K. (5) This pin must not be left floating before or during configuration.
ECCLKIN	Multiplexed	Input	The external clock input for the Master configuration mode, which is an optional external clock input to the configuration

PIN Name	PIN Type	PIN Direction	PIN Description
			logic. (1) In the master SPI mode, the FPGA can select this clock input as the configuration clock for the configuration logic. This clock can be divided (Depends on the settings in the bitstream) and output from the CFG_CLK pin. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.
BFOE_N	Multiplexed	Output	Multi-function configuration pin. After the configuration is complete, the pin as a general pin.
BFWE_FCS2_N	Multiplexed	Output	Multi-function configuration pin used for the master SPI X8 configuration modes. (1) In the Master SPI X8 mode, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin as a general pin.
BADRVO_N	Multiplexed	Output	Multi-function configuration pin. After the configuration is complete, the pin as a general pin.
ClockPIN			
GMCLK	Multiplexed	Input	Multiplexing global multi-regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL, PPLL, and also drive the multi-regional clock buffer. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. When these pins serve as single regional clock sources, they are able to drive all the IO clock buffers and regional clock buffers of the BANK.
GSCLK	Multiplexed	Input	Multiplexing global single regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL and PPLL. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. They are able to drive all the IO clock buffers and regional clock buffers of the BANK.

PIN Name	PIN Type	PIN Direction	PIN Description
Memory Interface PIN			
DQS	Multiplexed	N/A	DDR DQS PIN, each memory group contains two pins.
Reference PIN			
VREF	Multiplexed	N/A	Input reference voltage pins,. When not used as external reference voltage pins, these pins serve as general pins,
Power/ Ground PIN			
VCC	Dedicated	Power	Core logic power, 1.0V. Power supply for core logic.
VCC_DRM	Dedicated	Power	DRM power, 1.0V. Dedicated power supply for DRM. If the voltage is the same as VCC, it can be connected to VCC at the board.
VCCA	Dedicated	Power	Analog power, 1.8V. Power supply for internal analog circuit.
VCCIO[L3, L4, L5, L6, L7, R4, R5, R6, CFG]	Dedicated	Power	IO BANK power.
VCCB	Dedicated	Power	Key memory backup battery power supply voltage, 1.0V~1.9V. When the key function is not used, the pin needs to be connected to the VCCA or ground.
VSS	Dedicated	Ground	Ground
ADC PIN			
VCCADC	Dedicated	Power	ADC analog power, 1.8V. Power supply for ADC analog circuit.
VSSADC	Dedicated	Ground	GND relative to VCCADC
VAADC_P	Dedicated	Input	ADC dedicated analog differential input (Positive).
VAADC_N	Dedicated	Input	ADC dedicated analog differential input (Negative).
VREFADC_P	Dedicated	N/A	1.255V ADC reference voltage pin.
VREFADC_N	Dedicated	N/A	ADC reference voltage ground.
VAA[0,..,15]P,VAA[0,..,15]N	Multiplexed	Input	ADC differential analog input signals.
TSDP	Dedicated	N/A	Positive pin of the temperature sensor diode. When not used temperature diode, the pin needs to be connected to the VSS. When temperature sensor diode is to be used, then appropriate external temperature monitoring chip is required.
TSDN	Dedicated	N/A	Negative pin of the temperature sensor diode.
HSST PIN			
HSSTAVCC_G[3, 7]	Dedicated	Power	1.0V analog power pin, power supply for HSST internal transmits and receives circuit.
HSSTAVCCPLL_ G[3, 7]	Dedicated	Power	1.2V analog power pin, power supply for HSST internal PLL.
HSSTRREF_Q[L3, L7]	Dedicated	Input	Calibration resistance input pin of the terminal resistance calibration circuit.
HSSTREFCLK[0,1]P_Q[L3, L7]	Dedicated	Input	Positive end of differential clock input pin, provide a reference clock to HSST.

PIN Name	PIN Type	PIN Direction	PIN Description
HSSTREFCLK[0,1]N_Q[L3, L7]	Dedicated	Input	Negative end of differential clock input pin, provide a reference clock to HSST.
HSSTTX[0,1,2,3][P,N]_Q[L3, L7]	Dedicated	Output	Channel differential outputs of HSST. Each HSST has 4 pairs.
HSSTRX[0,1,2,3][P,N]_Q[L3, L7]	Dedicated	Input	Channel differential inputs of HSST. Each HSST has 4 pairs.

2.2.1 Pin Name List

Table 2-2 Pin Name List

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L3	SIO_L3_00	H17		15.7	
L3	DIFFIO_L3_G0_00P	H14	IO_1_P	34.0	BANKL3_G0_DQS
L3	DIFFIO_L3_G0_00N	H15	IO_1_N	33.5	
L3	DIFFIO_L3_G0_01P	G17	IO_2_P	31.6	
L3	DIFFIO_L3_G0_01N	F17	IO_2_N	32.1	
L3	DIFFIO_L3_G0_02P_DQS	F18	IO_3_P	17.7	
L3	DIFFIO_L3_G0_02N_DQS	F19	IO_3_N	18.0	
L3	DIFFIO_L3_G0_03P	G15	IO_4_P	47.6	
L3	DIFFIO_L3_G0_03N	F15	IO_4_N	48.1	
L3	DIFFIO_L3_G0_04P	G19	IO_5_P	22.8	
L3	DIFFIO_L3_G0_04N	F20	IO_5_N	23.1	
L3	DIFFIO_L3_G0_05P	H16	IO_6_P	29.9	
L3	DIFFIO_L3_G0_05N_VREF	G16	IO_6_N	30.3	
L3	DIFFIO_L3_G1_06P	C17	IO_7_P	52.8	BANKL3_G1_DQS
L3	DIFFIO_L3_G1_06N	B17	IO_7_N	52.8	
L3	DIFFIO_L3_G1_07P	E16	IO_8_P	46.8	
L3	DIFFIO_L3_G1_07N	D16	IO_8_N	47.3	
L3	DIFFIO_L3_G1_08P_DQS	A17	IO_9_P	71.3	
L3	DIFFIO_L3_G1_08N_DQS	A18	IO_9_N	71.8	
L3	DIFFIO_L3_G1_09P	B19	IO_10_P	65.2	
L3	DIFFIO_L3_G1_09N	A19	IO_10_N	65.7	
L3	DIFFIO_L3_G1_10P_GSCLK	E17	IO_11_P	45.1	
L3	DIFFIO_L3_G1_10N_GSCLK	E18	IO_11_N	45.4	
L3	DIFFIO_L3_G1_11P_GMCLK	D18	IO_12_P	46.0	
L3	DIFFIO_L3_G1_11N_GMCLK	C18	IO_12_N	46.5	
L3	DIFFIO_L3_G2_12P_GMCLK	D19	IO_13_P	50.4	BANKL3_G2_DQS
L3	DIFFIO_L3_G2_12N_GMCLK	C19	IO_13_N	50.7	
L3	DIFFIO_L3_G2_13P_GSCLK	E20	IO_14_P	38.1	
L3	DIFFIO_L3_G2_13N_GSCLK	D20	IO_14_N	38.1	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L3	DIFFIO_L3_G2_14P_DQS	B20	IO_15_P	66.0	
L3	DIFFIO_L3_G2_14N_DQS	A20	IO_15_N	66.2	
L3	DIFFIO_L3_G2_15P	C21	IO_16_P	50.6	
L3	DIFFIO_L3_G2_15N	B21	IO_16_N	50.9	
L3	DIFFIO_L3_G2_16P	B22	IO_17_P	72.8	
L3	DIFFIO_L3_G2_16N	A22	IO_17_N	73.1	
L3	DIFFIO_L3_G2_17P	E21	IO_18_P	41.3	
L3	DIFFIO_L3_G2_17N	D21	IO_18_N	41.5	
L3	DIFFIO_L3_G3_18P	C22	IO_19_P	59.1	BANKL3_G3_DQS
L3	DIFFIO_L3_G3_18N_VREF	C23	IO_19_N	59.6	
L3	DIFFIO_L3_G3_19P	B25	IO_20_P	73.6	
L3	DIFFIO_L3_G3_19N	A25	IO_20_N	73.9	
L3	DIFFIO_L3_G3_20P_DQS	A23	IO_21_P	75.7	
L3	DIFFIO_L3_G3_20N_DQS	A24	IO_21_N	76.0	
L3	DIFFIO_L3_G3_21P	C26	IO_22_P	74.6	
L3	DIFFIO_L3_G3_21N	B26	IO_22_N	75.0	
L3	DIFFIO_L3_G3_22P	C24	IO_23_P	77.4	
L3	DIFFIO_L3_G3_22N	B24	IO_23_N	77.8	
L3	DIFFIO_L3_G3_23P	D23	IO_24_P	49.6	
L3	DIFFIO_L3_G3_23N	D24	IO_24_N	50.0	
L3	SIO_L3_01	E22		51.9	
L4	SIO_L4_00	K18		8.5	
L4	DIFFIO_L4_G0_00P_VAA1P	K15	IO_25_P	35.6	BANKL4_G0_DQS
L4	DIFFIO_L4_G0_00N_VAA1N	J16	IO_25_N	35.3	
L4	DIFFIO_L4_G0_01P_VAA2P	J14	IO_26_P	43.7	
L4	DIFFIO_L4_G0_01N_VAA2N	J15	IO_26_N	43.4	
L4	DIFFIO_L4_G0_02P_DQS_VAA3P	K16	IO_27_P	25.1	
L4	DIFFIO_L4_G0_02N_DQS_VAA3N	K17	IO_27_N	24.9	
L4	DIFFIO_L4_G0_03P	M14	IO_28_P	44.2	
L4	DIFFIO_L4_G0_03N	L14	IO_28_N	44.3	
L4	DIFFIO_L4_G0_04P_VAA5P	M15	IO_29_P	40.7	
L4	DIFFIO_L4_G0_04N_VAA5N	L15	IO_29_N	40.7	
L4	DIFFIO_L4_G0_05P	M16	IO_30_P	29.1	
L4	DIFFIO_L4_G0_05N_VREF	M17	IO_30_N	28.9	
L4	DIFFIO_L4_G1_06P_VAA7P	J19	IO_31_P	22.9	BANKL4_G1_DQS
L4	DIFFIO_L4_G1_06N_VAA7N	H19	IO_31_N	22.9	
L4	DIFFIO_L4_G1_07P_VAA8P	L17	IO_32_P	18.3	
L4	DIFFIO_L4_G1_07N_VAA8N	L18	IO_32_N	18.1	
L4	DIFFIO_L4_G1_08P_DQS_VAA9P	K20	IO_33_P	23.7	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L4	DIFFIO_L4_G1_08N_DQS_VAA9N	J20	IO_33_N	24.2	
L4	DIFFIO_L4_G1_09P_VAA10P	J18	IO_34_P	27.3	
L4	DIFFIO_L4_G1_09N_VAA10N	H18	IO_34_N	27.7	
L4	DIFFIO_L4_G1_10P_GSCLK	G20	IO_35_P	53.6	
L4	DIFFIO_L4_G1_10N_GSCLK	G21	IO_35_N	54.2	
L4	DIFFIO_L4_G1_11P_GMCLK	K21	IO_36_P	19.1	
L4	DIFFIO_L4_G1_11N_GMCLK	J21	IO_36_N	19.3	
L4	DIFFIO_L4_G2_12P_GMCLK	H21	IO_37_P	39.8	BANKL4_G2_DQS
L4	DIFFIO_L4_G2_12N_GMCLK	H22	IO_37_N	39.9	
L4	DIFFIO_L4_G2_13P_GSCLK	J23	IO_38_P	38.1	
L4	DIFFIO_L4_G2_13N_GSCLK	H23	IO_38_N	38.5	
L4	DIFFIO_L4_G2_14P_DQS	G22	IO_39_P	57.7	
L4	DIFFIO_L4_G2_14N_DQS_BADRVO_N	F22	IO_39_N	57.3	
L4	DIFFIO_L4_G2_15P_A28	J24	IO_40_P	43.6	
L4	DIFFIO_L4_G2_15N_A27	H24	IO_40_N	44.1	
L4	DIFFIO_L4_G2_16P_A26	F23	IO_41_P	65.1	
L4	DIFFIO_L4_G2_16N_A25	E23	IO_41_N	65.2	
L4	DIFFIO_L4_G2_17P_A24	K22	IO_42_P	27.6	
L4	DIFFIO_L4_G2_17N_A23	K23	IO_42_N	28.0	
L4	DIFFIO_L4_G3_18P_A22	G24	IO_43_P	64.2	BANKL4_G3_DQS
L4	DIFFIO_L4_G3_18N_VREF_A21	F24	IO_43_N	64.7	
L4	DIFFIO_L4_G3_19P_A20	E25	IO_44_P	72.0	
L4	DIFFIO_L4_G3_19N_A19	D25	IO_44_N	72.5	
L4	DIFFIO_L4_G3_20P_DQS	E26	IO_45_P	88.1	
L4	DIFFIO_L4_G3_20N_DQS_A18	D26	IO_45_N	88.6	
L4	DIFFIO_L4_G3_21P_A17	H26	IO_46_P	61.7	
L4	DIFFIO_L4_G3_21N_A16	G26	IO_46_N	62.2	
L4	DIFFIO_L4_G3_22P_BFOE_N	G25	IO_47_P	74.0	
L4	DIFFIO_L4_G3_22N_BFWE_FCS2_N	F25	IO_47_N	74.5	
L4	DIFFIO_L4_G3_23P_VS1	J25	IO_48_P	48.4	
L4	DIFFIO_L4_G3_23N_VS0	J26	IO_48_N	48.9	
L4	SIO_L4_01	L19		13.6	
L5	SIO_L5_00	M19		5.8	
L5	DIFFIO_L5_G0_00P_MOSI_D0	R14	IO_49_P	43.8	BANKL5_G0_DQS
L5	DIFFIO_L5_G0_00N_MISO_D1_DI	R15	IO_49_N	43.2	
L5	DIFFIO_L5_G0_01P_D2	P14	IO_50_P	14.3	
L5	DIFFIO_L5_G0_01N_D3	N14	IO_50_N	40.9	
L5	DIFFIO_L5_G0_02P_DQS_IO_STATUS_C	P15	IO_51_P	33.4	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L5	DIFFIO_L5_G0_02N_DQS_ECCLKIN	P16	IO_51_N	32.9	
L5	DIFFIO_L5_G0_03P_D4	N16	IO_52_P	26.8	
L5	DIFFIO_L5_G0_03N_D5	N17	IO_52_N	27.1	
L5	DIFFIO_L5_G0_04P_D6	R16	IO_53_P	30.9	
L5	DIFFIO_L5_G0_04N_D7	R17	IO_53_N	30.3	
L5	DIFFIO_L5_G0_05P_FCS_N	P18	IO_54_P	13.1	
L5	DIFFIO_L5_G0_05N_VREF_D8	N18	IO_54_N	12.5	
L5	DIFFIO_L5_G1_06P_D9	K25	IO_55_P	58.8	
L5	DIFFIO_L5_G1_06N_D10	K26	IO_55_N	59.3	
L5	DIFFIO_L5_G1_07P_D11	M20	IO_56_P	17.2	
L5	DIFFIO_L5_G1_07N_D12	L20	IO_56_N	17.2	
L5	DIFFIO_L5_G1_08P_DQS_N	L24	IO_57_P	53.9	
L5	DIFFIO_L5_G1_08N_DQS_D13	L25	IO_57_N	54.1	BANKL5_G1_DQS
L5	DIFFIO_L5_G1_09P_D14	M24	IO_58_P	42.8	
L5	DIFFIO_L5_G1_09N_D15	M25	IO_58_N	43.4	
L5	DIFFIO_L5_G1_10P_GSCLK	L22	IO_59_P	37.7	
L5	DIFFIO_L5_G1_10N_GSCLK	L23	IO_59_N	38.0	
L5	DIFFIO_L5_G1_11P_GMCLK	M21	IO_60_P	20.1	
L5	DIFFIO_L5_G1_11N_GMCLK	M22	IO_60_N	20.6	
L5	DIFFIO_L5_G2_12P_GMCLK	N21	IO_61_P	28.0	
L5	DIFFIO_L5_G2_12N_GMCLK	N22	IO_61_N	28.0	
L5	DIFFIO_L5_G2_13P_GSCLK	P20	IO_62_P	27.7	
L5	DIFFIO_L5_G2_13N_GSCLK	P21	IO_62_N	27.2	
L5	DIFFIO_L5_G2_14P_DQS_RWSEL	N23	IO_63_P	40.8	
L5	DIFFIO_L5_G2_14N_DQS_CSO_DOUT	N24	IO_63_N	41.3	BANKL5_G2_DQS
L5	DIFFIO_L5_G2_15P_CS_N	P19	IO_64_P	10.1	
L5	DIFFIO_L5_G2_15N_D31_A15	N19	IO_64_N	10.3	
L5	DIFFIO_L5_G2_16P_D30_A14	P23	IO_65_P	41.7	
L5	DIFFIO_L5_G2_16N_D29_A13	P24	IO_65_N	42.0	
L5	DIFFIO_L5_G2_17P_D28_A12	R20	IO_66_P	15.8	
L5	DIFFIO_L5_G2_17N_D27_A11	R21	IO_66_N	16.3	
L5	DIFFIO_L5_G3_18P_D26_A10	R25	IO_67_P	61.8	
L5	DIFFIO_L5_G3_18N_VREF_D25_A9	P25	IO_67_N	62.2	
L5	DIFFIO_L5_G3_19P_D24_A8	N26	IO_68_P	55.9	
L5	DIFFIO_L5_G3_19N_D23_A7	M26	IO_68_N	56.3	BANKL5_G3_DQS
L5	DIFFIO_L5_G3_20P_DQS	T24	IO_69_P	51.8	
L5	DIFFIO_L5_G3_20N_DQS_D22_A6	T25	IO_69_N	52.2	
L5	DIFFIO_L5_G3_21P_D21_A5	R26	IO_70_P	56.3	
L5	DIFFIO_L5_G3_21N_D20_A4	P26	IO_70_N	56.8	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L5	DIFFIO_L5_G3_22P_D19_A3	T22	IO_71_P	38.6	
L5	DIFFIO_L5_G3_22N_D18_A2	R22	IO_71_N	38.4	
L5	DIFFIO_L5_G3_23P_D17_A1	T23	IO_72_P	31.3	
L5	DIFFIO_L5_G3_23N_D16_A0	R23	IO_72_N	31.3	
L5	SIO_L5_01	R18		10.5	
L6	SIO_L6_00	U24		35.0	
L6	DIFFIO_L6_G0_00P	U25	IO_73_P	60.2	
L6	DIFFIO_L6_G0_00N	U26	IO_73_N	60.2	
L6	DIFFIO_L6_G0_01P	V26	IO_74_P	51.3	
L6	DIFFIO_L6_G0_01N	W26	IO_74_N	51.2	
L6	DIFFIO_L6_G0_02P_DQS	AB26	IO_75_P	85.4	
L6	DIFFIO_L6_G0_02N_DQS	AC26	IO_75_N	85.8	BANKL6_G0_DQS
L6	DIFFIO_L6_G0_03P	W25	IO_76_P	53.3	
L6	DIFFIO_L6_G0_03N	Y26	IO_76_N	53.8	
L6	DIFFIO_L6_G0_04P	Y25	IO_77_P	69.5	
L6	DIFFIO_L6_G0_04N	AA25	IO_77_N	69.4	
L6	DIFFIO_L6_G0_05P	V24	IO_78_P	42.0	
L6	DIFFIO_L6_G0_05N_VREF	W24	IO_78_N	41.8	
L6	DIFFIO_L6_G1_06P	AA24	IO_79_P	77.6	
L6	DIFFIO_L6_G1_06N	AB25	IO_79_N	78.1	
L6	DIFFIO_L6_G1_07P	AA22	IO_80_P	59.2	
L6	DIFFIO_L6_G1_07N	AA23	IO_80_N	58.7	
L6	DIFFIO_L6_G1_08P_DQS	AB24	IO_81_P	77.3	
L6	DIFFIO_L6_G1_08N_DQS	AC24	IO_81_N	77.6	BANKL6_G1_DQS
L6	DIFFIO_L6_G1_09P	V23	IO_82_P	36.7	
L6	DIFFIO_L6_G1_09N	W23	IO_82_N	36.3	
L6	DIFFIO_L6_G1_10P_GSCLK	Y22	IO_83_P	69.0	
L6	DIFFIO_L6_G1_10N_GSCLK	Y23	IO_83_N	68.6	
L6	DIFFIO_L6_G1_11P_GMCLK	U22	IO_84_P	26.0	
L6	DIFFIO_L6_G1_11N_GMCLK	V22	IO_84_N	26.5	
L6	DIFFIO_L6_G2_12P_GMCLK	U21	IO_85_P	30.4	
L6	DIFFIO_L6_G2_12N_GMCLK	V21	IO_85_N	30.3	
L6	DIFFIO_L6_G2_13P_GSCLK	W21	IO_86_P	47.8	
L6	DIFFIO_L6_G2_13N_GSCLK	Y21	IO_86_N	48.1	BANKL6_G2_DQS
L6	DIFFIO_L6_G2_14P_DQS	T20	IO_87_P	18.1	
L6	DIFFIO_L6_G2_14N_DQS	U20	IO_87_N	18.2	
L6	DIFFIO_L6_G2_15P	W20	IO_88_P	45.2	
L6	DIFFIO_L6_G2_15N	Y20	IO_88_N	44.9	
L6	DIFFIO_L6_G2_16P	T19	IO_89_P	17.1	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L6	DIFFIO_L6_G2_16N	U19	IO_89_N	16.6	
L6	DIFFIO_L6_G2_17P	V19	IO_90_P	23.9	
L6	DIFFIO_L6_G2_17N	W19	IO_90_N	23.5	
L6	DIFFIO_L6_G3_18P	V18	IO_91_P	26.8	BANKL6_G3_DQS
L6	DIFFIO_L6_G3_18N_VREF	W18	IO_91_N	26.3	
L6	DIFFIO_L6_G3_19P	T14	IO_92_P	40.9	
L6	DIFFIO_L6_G3_19N	T15	IO_92_N	40.9	
L6	DIFFIO_L6_G3_20P_DQS	T17	IO_93_P	15.3	
L6	DIFFIO_L6_G3_20N_DQS	T18	IO_93_N	15.0	
L6	DIFFIO_L6_G3_21P	U15	IO_94_P	30.5	
L6	DIFFIO_L6_G3_21N	U16	IO_94_N	30.0	
L6	DIFFIO_L6_G3_22P	U14	IO_95_P	43.6	
L6	DIFFIO_L6_G3_22N	V14	IO_95_N	43.8	
L6	DIFFIO_L6_G3_23P	V16	IO_96_P	28.4	
L6	DIFFIO_L6_G3_23N	V17	IO_96_N	28.0	
L6	SIO_L6_01	U17		12.7	
L7	SIO_L7_00	AB22		38.7	
L7	DIFFIO_L7_G0_00P	AE25	IO_97_P	99.0	BANKL7_G0_DQS
L7	DIFFIO_L7_G0_00N	AE26	IO_97_N	98.4	
L7	DIFFIO_L7_G0_01P	AC22	IO_98_P	53.2	
L7	DIFFIO_L7_G0_01N	AC23	IO_98_N	53.5	
L7	DIFFIO_L7_G0_02P_DQS	AF24	IO_99_P	90.9	
L7	DIFFIO_L7_G0_02N_DQS	AF25	IO_99_N	91.4	
L7	DIFFIO_L7_G0_03P	AD25	IO_100_P	71.9	
L7	DIFFIO_L7_G0_03N	AD26	IO_100_N	72.4	
L7	DIFFIO_L7_G0_04P	AE23	IO_101_P	73.3	
L7	DIFFIO_L7_G0_04N	AF23	IO_101_N	73.1	
L7	DIFFIO_L7_G0_05P	AD23	IO_102_P	61.0	
L7	DIFFIO_L7_G0_05N_VREF	AD24	IO_102_N	61.5	
L7	DIFFIO_L7_G1_06P	AD21	IO_103_P	63.3	BANKL7_G1_DQS
L7	DIFFIO_L7_G1_06N	AE21	IO_103_N	63.3	
L7	DIFFIO_L7_G1_07P	AF19	IO_104_P	63.1	
L7	DIFFIO_L7_G1_07N	AF20	IO_104_N	62.9	
L7	DIFFIO_L7_G1_08P_DQS	AE22	IO_105_P	73.2	
L7	DIFFIO_L7_G1_08N_DQS	AF22	IO_105_N	73.3	
L7	DIFFIO_L7_G1_09P	AD20	IO_106_P	49.0	
L7	DIFFIO_L7_G1_09N	AE20	IO_106_N	49.6	
L7	DIFFIO_L7_G1_10P_GSCLK	AB21	IO_107_P	44.0	
L7	DIFFIO_L7_G1_10N_GSCLK	AC21	IO_107_N	44.4	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L7	DIFFIO_L7_G1_11P_GMCLK	AA20	IO_108_P	32.9	
L7	DIFFIO_L7_G1_11N_GMCLK	AB20	IO_108_N	33.2	
L7	DIFFIO_L7_G2_12P_GMCLK	AA19	IO_109_P	42.6	BANKL7_G2_DQS
L7	DIFFIO_L7_G2_12N_GMCLK	AB19	IO_109_N	43.0	
L7	DIFFIO_L7_G2_13P_GSCLK	AC19	IO_110_P	41.9	
L7	DIFFIO_L7_G2_13N_GSCLK	AD19	IO_110_N	42.3	
L7	DIFFIO_L7_G2_14P_DQS	AC18	IO_111_P	56.1	
L7	DIFFIO_L7_G2_14N_DQS	AD18	IO_111_N	55.8	
L7	DIFFIO_L7_G2_15P	AE18	IO_112_P	53.4	
L7	DIFFIO_L7_G2_15N	AF18	IO_112_N	53.7	
L7	DIFFIO_L7_G2_16P	Y18	IO_113_P	50.2	
L7	DIFFIO_L7_G2_16N	AA18	IO_113_N	49.7	
L7	DIFFIO_L7_G2_17P	AE17	IO_114_P	52.1	
L7	DIFFIO_L7_G2_17N	AF17	IO_114_N	52.5	
L7	DIFFIO_L7_G3_18P	AA17	IO_115_P	43.2	BANKL7_G3_DQS
L7	DIFFIO_L7_G3_18N_VREF	AB17	IO_115_N	43.4	
L7	DIFFIO_L7_G3_19P	AC17	IO_116_P	39.4	
L7	DIFFIO_L7_G3_19N	AD17	IO_116_N	39.8	
L7	DIFFIO_L7_G3_20P_DQS	Y16	IO_117_P	43.2	
L7	DIFFIO_L7_G3_20N_DQS	Y17	IO_117_N	43.6	
L7	DIFFIO_L7_G3_21P	AB16	IO_118_P	35.6	
L7	DIFFIO_L7_G3_21N	AC16	IO_118_N	35.7	
L7	DIFFIO_L7_G3_22P	Y15	IO_119_P	42.2	
L7	DIFFIO_L7_G3_22N	AA15	IO_119_N	42.8	
L7	DIFFIO_L7_G3_23P	W14	IO_120_P	42.3	
L7	DIFFIO_L7_G3_23N	W15	IO_120_N	42.1	
L7	SIO_L7_01	W16		24.0	
R4	SIO_R4_00	J8		5.6	
R4	DIFFIO_R4_G0_00P_VAA4P	E6	IO_121_P	52.4	BANKR4_G0_DQS
R4	DIFFIO_R4_G0_00N_VAA4N	D6	IO_121_N	53.0	
R4	DIFFIO_R4_G0_01P_VAA6P	H8	IO_122_P	26.3	
R4	DIFFIO_R4_G0_01N_VAA6N	G8	IO_122_N	26.7	
R4	DIFFIO_R4_G0_02P_DQS_VAA11P	H7	IO_123_P	34.1	
R4	DIFFIO_R4_G0_02N_DQS_VAA11N	G7	IO_123_N	34.4	
R4	DIFFIO_R4_G0_03P	F8	IO_124_P	32.3	
R4	DIFFIO_R4_G0_03N	F7	IO_124_N	32.7	
R4	DIFFIO_R4_G0_04P_VAA12P	H6	IO_125_P	37.7	
R4	DIFFIO_R4_G0_04N_VAA12N	G6	IO_125_N	38.3	
R4	DIFFIO_R4_G0_05P	H9	IO_126_P	56.1	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R4	DIFFIO_R4_G0_05N_VREF	G9	IO_126_N	56.6	
R4	DIFFIO_R4_G1_06P_VAA13P	J6	IO_127_P	32.0	BANKR4_G1_DQS
R4	DIFFIO_R4_G1_06N_VAA13N	J5	IO_127_N	32.1	
R4	DIFFIO_R4_G1_07P_VAA14P	L8	IO_128_P	23.1	
R4	DIFFIO_R4_G1_07N_VAA14N	K8	IO_128_N	22.7	
R4	DIFFIO_R4_G1_08P_DQS_VAA15P	J4	IO_129_P	38.3	
R4	DIFFIO_R4_G1_08N_DQS_VAA15N	H4	IO_129_N	38.5	
R4	DIFFIO_R4_G1_09P_VAA0P	K7	IO_130_P	19.9	
R4	DIFFIO_R4_G1_09N_VAA0N	K6	IO_130_N	20.3	
R4	DIFFIO_R4_G1_10P_GSCLK	G4	IO_131_P	58.6	
R4	DIFFIO_R4_G1_10N_GSCLK	F4	IO_131_N	59.1	
R4	DIFFIO_R4_G1_11P_GMCLK	G5	IO_132_P	41.0	
R4	DIFFIO_R4_G1_11N_GMCLK	F5	IO_132_N	41.4	
R4	DIFFIO_R4_G2_12P_GMCLK	E5	IO_133_P	80.8	BANKR4_G2_DQS
R4	DIFFIO_R4_G2_12N_GMCLK	D5	IO_133_N	81.3	
R4	DIFFIO_R4_G2_13P_GSCLK	D4	IO_134_P	61.6	
R4	DIFFIO_R4_G2_13N_GSCLK	C4	IO_134_N	61.5	
R4	DIFFIO_R4_G2_14P_DQS	B5	IO_135_P	97.2	
R4	DIFFIO_R4_G2_14N_DQS	A5	IO_135_N	97.8	
R4	DIFFIO_R4_G2_15P	B4	IO_136_P	75.8	
R4	DIFFIO_R4_G2_15N	A4	IO_136_N	76.3	
R4	DIFFIO_R4_G2_16P	D3	IO_137_P	84.2	
R4	DIFFIO_R4_G2_16N	C3	IO_137_N	84.6	
R4	DIFFIO_R4_G2_17P	F3	IO_138_P	55.2	
R4	DIFFIO_R4_G2_17N	E3	IO_138_N	55.7	
R4	DIFFIO_R4_G3_18P	C2	IO_139_P	96.9	BANKR4_G3_DQS
R4	DIFFIO_R4_G3_18N_VREF	B2	IO_139_N	97.1	
R4	DIFFIO_R4_G3_19P	A3	IO_140_P	80.4	
R4	DIFFIO_R4_G3_19N	A2	IO_140_N	80.7	
R4	DIFFIO_R4_G3_20P_DQS	C1	IO_141_P	100.2	
R4	DIFFIO_R4_G3_20N_DQS	B1	IO_141_N	99.8	
R4	DIFFIO_R4_G3_21P	F2	IO_142_P	60.6	
R4	DIFFIO_R4_G3_21N	E2	IO_142_N	60.8	
R4	DIFFIO_R4_G3_22P	E1	IO_143_P	88.5	
R4	DIFFIO_R4_G3_22N	D1	IO_143_N	88.8	
R4	DIFFIO_R4_G3_23P	G2	IO_144_P	54.7	
R4	DIFFIO_R4_G3_23N	G1	IO_144_N	54.9	
R4	SIO_R4_01	H3		60.4	
R5	SIO_R5_00	N8		5.1	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R5	DIFFIO_R5_G0_00P	K3	IO_145_P	51.8	BANKR5_G0_DQS
R5	DIFFIO_R5_G0_00N	J3	IO_145_N	51.8	
R5	DIFFIO_R5_G0_01P	M7	IO_146_P	32.7	
R5	DIFFIO_R5_G0_01N	L7	IO_146_N	32.3	
R5	DIFFIO_R5_G0_02P_DQS	M4	IO_147_P	36.7	
R5	DIFFIO_R5_G0_02N_DQS	L4	IO_147_N	37.2	
R5	DIFFIO_R5_G0_03P	L5	IO_148_P	30.5	
R5	DIFFIO_R5_G0_03N	K5	IO_148_N	30.9	
R5	DIFFIO_R5_G0_04P	N7	IO_149_P	17.6	
R5	DIFFIO_R5_G0_04N	N6	IO_149_N	17.8	
R5	DIFFIO_R5_G0_05P	M6	IO_150_P	20.3	
R5	DIFFIO_R5_G0_05N_VREF	M5	IO_150_N	20.6	
R5	DIFFIO_R5_G1_06P	K1	IO_151_P	77.6	BANKR5_G1_DQS
R5	DIFFIO_R5_G1_06N	J1	IO_151_N	77.9	
R5	DIFFIO_R5_G1_07P	L3	IO_152_P	44.9	
R5	DIFFIO_R5_G1_07N	K2	IO_152_N	45.4	
R5	DIFFIO_R5_G1_08P_DQS	N1	IO_153_P	73.3	
R5	DIFFIO_R5_G1_08N_DQS	M1	IO_153_N	72.7	
R5	DIFFIO_R5_G1_09P	H2	IO_154_P	60.4	
R5	DIFFIO_R5_G1_09N	H1	IO_154_N	60.6	
R5	DIFFIO_R5_G1_10P_GSCLK	M2	IO_155_P	59.9	
R5	DIFFIO_R5_G1_10N_GSCLK	L2	IO_155_N	60.1	
R5	DIFFIO_R5_G1_11P_GMCLK	N3	IO_156_P	40.2	
R5	DIFFIO_R5_G1_11N_GMCLK	N2	IO_156_N	40.4	
R5	DIFFIO_R5_G2_12P_GMCLK	R3	IO_157_P	51.2	BANKR5_G2_DQS
R5	DIFFIO_R5_G2_12N_GMCLK	P3	IO_157_N	50.9	
R5	DIFFIO_R5_G2_13P_GSCLK	P4	IO_158_P	32.1	
R5	DIFFIO_R5_G2_13N_GSCLK	N4	IO_158_N	31.8	
R5	DIFFIO_R5_G2_14P_DQS	R1	IO_159_P	71.3	
R5	DIFFIO_R5_G2_14N_DQS	P1	IO_159_N	70.8	
R5	DIFFIO_R5_G2_15P	T4	IO_160_P	45.6	
R5	DIFFIO_R5_G2_15N	T3	IO_160_N	45.8	
R5	DIFFIO_R5_G2_16P	T2	IO_161_P	61.7	
R5	DIFFIO_R5_G2_16N	R2	IO_161_N	61.6	
R5	DIFFIO_R5_G2_17P	U2	IO_162_P	54.9	
R5	DIFFIO_R5_G2_17N	U1	IO_162_N	54.6	
R5	DIFFIO_R5_G3_18P	P6	IO_163_P	25.3	BANKR5_G3_DQS
R5	DIFFIO_R5_G3_18N_VREF	P5	IO_163_N	25.7	
R5	DIFFIO_R5_G3_19P	T5	IO_164_P	31.3	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R5	DIFFIO_R5_G3_19N	R5	IO_164_N	30.8	
R5	DIFFIO_R5_G3_20P_DQS	U6	IO_165_P	51.9	
R5	DIFFIO_R5_G3_20N_DQS	U5	IO_165_N	52.0	
R5	DIFFIO_R5_G3_21P	R8	IO_166_P	44.8	
R5	DIFFIO_R5_G3_21N	P8	IO_166_N	44.6	
R5	DIFFIO_R5_G3_22P	R7	IO_167_P	18.7	
R5	DIFFIO_R5_G3_22N	R6	IO_167_N	19.3	
R5	DIFFIO_R5_G3_23P	T8	IO_168_P	35.8	
R5	DIFFIO_R5_G3_23N	T7	IO_168_N	35.4	
R5	SIO_R5_01	U4		32.9	
R6	SIO_R6_00	V4		35.4	
R6	DIFFIO_R6_G0_00P	V1	IO_169_P	67.2	
R6	DIFFIO_R6_G0_00N	W1	IO_169_N	67.5	
R6	DIFFIO_R6_G0_01P	W5	IO_170_P	45.3	
R6	DIFFIO_R6_G0_01N	W4	IO_170_N	45.2	
R6	DIFFIO_R6_G0_02P_DQS	V3	IO_171_P	67.3	
R6	DIFFIO_R6_G0_02N_DQS	V2	IO_171_N	66.8	BANKR6_G0_DQS
R6	DIFFIO_R6_G0_03P	V6	IO_172_P	39.5	
R6	DIFFIO_R6_G0_03N	W6	IO_172_N	39.6	
R6	DIFFIO_R6_G0_04P	W3	IO_173_P	57.2	
R6	DIFFIO_R6_G0_04N	Y3	IO_173_N	57.6	
R6	DIFFIO_R6_G0_05P	U7	IO_174_P	42.9	
R6	DIFFIO_R6_G0_05N_VREF	V7	IO_174_N	43.4	
R6	DIFFIO_R6_G1_06P	AB1	IO_175_P	82.3	
R6	DIFFIO_R6_G1_06N	AC1	IO_175_N	81.8	
R6	DIFFIO_R6_G1_07P	Y2	IO_176_P	59.1	
R6	DIFFIO_R6_G1_07N	Y1	IO_176_N	59.5	
R6	DIFFIO_R6_G1_08P_DQS	AD1	IO_177_P	92.4	
R6	DIFFIO_R6_G1_08N_DQS	AE1	IO_177_N	92.1	BANKR6_G1_DQS
R6	DIFFIO_R6_G1_09P	AE2	IO_178_P	85.1	
R6	DIFFIO_R6_G1_09N	AF2	IO_178_N	85.4	
R6	DIFFIO_R6_G1_10P_GSCLK	AB2	IO_179_P	75.2	
R6	DIFFIO_R6_G1_10N_GSCLK	AC2	IO_179_N	75.3	
R6	DIFFIO_R6_G1_11P_GMCLK	AA3	IO_180_P	56.3	
R6	DIFFIO_R6_G1_11N_GMCLK	AA2	IO_180_N	56.6	
R6	DIFFIO_R6_G2_12P_GMCLK	AA4	IO_181_P	57.7	
R6	DIFFIO_R6_G2_12N_GMCLK	AB4	IO_181_N	58.0	BANKR6_G2_DQS
R6	DIFFIO_R6_G2_13P_GSCLK	AC3	IO_182_P	61.8	
R6	DIFFIO_R6_G2_13N_GSCLK	AD3	IO_182_N	62.2	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R6	DIFFIO_R6_G2_14P_DQS	AD5	IO_183_P	75.2	
R6	DIFFIO_R6_G2_14N_DQS	AE5	IO_183_N	75.0	
R6	DIFFIO_R6_G2_15P	AE3	IO_184_P	72.2	
R6	DIFFIO_R6_G2_15N	AF3	IO_184_N	72.6	
R6	DIFFIO_R6_G2_16P	AF5	IO_185_P	86.4	
R6	DIFFIO_R6_G2_16N	AF4	IO_185_N	86.7	
R6	DIFFIO_R6_G2_17P	AC4	IO_186_P	57.5	
R6	DIFFIO_R6_G2_17N	AD4	IO_186_N	58.0	
R6	DIFFIO_R6_G3_18P	Y7	IO_187_P	41.0	BANKR6_G3_DQS
R6	DIFFIO_R6_G3_18N_VREF	AA7	IO_187_N	40.6	
R6	DIFFIO_R6_G3_19P	Y6	IO_188_P	35.9	
R6	DIFFIO_R6_G3_19N	Y5	IO_188_N	35.8	
R6	DIFFIO_R6_G3_20P_DQS	V8	IO_189_P	27.6	
R6	DIFFIO_R6_G3_20N_DQS	W8	IO_189_N	27.9	
R6	DIFFIO_R6_G3_21P	AA5	IO_190_P	40.0	
R6	DIFFIO_R6_G3_21N	AB5	IO_190_N	40.0	
R6	DIFFIO_R6_G3_22P	Y8	IO_191_P	35.9	
R6	DIFFIO_R6_G3_22N	AA8	IO_191_N	36.1	
R6	DIFFIO_R6_G3_23P	AB6	IO_192_P	43.2	
R6	DIFFIO_R6_G3_23N	AC6	IO_192_N	43.2	
R6	SIO_R6_01	V9		13.8	
	INIT_FLAG_N	V11		58.9	
	CFG_DONE	W10		70.7	
	RSTN	AE16		78.4	
	CFG_CLK	H13		115.9	
	TCK	H12		101.9	
	TMS	H11		91.2	
	TDI	H10		97.5	
	TDO	J10		94.9	
	MODE_0	AB7		101.0	
	MODE_1	Y9		81.0	
	MODE_2	W9		73.4	
	SCBV	AB15		57.3	
	VAADC_N	P11	IO_193_N	51.9	
	VAADC_P	N12	IO_193_P	51.9	
	VCCADC	M12			
	VREFADC_N	N11	IO_194_N	53.4	
	VREFADC_P	P12	IO_194_P	53.1	
	VSSADC	M11			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	TSDN	R11	IO_195_N	58.4	
	TSDP	R12	IO_195_P	58.7	
	VCCB	G14		56.4	
	VCCIOCFG	W11		23.2	
	VCCIOCFG	Y14		23.2	
	HSSTRX0N_QL3	A11	IO_196_N	52.3	
	HSSTRX0P_QL3	B11	IO_196_P	52.0	
	HSSTRX1N_QL3	C14	IO_197_N	44.1	
	HSSTRX1P_QL3	D14	IO_197_P	44.0	
	HSSTRX2N_QL3	A13	IO_198_N	57.1	
	HSSTRX2P_QL3	B13	IO_198_P	57.0	
	HSSTRX3N_QL3	C12	IO_199_N	69.7	
	HSSTRX3P_QL3	D12	IO_199_P	69.9	
	HSSTTX0N_QL3	A7	IO_200_N	89.5	
	HSSTTX0P_QL3	B7	IO_200_P	89.7	
	HSSTTX1N_QL3	C8	IO_201_N	96.1	
	HSSTTX1P_QL3	D8	IO_201_P	95.9	
	HSSTTX2N_QL3	A9	IO_202_N	78.0	
	HSSTTX2P_QL3	B9	IO_202_P	78.0	
	HSSTTX3N_QL3	C10	IO_203_N	65.1	
	HSSTTX3P_QL3	D10	IO_203_P	65.4	
	HSSTREFCLK0P_QL3	F11	IO_204_P	41.7	
	HSSTREFCLK0N_QL3	E11	IO_204_N	42.0	
	HSSTREFCLK1N_QL3	E13	IO_205_N	31.3	
	HSSTREFCLK1P_QL3	F13	IO_205_P	31.2	
	HSSTRREF_QL3	A15		51.1	
	HSSTRX0N_QL7	AD12	IO_206_N	111.2	
	HSSTRX0P_QL7	AC12	IO_206_P	111.3	
	HSSTRX1N_QL7	AF13	IO_207_N	68.9	
	HSSTRX1P_QL7	AE13	IO_207_P	68.7	
	HSSTRX2N_QL7	AD14	IO_208_N	43.2	
	HSSTRX2P_QL7	AC14	IO_208_P	43.0	
	HSSTRX3N_QL7	AF11	IO_209_N	52.5	
	HSSTRX3P_QL7	AE11	IO_209_P	52.7	
	HSSTTX0N_QL7	AD10	IO_210_N	122.8	
	HSSTTX0P_QL7	AC10	IO_210_P	122.8	
	HSSTTX1N_QL7	AF9	IO_211_N	88.6	
	HSSTTX1P_QL7	AE9	IO_211_P	88.4	
	HSSTTX2N_QL7	AD8	IO_212_N	64.1	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	HSSTTX2P_QL7	AC8	IO_212_P	63.9	
	HSSTTX3N_QL7	AF7	IO_213_N	89.1	
	HSSTTX3P_QL7	AE7	IO_213_P	89.4	
	HSSTREFCLK0P_QL7	AA13	IO_214_P	32.2	
	HSSTREFCLK0N_QL7	AB13	IO_214_N	32.5	
	HSSTREFCLK1N_QL7	AB11	IO_215_N	52.4	
	HSSTREFCLK1P_QL7	AA11	IO_215_P	52.3	
	HSSTRREF_QL7	AF15		56.8	
	HSSTAVCC_G3	D11			
	HSSTAVCC_G3	D13			
	HSSTAVCC_G3	D9			
	HSSTAVCC_G3	F10			
	HSSTAVCC_G3	F12			
	HSSTAVCCPLL_G3	B10			
	HSSTAVCCPLL_G3	B12			
	HSSTAVCCPLL_G3	B14			
	HSSTAVCCPLL_G3	B8			
	HSSTAVCCPLL_G3	C15			
	HSSTAVCCPLL_G3	C7			
	HSSTAVCC_G7	AA10			
	HSSTAVCC_G7	AA12			
	HSSTAVCC_G7	AC11			
	HSSTAVCC_G7	AC13			
	HSSTAVCC_G7	AC9			
	HSSTAVCCPLL_G7	AD15			
	HSSTAVCCPLL_G7	AD7			
	HSSTAVCCPLL_G7	AE10			
	HSSTAVCCPLL_G7	AE12			
	HSSTAVCCPLL_G7	AE14			
	HSSTAVCCPLL_G7	AE8			
	VCC	J11			
	VCC	J13			
	VCC	K10			
	VCC	K12			
	VCC	L11			
	VCC	L13			
	VCC	M10			
	VCC	P10			
	VCC	T10			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCC	T12			
	VCC	U11			
	VCC	V10			
	VCC	V12			
	VCCA	J9			
	VCCA	L9			
	VCCA	N9			
	VCCA	R9			
	VCCA	U9			
	VCC_DRM	N13			
	VCC_DRM	R13			
	VCC_DRM	U13			
	VCC_DRM	W13			
	VCCIO_L3	A21			
	VCCIO_L3	B18			
	VCCIO_L3	C25			
	VCCIO_L3	D22			
	VCCIO_L3	E19			
	VCCIO_L3	F16			
	VCCIO_L4	F26			
	VCCIO_L4	G23			
	VCCIO_L4	H20			
	VCCIO_L4	J17			
	VCCIO_L4	K14			
	VCCIO_L4	M18			
	VCCIO_L5	K24			
	VCCIO_L5	L21			
	VCCIO_L5	N15			
	VCCIO_L5	N25			
	VCCIO_L5	P22			
	VCCIO_L5	R19			
	VCCIO_L6	AC25			
	VCCIO_L6	T16			
	VCCIO_L6	T26			
	VCCIO_L6	U23			
	VCCIO_L6	V20			
	VCCIO_L6	Y24			
	VCCIO_L7	AA21			
	VCCIO_L7	AB18			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCCIO_L7	AD22			
	VCCIO_L7	AE19			
	VCCIO_L7	AF26			
	VCCIO_L7	W17			
	VCCIO_R4	A1			
	VCCIO_R4	C5			
	VCCIO_R4	D2			
	VCCIO_R4	F6			
	VCCIO_R4	G3			
	VCCIO_R4	J7			
	VCCIO_R5	K4			
	VCCIO_R5	L1			
	VCCIO_R5	M8			
	VCCIO_R5	N5			
	VCCIO_R5	P2			
	VCCIO_R5	T6			
	VCCIO_R6	AA1			
	VCCIO_R6	AC5			
	VCCIO_R6	AD2			
	VCCIO_R6	U3			
	VCCIO_R6	W7			
	VCCIO_R6	Y4			
	VSS	A10			
	VSS	A12			
	VSS	A14			
	VSS	A16			
	VSS	A26			
	VSS	A6			
	VSS	A8			
	VSS	AA14			
	VSS	AA16			
	VSS	AA26			
	VSS	AA6			
	VSS	AA9			
	VSS	AB10			
	VSS	AB12			
	VSS	AB14			
	VSS	AB23			
	VSS	AB3			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	AB8			
	VSS	AB9			
	VSS	AC15			
	VSS	AC20			
	VSS	AC7			
	VSS	AD11			
	VSS	AD13			
	VSS	AD16			
	VSS	AD6			
	VSS	AD9			
	VSS	AE15			
	VSS	AE24			
	VSS	AE4			
	VSS	AE6			
	VSS	AF1			
	VSS	AF10			
	VSS	AF12			
	VSS	AF14			
	VSS	AF16			
	VSS	AF21			
	VSS	AF6			
	VSS	AF8			
	VSS	B15			
	VSS	B16			
	VSS	B23			
	VSS	B3			
	VSS	B6			
	VSS	C11			
	VSS	C13			
	VSS	C16			
	VSS	C20			
	VSS	C6			
	VSS	C9			
	VSS	D15			
	VSS	D17			
	VSS	D7			
	VSS	E10			
	VSS	E12			
	VSS	E14			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	E15			
	VSS	E24			
	VSS	E4			
	VSS	E7			
	VSS	E8			
	VSS	E9			
	VSS	F1			
	VSS	F14			
	VSS	F21			
	VSS	F9			
	VSS	G10			
	VSS	G11			
	VSS	G12			
	VSS	G13			
	VSS	G18			
	VSS	H25			
	VSS	H5			
	VSS	J12			
	VSS	J2			
	VSS	J22			
	VSS	K11			
	VSS	K13			
	VSS	K19			
	VSS	K9			
	VSS	L10			
	VSS	L12			
	VSS	L16			
	VSS	L26			
	VSS	L6			
	VSS	M13			
	VSS	M23			
	VSS	M3			
	VSS	M9			
	VSS	N10			
	VSS	N20			
	VSS	P13			
	VSS	P17			
	VSS	P7			
	VSS	P9			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	R10			
	VSS	R24			
	VSS	R4			
	VSS	T1			
	VSS	T11			
	VSS	T13			
	VSS	T21			
	VSS	T9			
	VSS	U10			
	VSS	U12			
	VSS	U18			
	VSS	U8			
	VSS	V13			
	VSS	V15			
	VSS	V25			
	VSS	V5			
	VSS	W12			
	VSS	W2			
	VSS	W22			
	VSS	Y10			
	VSS	Y11			
	VSS	Y12			
	VSS	Y13			
	VSS	Y19			

2.2.2 Thermal Resistance

Table 2-3 Thermal Resistance

θJA(℃/W) (Flow: 0m/s)	θJB(℃/W)	θJC(℃/W)	θJA(℃/W) (Flow: 1m/s)	θJA(℃/W) (Flow: 2m/s)
10.7	5.1	0.02	9.4	8.8

2.2.3 Pressure value

1. Short term pressure(within 5 minutes): 100g/ball, 676 balls, short term pressure can meet 67.6kg.
2. Long term pressure: 30g/ball, 676 balls, long term pressure can meet 20.28kg.

Disclaimer

Copyright Notice

Disclaimer

1. This document only provides information in stages and may be updated at any time based on the actual situation of the products without further notice. The Company assumes no legal responsibility for any direct or indirect losses caused by improper use of this document.
2. This document is provided "as is" without any warranties, including but not limited to warranties of merchantability, fitness for a particular purpose, non-infringement, or any other warranties mentioned in proposals, specifications, or samples. This document does not grant any explicit or implied intellectual property usage license, whether by estoppel or otherwise.
3. The Company reserves the right to modify any documents related to its series products at any time without prior notice.