PG2L200H_FBB484

(PK04009, V1.0)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	05.08.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Full Spelling
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

PG2L200H_FBB484 uses a Bare Die Flip chip BGA type of packaging. Package size: 23x23mm; Number of balls: 484; Ball pitch: 1.0mm; Maximum package thickness: 2.310mm.

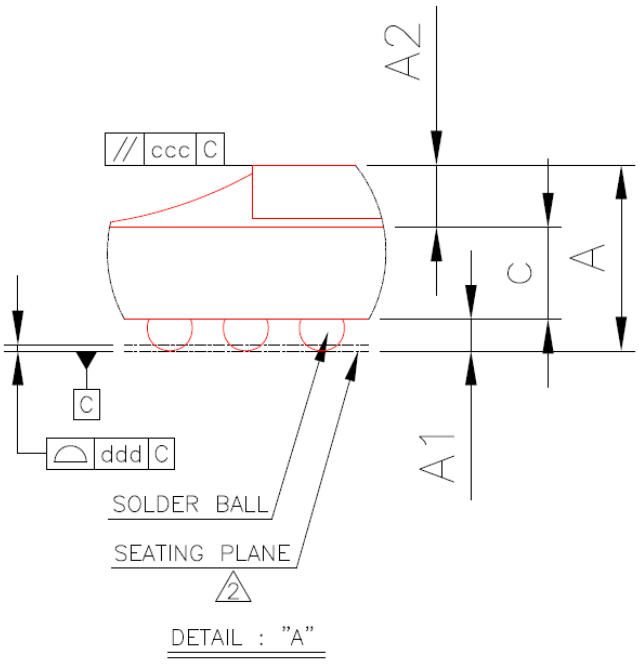
Chapter 2 Package Dimension and Pin

2.1 Package Dimension

Figure 2-1 Dimensional Values

Unit: millimeter

Dimension Symbol	Value			Dimension Symbol	Value		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	2.146	2.310	2.474	e	-	1.00	-
A1	0.40	0.50	0.60	b	0.50	0.60	0.70
A2	0.584	0.634	0.684	aaa	-	0.20	-
C	1.056	1.176	1.296	ccc	-	0.20	-
D	22.90	23.00	23.10	ddd	-	0.15	-
E	22.90	23.00	23.10	eee	-	0.25	-
D1	-	21.00	-	fff	-	0.10	-
E1	-	21.00	-	Ball Diam	-	0.60	-



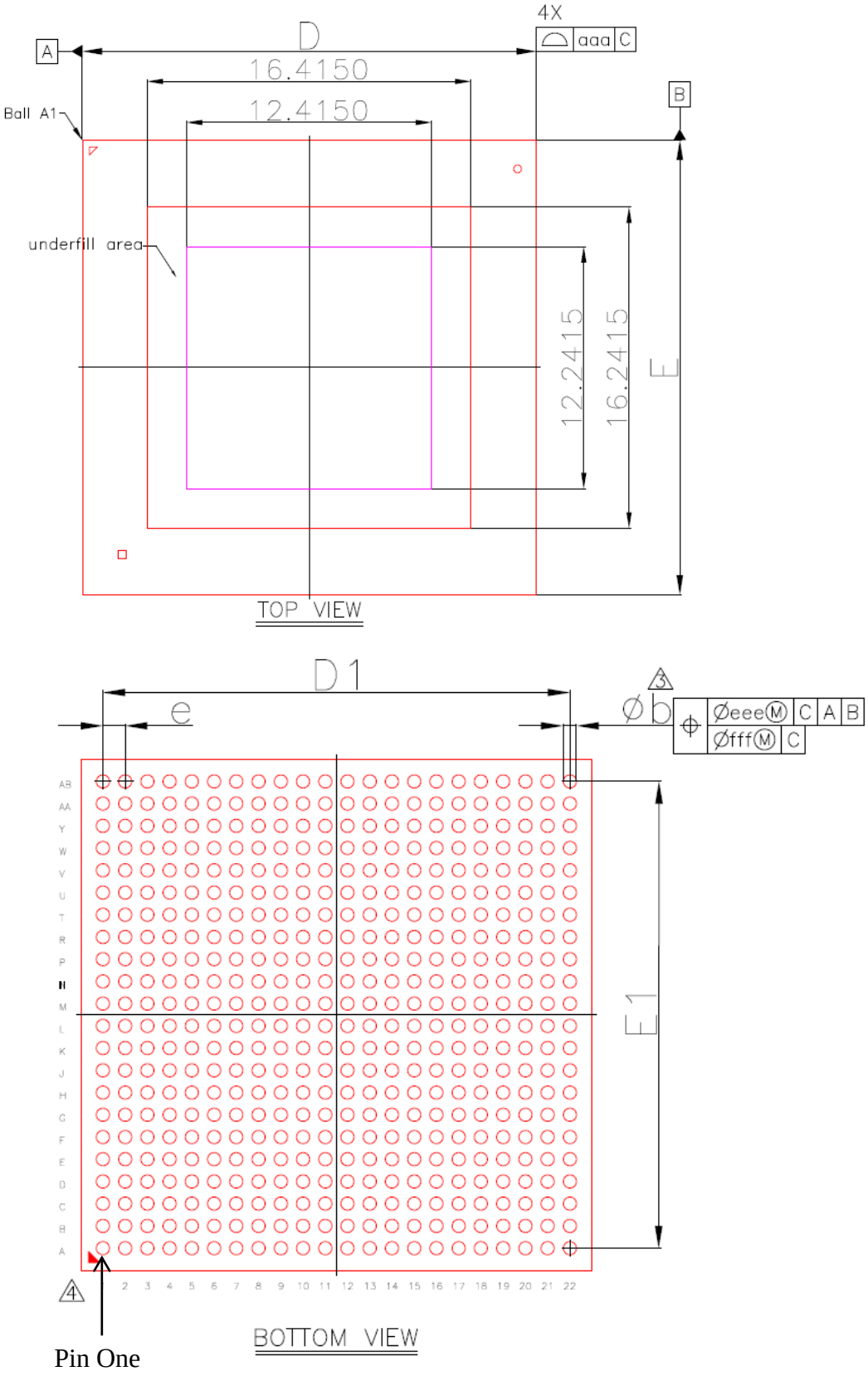


Figure 2-2 Package Outline Dimension (POD)

2.2 Pin Definitions

PG2L200H _ FBB484 has 285 user IOs.

Table 2-1 Product Pin Definitions

PIN Name	PIN Type	PIN Direction	PIN Description
General PIN			
DIFFIO_XX_GY_NN[P,N]	General	Input/Output	General pin; (1) "DIFFIO" indicates the pin supports differential input/output and can be used for transmitting and receiving LVDS signals; (2) " XX " indicates bank numbers, which can be L3, L4, L5, L6, R4, R5; (3) " G " indicates belonging to a memory group; (4) " Y " indicates the group number in a bank, each of which contains four groups; (5) "NN" indicates the sequence number of programmable IO pairs in a bank, increasing from 0, a bank contains 24 difference pairs; (6) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end; During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri-state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.
SIO_XX_NN	General	Input/Output	General pin; (1) " SIO " indicates the pin only supports single ended input/output; (2) " XX " indicates bank numbers, which can be L3, L4, L5, L6, R4, R5; (3) "NN" indicates the sequence number of programmable IO in a bank, increasing from 0, a bank contains 2 single ended IOs; During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri- state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.
Configuration PIN			
INIT_FLAG_N	Dedicated	Bidirectional (open-drain)	Initialization and configuration status dedicated pin: When it is low, it indicates that the FPGA is being initialized (clear configuration memory) or a configuration error has occurred. The pin has an internal weak pull-up resistor that

PIN Name	PIN Type	PIN Direction	PIN Description
			is enabled during configuration; When the FPGA powers up completion, the pin is driven to low level. Once the FPGA completes initialization, the pin is released. During the power up and initialization process, this pin can accept an external low level input to delay the configuration process. When the FPGA detects high level input on this pin after initialization, the FPGA starts the configuration process.During configuration, this pin serves as an output for the configuration error indication state, low level indicates that an error occurred. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. After the configuration is complete, user can configure weak pull-up or float state for this pin.
CFG_DONE	Dedicated	Bidirectional (open-drain)	Dedicated configuration status pin, built in weak pull-up resistor about 10K. Output as the configuration completion indicator, high level indicates that the configuration is complete. This pin is an open-drain output. When the FPGA powers up completion, the pin is driven to low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released. After the configuration is complete, the pin can be driven externally to low level, Once the internal start-up timing finds that the external DONE pin is low, the internal start-up circuit stops until the external pin is high. After the configuration is complete, user can configure weak pull-up or float state for this pin.
RSTN	Dedicated	Input	Dedicated configuration reset pin, built in weak pull-up resistor and always effective. For restarting configuration logic and configuration memory, active-low. When this pin is low, the FPGA configuration memory is emptied and a new configuration process begins. The configuration logic reset begins with the falling edge of the pin, and the configuration process begins with the rising edge of the pin. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. Keeping this pin low during power up does not put the FPGA configuration logic in a reset state. After the configuration is complete, user can configure weak pull-up or float state for this pin.
CFG_CLK	Dedicated	Input/Output	Configuration clock pin. Except for the JTAG configuration mode, the configuration process of the FPGA is synchronize by this clock in other modes. In the slave serial and slave parallel onfiguration modes, the pin serves as a clock input to obtain configuration data from external sources.

PIN Name	PIN Type	PIN Direction	PIN Description
			In the master SPI configuration mode, the pin serves as a clock output to obtain configuration data from external sources and an external pull-up resistor of 1K is required. When the clock is not needed (such as in the JTAG mode), this pin is in the High-Z state. After the configuration is complete, user can configure weak pull-up or float state for this pin.
TCK	Dedicated	Input	Test clock input pin compliant with IEEE STD 1149.1 and provides a clock for the JTAG chain of the FPGA. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TMS	Dedicated	Input	Dedicated JTAG test mode selection input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDI	Dedicated	Input	Dedicated JTAG test data input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDO	Dedicated	Output	Dedicated JTAG test data output pin Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
MODE_2	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_1	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_0	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
SCBV	Dedicated	Input	The pin is always effective on BANKCFG, but only on BANK which the multiplexing configuration pins is located during configuration. When the voltage of VCCIOCFG is 2.5V or 3.3V, the pin must be connected to high level and can be connected directly to the VCCIOCFG. When the voltage of VCCIOCFG is 1.8V or lower, the pin must be connected to low level and can be connected directly to the ground. Note: The pin must be used in conjunction with the software, and the SCBV selection in the bitstream setting must be consistent with the hardware setting. For details about the SCBV pin pull-up/pull-down level corresponds to the configured BANK power,

PIN Name	PIN Type	PIN Direction	PIN Description
			see “UG040012_Logos2 Family Hardware Design Guide”.
FCS_N	Multiplexed	Output	Multi-function configuration pin, used for the Master SPI configuration mode. (1) In the Master SPI X1, X2 and X4 modes, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
MOSI_D0	Multiplexed	Input/Output	Multi-function configuration data pin. (1) “MOSI”, in the master SPI X1 mode, this pin used for serial data output and connects to the data input pin of the external SPI flash (such as DQ0,D, SI,IO0, etc). After the command and address are sent to the external SPI flash, the pin output high-Z or weak pull-up, depending on the state of the IO_STATUS_C pin. (2) In the master SPI X2, X4 and X8 modes, the pin is bidirectional data port, as command and address output to the external SPI flash. Receive the lowest bit data from the external SPI flash. The pin connects to the bidirectional data pin of the external SPI flash (such as DQ0,D,SI,IO0, etc). (3) “D0” in the slave parallel mode, this pin serves as the D[0] bit of the data bus. (4) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (5) After the configuration is complete, the pin serves as a general pin.
MISO_D1_DI	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X1 mode, “MISO” serves as data input and connects to the data output pin of the external SPI flash (such as DQ1,Q,SO,IO1, etc). (2) In the master SPI X2, X4 and X8 modes, “D1” connects to the second serial data output pin of the external SPI flash (such as DQ1,Q,SO,IO1, etc). (3) In the slave parallel mode, this pin serves as the D[1] bit of the data bus. (4) In the slave serial mode, “D1” serves as data input pin. (5) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. In the other configuration modes(such as JTAG), the state on the pin is ignored (6) After the configuration is complete, the pin serves as a general pin.
D[2, 3]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X4 and X8 modes, serve as

PIN Name	PIN Type	PIN Direction	PIN Description
			data input and connects to the data output pin of the external SPI flash. “D2” connects to the third bit data output pin of the external SPI flash(such as DQ2,W#,WP#,IO2, etc). “D3” connects to the fourth bit data output pin of the external SPI flash(such as DQ3,HOLD#, IO3, etc). These pins should be connected to VCCIO via an external weak pull-up resistor of 4.7K. (2) In the slave parallel mode, these pins serve as the D[3:2] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[4, 5, 6, 7]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X8 mode, connect to the second flash in the same way as D[3:0]. (2) In the slave parallel mode, these pins serve as the D[7:4] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[8,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1)In the slave parallel X16 and X32 modes, serve as the D[15:8] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
D[16,…,31]_A[0,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the slave parallel X32 mode, serve as the D[31:16] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
A[16,…,28]	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (2) After the configuration is complete, these pins serve as general pins.
CS_N	Multiplexed	Input	Multi-function configuration pin. For chip select input. Active low. (1) When it is low level, this pin enables the slave parallel mode configuration interface. In the slave parallel configuration mode, the external controller can select the slave parallel bus of the FPGA by controlling this pin. Or this pin connected to the previous FPGA CSO_DOUT pin in the slave parallel configuration chain. (2) In the other configuration modes or in

PIN Name	PIN Type	PIN Direction	PIN Description
			initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
RWSEL	Multiplexed	Input	Multi-function configuration pin. For selecting the read/write input in the slave parallel configuration mode (high for read and low for write). (1) When it is high level, the slave parallel configuration mode reads data from the data bus. (2) When it is low level, the slave parallel configuration mode writes data to the data bus. (3) Read and write can be switched only when CS_N is high level. (4) After the configuration is complete, the pin serves as a general pin. (5) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.
CSO_DOUT	Multiplexed	Output	Multi-function configuration pin. Needed for cascade. (1) In the master SPI X1 mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2) In the slave serial configuration mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (3) In the slave parallel cascade configuration mode, this pin serves as a chip select signal open-drain output, connects to downstream chip CS_N pin and should be connected to VCCIO via an external pull-up resistor of 330Ω. (4) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.
VS[0, 1]	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (2)After the configuration is complete, these pins as general pins.
IO_STATUS_C	Multiplexed	Input	Multi-function configuration pin, used for controlling whether the weak pull-up resistors for all general pins are enabled during the configuration process. (1) When it is set to "0", the internal pull-up resistors for all general pins are enabled. (2) When it is set to "1", the internal pull-up resistors for all general pins are disabled. (3)It is recommended that the pin connects to VCCIO via an external weak pull-up resistor. (4)The pin can connect to VCCIO or VSS, either directly or via an external resistor of no more than

PIN Name	PIN Type	PIN Direction	PIN Description
			1K. (5) This pin must not be left floating before or during configuration.
ECCLKIN	Multiplexed	Input	The external clock input for the Master configuration mode, which is an optional external clock input to the configuration logic. (1) In the master SPI mode, the FPGA can select this clock input as the configuration clock for the configuration logic. This clock can be divided (Depends on the settings in the bitstream) and output from the CFG_CLK pin. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.
BFOE_N	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2)After the configuration is complete, the pin as a general pin.
BFWE_FCS2_N	Multiplexed	Output	Multi-function configuration pin, used for the master SPI X8 configuration mode. (1) In the Master SPI X8 mode, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin as a general pin.
BADRVO_N	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2)After the configuration is complete, the pin as a general pin.
Clock PIN			
GMCLK	Multiplexed	Input	Multiplexing global multi-regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL, PPLL, and also drive the multi-regional clock buffer. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. When these pins serve as single regional clock sources, they are able to drive all the IO clock buffers and regional clock buffers of the BANK.
GSCLK	Multiplexed	Input	Multiplexing global single regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL and PPLL. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair

PIN Name	PIN Type	PIN Direction	PIN Description
			needs to be connected. They are able to drive all the IO clock buffers and regional clock buffers of the BANK.
Memory Interface PIN			
DQS	Multiplexed	Input/Output	DDR DQS PIN, each memory group contains two pins.
Reference PIN			
VREF	Multiplexed	N/A	Input reference voltage pins. When not used as external reference voltage pins, these pins serve as general pins,
Power/ Ground PIN			
VCC	Dedicated	N/A	Core logic power, 1.0V. Power supply for core logic.
VCC_DRM	Dedicated	N/A	DRM power, 1.0V. Dedicated power supply for DRM. If the voltage is the same as VCC, it can be connected to VCC at the board.
VCCA	Dedicated	N/A	Analog power, 1.8V. Power supply for internal analog circuit.
VCCIO[L3, L4, L5, L6, R4, R5, CFG]	dedicated	N/A	IO BANK power.
VCCB	Dedicated	N/A	Key memory backup battery power supply voltage. When the key function is not used, the pin needs to be connected to the VCCA or ground.
VSS	Dedicated	N/A	Ground
ADC PIN			
VCCADC	Dedicated	N/A	ADC analog power, 1.8V. Power supply for ADC analog circuit.
VSSADC	Dedicated	N/A	GND relative to VCCADC
VAADC_P	Dedicated	Input	ADC dedicated analog differential input (Positive).
VAADC_N	Dedicated	Input	ADC dedicated analog differential input (Negative).
VREFADC_P	Dedicated	N/A	1.255V ADC reference voltage pin.
VREFADC_N	Dedicated	N/A	ADC reference voltage ground.
VAA[0,..,15]P,VAA[0,..,15]N	Multiplexed	Input	ADC differential analog input signals.
TSDP	Dedicated	N/A	Positive pin of the temperature sensor diode. When not used temperature diode, the pin needs to be connected to the VSS. When temperature sensor diode is to be used, then appropriate external temperature monitoring chip is required.
TSDN	Dedicated	N/A	Negative pin of the temperature sensor diode.
HSST PIN			
HSSTAVCC_G3	Dedicated	N/A	1.0V analog power pin, power supply for HSST internal transmits and receives circuit.
HSSTAVCCPLL_ G3	Dedicated	N/A	1.2V analog power pin, power supply for HSST internal PLL.
HSSTRREF_QL3	Dedicated	Input	Calibration resistance input pin of the terminal resistance calibration circuit.
HSSTREFCLK[0,1]P_QL3	Dedicated	Input	Positive end of differential clock input pin, provide a reference clock to HSST.

PIN Name	PIN Type	PIN Direction	PIN Description
HSSTREFCLK[0,1]N_QL3	Dedicated	Input	Negative end of differential clock input pin, provide a reference clock to HSST.
HSSTTX[0,1,2,3][P,N]_QL3	Dedicated	Output	Channel differential outputs of HSST. Each HSST has 4 pairs.
HSSTRX[0,1,2,3][P,N]_QL3	Dedicated	Input	Channel differential inputs of HSST. Each HSST has 4 pairs.

2.2.1 Pin Name List

Table 2-2 Pin Name List

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L3	SIO_L3_00	F15		20.7	
L3	DIFFIO_L3_G0_00P	F13	IO_1_P	23.8	BANKL3_G0_DQS
L3	DIFFIO_L3_G0_00N	F14	IO_1_N	24.1	
L3	DIFFIO_L3_G0_01P	F16	IO_2_P	9.6	
L3	DIFFIO_L3_G0_01N	E17	IO_2_N	9.6	
L3	DIFFIO_L3_G0_02P_DQS	C14	IO_3_P	30.7	
L3	DIFFIO_L3_G0_02N_DQS	C15	IO_3_N	31.3	
L3	DIFFIO_L3_G0_03P	E13	IO_4_P	33.2	
L3	DIFFIO_L3_G0_03N	E14	IO_4_N	33.5	
L3	DIFFIO_L3_G0_04P	E16	IO_5_P	18.8	
L3	DIFFIO_L3_G0_04N	D16	IO_5_N	19.4	
L3	DIFFIO_L3_G0_05P	D14	IO_6_P	31.3	
L3	DIFFIO_L3_G0_05N_VREF	D15	IO_6_N	31.4	
L3	DIFFIO_L3_G1_06P	B15	IO_7_P	35.8	BANKL3_G1_DQS
L3	DIFFIO_L3_G1_06N	B16	IO_7_N	35.6	
L3	DIFFIO_L3_G1_07P	C13	IO_8_P	44.2	
L3	DIFFIO_L3_G1_07N	B13	IO_8_N	44.7	
L3	DIFFIO_L3_G1_08P_DQS	A15	IO_9_P	45.0	
L3	DIFFIO_L3_G1_08N_DQS	A16	IO_9_N	45.5	
L3	DIFFIO_L3_G1_09P	A13	IO_10_P	50.2	
L3	DIFFIO_L3_G1_09N	A14	IO_10_N	50.6	
L3	DIFFIO_L3_G1_10P_GSCLK	B17	IO_11_P	34.9	
L3	DIFFIO_L3_G1_10N_GSCLK	B18	IO_11_N	35.5	
L3	DIFFIO_L3_G1_11P_GMCLK	D17	IO_12_P	29.0	
L3	DIFFIO_L3_G1_11N_GMCLK	C17	IO_12_N	29.5	
L3	DIFFIO_L3_G2_12P_GMCLK	C18	IO_13_P	31.1	BANKL3_G2_DQS
L3	DIFFIO_L3_G2_12N_GMCLK	C19	IO_13_N	31.7	
L3	DIFFIO_L3_G2_13P_GSCLK	E19	IO_14_P	24.3	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L3	DIFFIO_L3_G2_13N_GSCLK	D19	IO_14_N	24.8	
L3	DIFFIO_L3_G2_14P_DQS	F18	IO_15_P	19.7	
L3	DIFFIO_L3_G2_14N_DQS	E18	IO_15_N	20.3	
L3	DIFFIO_L3_G2_15P	B20	IO_16_P	48.4	
L3	DIFFIO_L3_G2_15N	A20	IO_16_N	47.9	
L3	DIFFIO_L3_G2_16P	A18	IO_17_P	53.9	
L3	DIFFIO_L3_G2_16N	A19	IO_17_N	54.4	
L3	DIFFIO_L3_G2_17P	F19	IO_18_P	18.7	
L3	DIFFIO_L3_G2_17N	F20	IO_18_N	18.5	
L3	DIFFIO_L3_G3_18P	D20	IO_19_P	45.8	
L3	DIFFIO_L3_G3_18N_VREF	C20	IO_19_N	46.4	
L3	DIFFIO_L3_G3_19P	C22	IO_20_P	48.4	
L3	DIFFIO_L3_G3_19N	B22	IO_20_N	48.9	
L3	DIFFIO_L3_G3_20P_DQS	B21	IO_21_P	63.5	
L3	DIFFIO_L3_G3_20N_DQS	A21	IO_21_N	64.0	BANKL3_G3_DQS
L3	DIFFIO_L3_G3_21P	E22	IO_22_P	39.9	
L3	DIFFIO_L3_G3_21N	D22	IO_22_N	40.4	
L3	DIFFIO_L3_G3_22P	E21	IO_23_P	46.5	
L3	DIFFIO_L3_G3_22N	D21	IO_23_N	47.1	
L3	DIFFIO_L3_G3_23P	G21	IO_24_P	28.2	
L3	DIFFIO_L3_G3_23N	G22	IO_24_N	28.5	
L3	SIO_L3_01	F21		31.1	
L4	SIO_L4_00	J16		11.3	
L4	DIFFIO_L4_G0_00P_VAA1P	H13	IO_25_P	30.9	
L4	DIFFIO_L4_G0_00N_VAA1N	G13	IO_25_N	31.3	
L4	DIFFIO_L4_G0_01P_VAA2P	G15	IO_26_P	16.1	
L4	DIFFIO_L4_G0_01N_VAA2N	G16	IO_26_N	16.4	
L4	DIFFIO_L4_G0_02P_DQS_VAA3P	J14	IO_27_P	15.4	
L4	DIFFIO_L4_G0_02N_DQS_VAA3N	H14	IO_27_N	16.8	BANKL4_G0_DQS
L4	DIFFIO_L4_G0_03P	G17	IO_28_P	23.0	
L4	DIFFIO_L4_G0_03N	G18	IO_28_N	9.7	
L4	DIFFIO_L4_G0_04P_VAA5P	J15	IO_29_P	9.6	
L4	DIFFIO_L4_G0_04N_VAA5N	H15	IO_29_N	8.6	
L4	DIFFIO_L4_G0_05P	H17	IO_30_P	7.0	
L4	DIFFIO_L4_G0_05N_VREF	H18	IO_30_N	9.0	
L4	DIFFIO_L4_G1_06P_VAA7P	J22	IO_31_P	37.5	
L4	DIFFIO_L4_G1_06N_VAA7N	H22	IO_31_N	37.4	BANKL4_G1_DQS
L4	DIFFIO_L4_G1_07P_VAA8P	H20	IO_32_P	20.8	
L4	DIFFIO_L4_G1_07N_VAA8N	G20	IO_32_N	21.1	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L4	DIFFIO_L4_G1_08P_DQS_VAA9P	K21	IO_33_P	37.4	
L4	DIFFIO_L4_G1_08N_DQS_VAA9N	K22	IO_33_N	36.8	
L4	DIFFIO_L4_G1_09P_VAA10P	M21	IO_34_P	39.1	
L4	DIFFIO_L4_G1_09N_VAA10N	L21	IO_34_N	39.4	
L4	DIFFIO_L4_G1_10P_GSCLK	J20	IO_35_P	29.5	
L4	DIFFIO_L4_G1_10N_GSCLK	J21	IO_35_N	29.6	
L4	DIFFIO_L4_G1_11P_GMCLK	J19	IO_36_P	20.1	
L4	DIFFIO_L4_G1_11N_GMCLK	H19	IO_36_N	21.8	
L4	DIFFIO_L4_G2_12P_GMCLK	K18	IO_37_P	19.8	BANKL4_G2_DQS
L4	DIFFIO_L4_G2_12N_GMCLK	K19	IO_37_N	21.2	
L4	DIFFIO_L4_G2_13P_GSCLK	L19	IO_38_P	24.4	
L4	DIFFIO_L4_G2_13N_GSCLK	L20	IO_38_N	25.4	
L4	DIFFIO_L4_G2_14P_DQS	N22	IO_39_P	56.0	
L4	DIFFIO_L4_G2_14N_DQS_BADRVO_N	M22	IO_39_N	56.4	
L4	DIFFIO_L4_G2_15P_A28	M18	IO_40_P	19.8	
L4	DIFFIO_L4_G2_15N_A27	L18	IO_40_N	20.6	
L4	DIFFIO_L4_G2_16P_A26	N18	IO_41_P	60.7	
L4	DIFFIO_L4_G2_16N_A25	N19	IO_41_N	57.2	
L4	DIFFIO_L4_G2_17P_A24	N20	IO_42_P	25.8	
L4	DIFFIO_L4_G2_17N_A23	M20	IO_42_N	28.2	
L4	DIFFIO_L4_G3_18P_A22	K13	IO_43_P	9.8	BANKL4_G3_DQS
L4	DIFFIO_L4_G3_18N_VREF_A21	K14	IO_43_N	8.1	
L4	DIFFIO_L4_G3_19P_A20	M13	IO_44_P	30.5	
L4	DIFFIO_L4_G3_19N_A19	L13	IO_44_N	31.9	
L4	DIFFIO_L4_G3_20P_DQS	K17	IO_45_P	6.0	
L4	DIFFIO_L4_G3_20N_DQS_A18	J17	IO_45_N	7.7	
L4	DIFFIO_L4_G3_21P_A17	L14	IO_46_P	15.7	
L4	DIFFIO_L4_G3_21N_A16	L15	IO_46_N	17.3	
L4	DIFFIO_L4_G3_22P_BFOE_N	L16	IO_47_P	6.9	
L4	DIFFIO_L4_G3_22N_BFWE_FCS2_N	K16	IO_47_N	6.3	
L4	DIFFIO_L4_G3_23P_VS1	M15	IO_48_P	11.3	
L4	DIFFIO_L4_G3_23N_VS0	M16	IO_48_N	12.1	
L4	SIO_L4_01	M17		20.6	
L5	SIO_L5_00	P20		26.1	
L5	DIFFIO_L5_G0_00P_MOSI_D0	P22	IO_49_P	54.8	BANKL5_G0_DQS
L5	DIFFIO_L5_G0_00N_MISO_D1_DI	R22	IO_49_N	54.5	
L5	DIFFIO_L5_G0_01P_D2	P21	IO_50_P	36.1	
L5	DIFFIO_L5_G0_01N_D3	R21	IO_50_N	35.7	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L5	DIFFIO_L5_G0_02P_DQS_IO_STATUS_C	U22	IO_51_P	72.5	
L5	DIFFIO_L5_G0_02N_DQS_ECCLKIN	V22	IO_51_N	72.5	
L5	DIFFIO_L5_G0_03P_D4	T21	IO_52_P	45.6	
L5	DIFFIO_L5_G0_03N_D5	U21	IO_52_N	45.7	
L5	DIFFIO_L5_G0_04P_D6	P19	IO_53_P	32.1	
L5	DIFFIO_L5_G0_04N_D7	R19	IO_53_N	33.0	
L5	DIFFIO_L5_G0_05P_FCS_N	T19	IO_54_P	40.9	
L5	DIFFIO_L5_G0_05N_VREF_D8	T20	IO_54_N	39.0	
L5	DIFFIO_L5_G1_06P_D9	W21	IO_55_P	76.6	
L5	DIFFIO_L5_G1_06N_D10	W22	IO_55_N	77.2	
L5	DIFFIO_L5_G1_07P_D11	AA20	IO_56_P	76.3	
L5	DIFFIO_L5_G1_07N_D12	AA21	IO_56_N	76.1	
L5	DIFFIO_L5_G1_08P_DQS_N	Y21	IO_57_P	81.8	
L5	DIFFIO_L5_G1_08N_DQS_D13	Y22	IO_57_N	82.3	BANKL5_G1_DQS
L5	DIFFIO_L5_G1_09P_D14	AB21	IO_58_P	84.4	
L5	DIFFIO_L5_G1_09N_D15	AB22	IO_58_N	84.2	
L5	DIFFIO_L5_G1_10P_GSCLK	U20	IO_59_P	56.4	
L5	DIFFIO_L5_G1_10N_GSCLK	V20	IO_59_N	56.8	
L5	DIFFIO_L5_G1_11P_GMCLK	W19	IO_60_P	61.0	
L5	DIFFIO_L5_G1_11N_GMCLK	W20	IO_60_N	61.2	
L5	DIFFIO_L5_G2_12P_GMCLK	Y18	IO_61_P	74.3	
L5	DIFFIO_L5_G2_12N_GMCLK	Y19	IO_61_N	78.7	
L5	DIFFIO_L5_G2_13P_GSCLK	V18	IO_62_P	44.1	
L5	DIFFIO_L5_G2_13N_GSCLK	V19	IO_62_N	45.2	
L5	DIFFIO_L5_G2_14P_DQS_RWSEL	AA19	IO_63_P	85.4	
L5	DIFFIO_L5_G2_14N_DQS_CSO_DOUT	AB20	IO_63_N	85.7	BANKL5_G2_DQS
L5	DIFFIO_L5_G2_15P_CS_N	V17	IO_64_P	48.1	
L5	DIFFIO_L5_G2_15N_D31_A15	W17	IO_64_N	48.3	
L5	DIFFIO_L5_G2_16P_D30_A14	AA18	IO_65_P	87.5	
L5	DIFFIO_L5_G2_16N_D29_A13	AB18	IO_65_N	87.3	
L5	DIFFIO_L5_G2_17P_D28_A12	U17	IO_66_P	33.4	
L5	DIFFIO_L5_G2_17N_D27_A11	U18	IO_66_N	32.8	
L5	DIFFIO_L5_G3_18P_D26_A10	P14	IO_67_P	23.6	
L5	DIFFIO_L5_G3_18N_VREF_D25_A9	R14	IO_67_N	23.7	
L5	DIFFIO_L5_G3_19P_D24_A8	R18	IO_68_P	23.8	BANKL5_G3_DQS
L5	DIFFIO_L5_G3_19N_D23_A7	T18	IO_68_N	24.4	
L5	DIFFIO_L5_G3_20P_DQS	N17	IO_69_P	10.9	
L5	DIFFIO_L5_G3_20N_DQS_D22_A6	P17	IO_69_N	12.7	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L5	DIFFIO_L5_G3_21P_D21_A5	P15	IO_70_P	26.1	
L5	DIFFIO_L5_G3_21N_D20_A4	R16	IO_70_N	27.1	
L5	DIFFIO_L5_G3_22P_D19_A3	N13	IO_71_P	16.4	
L5	DIFFIO_L5_G3_22N_D18_A2	N14	IO_71_N	16.6	
L5	DIFFIO_L5_G3_23P_D17_A1	P16	IO_72_P	16.4	
L5	DIFFIO_L5_G3_23N_D16_A0	R17	IO_72_N	16.5	
L5	SIO_L5_01	N15		12.7	
L6	SIO_L6_00	Y17		49.2	
L6	DIFFIO_L6_G0_00P	Y16	IO_73_P	71.9	
L6	DIFFIO_L6_G0_00N	AA16	IO_73_N	71.5	
L6	DIFFIO_L6_G0_01P	AB16	IO_74_P	67.3	
L6	DIFFIO_L6_G0_01N	AB17	IO_74_N	67.7	
L6	DIFFIO_L6_G0_02P_DQS	AA13	IO_75_P	103.5	
L6	DIFFIO_L6_G0_02N_DQS	AB13	IO_75_N	103.9	BANKL6_G0_DQS
L6	DIFFIO_L6_G0_03P	AA15	IO_76_P	73.4	
L6	DIFFIO_L6_G0_03N	AB15	IO_76_N	73.6	
L6	DIFFIO_L6_G0_04P	Y13	IO_77_P	82.7	
L6	DIFFIO_L6_G0_04N	AA14	IO_77_N	83.1	
L6	DIFFIO_L6_G0_05P	W14	IO_78_P	58.8	
L6	DIFFIO_L6_G0_05N_VREF	Y14	IO_78_N	59.7	
L6	DIFFIO_L6_G1_06P	AB11	IO_79_P	97.1	
L6	DIFFIO_L6_G1_06N	AB12	IO_79_N	97.5	
L6	DIFFIO_L6_G1_07P	AA9	IO_80_P	92.0	
L6	DIFFIO_L6_G1_07N	AB10	IO_80_N	91.7	
L6	DIFFIO_L6_G1_08P_DQS	AA10	IO_81_P	91.2	
L6	DIFFIO_L6_G1_08N_DQS	AA11	IO_81_N	91.0	BANKL6_G1_DQS
L6	DIFFIO_L6_G1_09P	V10	IO_82_P	86.1	
L6	DIFFIO_L6_G1_09N	W10	IO_82_N	85.9	
L6	DIFFIO_L6_G1_10P_GSCLK	Y11	IO_83_P	79.3	
L6	DIFFIO_L6_G1_10N_GSCLK	Y12	IO_83_N	79.4	
L6	DIFFIO_L6_G1_11P_GMCLK	W11	IO_84_P	68.6	
L6	DIFFIO_L6_G1_11N_GMCLK	W12	IO_84_N	68.5	
L6	DIFFIO_L6_G2_12P_GMCLK	V13	IO_85_P	60.1	
L6	DIFFIO_L6_G2_12N_GMCLK	V14	IO_85_N	60.2	
L6	DIFFIO_L6_G2_13P_GSCLK	U15	IO_86_P	50.0	
L6	DIFFIO_L6_G2_13N_GSCLK	V15	IO_86_N	48.6	BANKL6_G2_DQS
L6	DIFFIO_L6_G2_14P_DQS	T14	IO_87_P	50.2	
L6	DIFFIO_L6_G2_14N_DQS	T15	IO_87_N	49.0	
L6	DIFFIO_L6_G2_15P	W15	IO_88_P	40.3	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L6	DIFFIO_L6_G2_15N	W16	IO_88_N	40.3	
L6	DIFFIO_L6_G2_16P	T16	IO_89_P	30.7	
L6	DIFFIO_L6_G2_16N	U16	IO_89_N	30.5	
R4	SIO_R4_00	F4		16.6	
R4	DIFFIO_R4_G0_00P_VAA4P	B1	IO_90_P	63.9	BANKR4_G0_DQS
R4	DIFFIO_R4_G0_00N_VAA4N	A1	IO_90_N	64.5	
R4	DIFFIO_R4_G0_01P_VAA6P	C2	IO_91_P	46.0	
R4	DIFFIO_R4_G0_01N_VAA6N	B2	IO_91_N	46.4	
R4	DIFFIO_R4_G0_02P_DQS_VAA11P	E1	IO_92_P	63.4	
R4	DIFFIO_R4_G0_02N_DQS_VAA11N	D1	IO_92_N	63.9	
R4	DIFFIO_R4_G0_03P	E2	IO_93_P	45.0	
R4	DIFFIO_R4_G0_03N	D2	IO_93_N	44.5	
R4	DIFFIO_R4_G0_04P_VAA12P	G1	IO_94_P	54.1	
R4	DIFFIO_R4_G0_04N_VAA12N	F1	IO_94_N	54.7	
R4	DIFFIO_R4_G0_05P	F3	IO_95_P	35.1	
R4	DIFFIO_R4_G0_05N_VREF	E3	IO_95_N	34.8	
R4	DIFFIO_R4_G1_06P_VAA13P	K1	IO_96_P	65.2	BANKR4_G1_DQS
R4	DIFFIO_R4_G1_06N_VAA13N	J1	IO_96_N	65.5	
R4	DIFFIO_R4_G1_07P_VAA14P	H2	IO_97_P	42.2	
R4	DIFFIO_R4_G1_07N_VAA14N	G2	IO_97_N	41.8	
R4	DIFFIO_R4_G1_08P_DQS_VAA15P	K2	IO_98_P	57.5	
R4	DIFFIO_R4_G1_08N_DQS_VAA15N	J2	IO_98_N	57.4	
R4	DIFFIO_R4_G1_09P_VAA0P	J5	IO_99_P	11.6	
R4	DIFFIO_R4_G1_09N_VAA0N	H5	IO_99_N	12.2	
R4	DIFFIO_R4_G1_10P_GSCLK	H3	IO_100_P	39.1	
R4	DIFFIO_R4_G1_10N_GSCLK	G3	IO_100_N	38.5	
R4	DIFFIO_R4_G1_11P_GMCLK	H4	IO_101_P	23.0	
R4	DIFFIO_R4_G1_11N_GMCLK	G4	IO_101_N	23.5	
R4	DIFFIO_R4_G2_12P_GMCLK	K4	IO_102_P	28.9	BANKR4_G2_DQS
R4	DIFFIO_R4_G2_12N_GMCLK	J4	IO_102_N	28.5	
R4	DIFFIO_R4_G2_13P_GSCLK	L3	IO_103_P	26.0	
R4	DIFFIO_R4_G2_13N_GSCLK	K3	IO_103_N	26.4	
R4	DIFFIO_R4_G2_14P_DQS	M1	IO_104_P	46.6	
R4	DIFFIO_R4_G2_14N_DQS	L1	IO_104_N	46.1	
R4	DIFFIO_R4_G2_15P	M3	IO_105_P	37.7	
R4	DIFFIO_R4_G2_15N	M2	IO_105_N	37.6	
R4	DIFFIO_R4_G2_16P	K6	IO_106_P	8.1	
R4	DIFFIO_R4_G2_16N	J6	IO_106_N	10.5	
R4	DIFFIO_R4_G2_17P	L5	IO_107_P	11.3	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R4	DIFFIO_R4_G2_17N	L4	IO_107_N	12.6	
R4	DIFFIO_R4_G3_18P	N4	IO_108_P	43.2	BANKR4_G3_DQS
R4	DIFFIO_R4_G3_18N_VREF	N3	IO_108_N	43.2	
R4	DIFFIO_R4_G3_19P	R1	IO_109_P	48.1	
R4	DIFFIO_R4_G3_19N	P1	IO_109_N	47.9	
R4	DIFFIO_R4_G3_20P_DQS	P5	IO_110_P	42.8	
R4	DIFFIO_R4_G3_20N_DQS	P4	IO_110_N	43.3	
R4	DIFFIO_R4_G3_21P	P2	IO_111_P	38.2	
R4	DIFFIO_R4_G3_21N	N2	IO_111_N	38.6	
R4	DIFFIO_R4_G3_22P	M6	IO_112_P	27.4	
R4	DIFFIO_R4_G3_22N	M5	IO_112_N	28.3	
R4	DIFFIO_R4_G3_23P	P6	IO_113_P	27.9	
R4	DIFFIO_R4_G3_23N	N5	IO_113_N	28.0	
R4	SIO_R4_01	L6		4.5	
R5	SIO_R5_00	T3		37.8	
R5	DIFFIO_R5_G0_00P	T1	IO_114_P	65.1	BANKR5_G0_DQS
R5	DIFFIO_R5_G0_00N	U1	IO_114_N	64.5	
R5	DIFFIO_R5_G0_01P	U2	IO_115_P	52.3	
R5	DIFFIO_R5_G0_01N	V2	IO_115_N	52.1	
R5	DIFFIO_R5_G0_02P_DQS	R3	IO_116_P	49.1	
R5	DIFFIO_R5_G0_02N_DQS	R2	IO_116_N	49.4	
R5	DIFFIO_R5_G0_03P	W2	IO_117_P	62.6	
R5	DIFFIO_R5_G0_03N	Y2	IO_117_N	62.1	
R5	DIFFIO_R5_G0_04P	W1	IO_118_P	79.5	
R5	DIFFIO_R5_G0_04N	Y1	IO_118_N	79.0	
R5	DIFFIO_R5_G0_05P	U3	IO_119_P	46.8	
R5	DIFFIO_R5_G0_05N_VREF	V3	IO_119_N	46.9	
R5	DIFFIO_R5_G1_06P	AA1	IO_120_P	90.2	BANKR5_G1_DQS
R5	DIFFIO_R5_G1_06N	AB1	IO_120_N	90.7	
R5	DIFFIO_R5_G1_07P	AB3	IO_121_P	76.7	
R5	DIFFIO_R5_G1_07N	AB2	IO_121_N	76.9	
R5	DIFFIO_R5_G1_08P_DQS	Y3	IO_122_P	73.7	
R5	DIFFIO_R5_G1_08N_DQS	AA3	IO_122_N	73.5	
R5	DIFFIO_R5_G1_09P	AA5	IO_123_P	70.6	
R5	DIFFIO_R5_G1_09N	AB5	IO_123_N	70.3	
R5	DIFFIO_R5_G1_10P_GSCLK	Y4	IO_124_P	74.4	
R5	DIFFIO_R5_G1_10N_GSCLK	AA4	IO_124_N	74.1	
R5	DIFFIO_R5_G1_11P_GMCLK	V4	IO_125_P	48.8	
R5	DIFFIO_R5_G1_11N_GMCLK	W4	IO_125_N	48.8	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R5	DIFFIO_R5_G2_12P_GMCLK	R4	IO_126_P	36.7	BANKR5_G2_DQS
R5	DIFFIO_R5_G2_12N_GMCLK	T4	IO_126_N	37.2	
R5	DIFFIO_R5_G2_13P_GSCLK	T5	IO_127_P	31.2	
R5	DIFFIO_R5_G2_13N_GSCLK	U5	IO_127_N	31.8	
R5	DIFFIO_R5_G2_14P_DQS	W6	IO_128_P	68.2	
R5	DIFFIO_R5_G2_14N_DQS	W5	IO_128_N	68.6	
R5	DIFFIO_R5_G2_15P	U6	IO_129_P	35.7	
R5	DIFFIO_R5_G2_15N	V5	IO_129_N	36.1	
R5	DIFFIO_R5_G2_16P	R6	IO_130_P	31.5	
R5	DIFFIO_R5_G2_16N	T6	IO_130_N	31.4	
R5	DIFFIO_R5_G2_17P	Y6	IO_131_P	57.3	
R5	DIFFIO_R5_G2_17N	AA6	IO_131_N	57.6	
R5	DIFFIO_R5_G3_18P	V7	IO_132_P	56.1	BANKR5_G3_DQS
R5	DIFFIO_R5_G3_18N_VREF	W7	IO_132_N	55.9	
R5	DIFFIO_R5_G3_19P	AB7	IO_133_P	71.9	
R5	DIFFIO_R5_G3_19N	AB6	IO_133_N	72.2	
R5	DIFFIO_R5_G3_20P_DQS	V9	IO_134_P	96.9	
R5	DIFFIO_R5_G3_20N_DQS	V8	IO_134_N	97.0	
R5	DIFFIO_R5_G3_21P	AA8	IO_135_P	65.4	
R5	DIFFIO_R5_G3_21N	AB8	IO_135_N	65.7	
R5	DIFFIO_R5_G3_22P	Y8	IO_136_P	75.7	
R5	DIFFIO_R5_G3_22N	Y7	IO_136_N	75.3	
R5	DIFFIO_R5_G3_23P	W9	IO_137_P	61.2	
R5	DIFFIO_R5_G3_23N	Y9	IO_137_N	61.7	
R5	SIO_R5_01	U7		37.7	
CFG	INIT_FLAG_N	U12		47.2	
CFG	CFG_DONE	G11		90.7	
CFG	RSTN	N12		17.8	
CFG	CFG_CLK	L12		24.3	
CFG	TCK	V12		48.7	
CFG	TMS	T13		35.2	
CFG	TDI	R13		29.7	
CFG	TDO	U13		45.0	
CFG	MODE_0	U11		54.0	
CFG	MODE_1	U10		52.9	
CFG	MODE_2	U9		57.8	
CFG	SCBV	U8		70.0	
CFG	VAADC_N	M9	IO_138_N	47.3	
CFG	VAADC_P	L10	IO_138_P	53.0	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
CFG	VCCADC	K10			
CFG	VREFADC_N	L9	IO_139_N	47.9	
CFG	VREFADC_P	M10	IO_139_P	48.2	
CFG	VSSADC	K9			
CFG	TSDN	N9	IO_140_N	65.9	
CFG	TSDP	N10	IO_140_P	66.4	
CFG	VCCB	E12			
CFG	VCCIOCFG	F12			
CFG	VCCIOCFG	T12			
	HSSTRX0N_QL3	A8	IO_141_N	46.5	
	HSSTRX0P_QL3	B8	IO_141_P	46.7	
	HSSTRX1N_QL3	C11	IO_142_N	28.1	
	HSSTRX1P_QL3	D11	IO_142_P	28.4	
	HSSTRX2N_QL3	A10	IO_143_N	52.7	
	HSSTRX2P_QL3	B10	IO_143_P	52.6	
	HSSTRX3N_QL3	C9	IO_144_N	63.4	
	HSSTRX3P_QL3	D9	IO_144_P	63.2	
	HSSTTX0N_QL3	A4	IO_145_N	82.4	
	HSSTTX0P_QL3	B4	IO_145_P	82.6	
	HSSTTX1N_QL3	C5	IO_146_N	57.5	
	HSSTTX1P_QL3	D5	IO_146_P	57.6	
	HSSTTX2N_QL3	A6	IO_147_N	88.3	
	HSSTTX2P_QL3	B6	IO_147_P	88.5	
	HSSTTX3N_QL3	C7	IO_148_N	57.3	
	HSSTTX3P_QL3	D7	IO_148_P	57.6	
	HSSTREFCLK0P_QL3	F6	IO_149_P	44.7	
	HSSTREFCLK0N_QL3	E6	IO_149_N	45.5	
	HSSTREFCLK1N_QL3	E10	IO_150_N	13.1	
	HSSTREFCLK1P_QL3	F10	IO_150_P	13.9	
	HSSTRREF_QL3	F8		29.8	
	HSSTAVCC_G3	D10			
	HSSTAVCC_G3	D6			
	HSSTAVCC_G3	E8			
	HSSTAVCC_G3	F7			
	HSSTAVCC_G3	F9			
	HSSTAVCCPLL_G3	B11			
	HSSTAVCCPLL_G3	B5			
	HSSTAVCCPLL_G3	B7			
	HSSTAVCCPLL_G3	B9			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	HSSTAVCCPLL_G3	C4			
	HSSTAVCCPLL_G3	C8			
	VCC	H10			
	VCC	H8			
	VCC	J7			
	VCC	J9			
	VCC	K8			
	VCC	L7			
	VCC	M8			
	VCC	N7			
	VCC	P10			
	VCC	P8			
	VCC	R7			
	VCC	R9			
	VCC	T10			
	VCC	T8			
	VCCA	H12			
	VCCA	K12			
	VCCA	M12			
	VCCA	P12			
	VCCA	R11			
	VCC_DRM	J11			
	VCC_DRM	L11			
	VCC_DRM	N11			
	VCCIO_L3	A17			
	VCCIO_L3	B14			
	VCCIO_L3	C21			
	VCCIO_L3	D18			
	VCCIO_L3	E15			
	VCCIO_L3	F22			
	VCCIO_L4	G19			
	VCCIO_L4	H16			
	VCCIO_L4	J13			
	VCCIO_L4	K20			
	VCCIO_L4	L17			
	VCCIO_L4	N21			
	VCCIO_L5	M14			
	VCCIO_L5	P18			
	VCCIO_L5	R15			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCCIO_L5	T22			
	VCCIO_L5	U19			
	VCCIO_L5	Y20			
	VCCIO_L6	AA17			
	VCCIO_L6	AB14			
	VCCIO_L6	V16			
	VCCIO_L6	W13			
	VCCIO_L6	Y10			
	VCCIO_R4	C1			
	VCCIO_R4	F2			
	VCCIO_R4	H6			
	VCCIO_R4	J3			
	VCCIO_R4	M4			
	VCCIO_R4	N1			
	VCCIO_R5	AA7			
	VCCIO_R5	AB4			
	VCCIO_R5	R5			
	VCCIO_R5	T2			
	VCCIO_R5	V6			
	VCCIO_R5	W3			
	VSS	A11			
	VSS	A12			
	VSS	A2			
	VSS	A22			
	VSS	A3			
	VSS	A5			
	VSS	A7			
	VSS	A9			
	VSS	AA12			
	VSS	AA2			
	VSS	AA22			
	VSS	AB19			
	VSS	AB9			
	VSS	B12			
	VSS	B19			
	VSS	B3			
	VSS	C10			
	VSS	C12			
	VSS	C16			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	C3			
	VSS	C6			
	VSS	D12			
	VSS	D13			
	VSS	D3			
	VSS	D4			
	VSS	D8			
	VSS	E11			
	VSS	E20			
	VSS	E4			
	VSS	E5			
	VSS	E7			
	VSS	E9			
	VSS	F11			
	VSS	F17			
	VSS	F5			
	VSS	G10			
	VSS	G12			
	VSS	G14			
	VSS	G5			
	VSS	G6			
	VSS	G7			
	VSS	G8			
	VSS	G9			
	VSS	H1			
	VSS	H11			
	VSS	H21			
	VSS	H7			
	VSS	H9			
	VSS	J10			
	VSS	J12			
	VSS	J18			
	VSS	J8			
	VSS	K11			
	VSS	K15			
	VSS	K5			
	VSS	K7			
	VSS	L2			
	VSS	L22			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	L8			
	VSS	M11			
	VSS	M19			
	VSS	M7			
	VSS	N16			
	VSS	N6			
	VSS	N8			
	VSS	P11			
	VSS	P13			
	VSS	P3			
	VSS	P7			
	VSS	P9			
	VSS	R10			
	VSS	R12			
	VSS	R20			
	VSS	R8			
	VSS	T11			
	VSS	T17			
	VSS	T7			
	VSS	T9			
	VSS	U14			
	VSS	U4			
	VSS	V1			
	VSS	V11			
	VSS	V21			
	VSS	W18			
	VSS	W8			
	VSS	Y15			
	VSS	Y5			

2.2.2 Thermal Resistance

Table 2-3 Thermal Resistance

θJA(℃/W) (Flow: 0m/s)	θJB(℃/W)	θJC(℃/W)	θJA(℃/W) (Flow: 1m/s)	θJA(℃/W) (Flow: 2m/s)
11.6	5.6	0.02	10.2	9.5

2.2.3 Pressure Value

1. Short term pressure (within 5 minutes): 100g/ball, 484 balls, short term pressure can meet 48.4kg.
2. Long term pressure: 30g/ball, 484 balls, long term pressure can meet 14.52kg.

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