Logos2 Family Hardware Design Guide

(UG040012, V1.4)

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Revisions History

Version	Date of Release	Revisions
V1.3	03.01.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
DRM	Dedicated RAM Module
DDR	Double Data Rate
ADC	Analog to Digital Converter
HSSTLP	High Speed Serial Transceiver Low Performance
TMDS	Transition-minimized differential signal
LVDS	Low-Voltage Differential Signaling

Tables of Contents

Tables

Chapter 1 Overview

This document is hardware design guide for the Logos2 Family FPGA devices by Shenzhen Pango Microsystems Co., Ltd. (hereinafter referred to as Pango Microsystems). Users can understand the relevant requirements when using the Logos2 Family FPGA hardware design through this document.

For details on Logos2 Family FPGA product features, resource scale, and packaging information, please refers to the "***DS04001_Logos2 Family FPGAs Device Data Sheet***".

Chapter 2 Power Supply Design

2.1 Voltage Requirements

For the absolute voltage limits, recommended operating voltage, power-up/power-down requirements, and power-up ramp time requirements of the device, please refer to the "***DS04001 Logos2 Family FPGAs Device Data Sheet***".

The Logos2 Family FPGA supports multiple configuration methods, with configuration-related pins distributed across three banks: Configuration bank, bank L4, and bank L5. For different configuration signal voltage levels, the power voltage limitations for the three banks are as shown in Table 2-1. Please note that voltage combinations outside the table are not supported.

Table 2-1 Configuration-related Bank Supply Voltages

Configuration Mode	**Configuration Interface IO Voltage Levels**	**Bank Voltage**			**SCBV Pin**
		VCCIOCFG	**VCCIOL4**	**VCCIOL5**	
JTAG	3.3V	3.3V	Any[1]	Any[1]	VCCIOCFG
	2.5V	2.5V	Any[1]	Any[1]	VCCIOCFG
	1.8V	1.8V	1.8V/1.5V/ 1.2V	1.8V/1.5V/ 1.2V	GND
	1.5V	1.5V	1.8V/1.5V/ 1.2V	1.8V/1.5V/ 1.2V	GND
	1.2V	1.2V	1.8V/1.5V/ 1.2V	1.8V/1.5V/ 1.2V	GND
Slave Serial, Slave Parallel, Master SPI(X1/X2/X4)	3.3V	3.3V	Any[1]	3.3V	VCCIOCFG
	2.5V	2.5V	Any[1]	2.5V	VCCIOCFG
	1.8V	1.8V	1.8V/1.5V/ 1.2V	1.8V	GND
	1.5V	1.5V	1.8V/1.5V/ 1.2V	1.5V	GND
	1.2V	1.2V	1.8V/1.5V/ 1.2V	1.2V	GND
Master SPI(X8)	3.3V	3.3V	3.3V	3.3V	VCCIOCFG
	2.5V	2.5V	2.5V	2.5V	VCCIOCFG
	1.8V	1.8V	1.8V	1.8V	GND
	1.5V	1.5V	1.5V	1.5V	GND
	1.2V	1.2V	1.2V	1.2V	GND

Notes:

1. The Any condition does not support floating.

2.2 Capacitance Requirements

The following tables provide the capacitance requirements and capacitor parameter requirements of each power supply under certain conditions. HSSTLP power decoupling capacitor requirements are shown in HSSTLP Design Description.

Table 2-2 PG2L25H Decoupling Capacitor Recommendations

Power Supply	Package	100uF	47uF	4.7uF	0.47uF	0.1uF	Description
VCC	MBG325	1	0	2	3	5	Core logic power supply
VCC_DRM	MBG325	0	1	0	2	2	DRM power supply
VCCA	MBG325	0	1	1	2	2	Auxiliary power supply
VCCIOCFG	MBG325	0	1	0	1	1	Configuration bank power supply
VCCIO	MBG325	0	2	2	4	2	For bank power supplies, the 47uF capacitance can be appropriately reduced when multiple banks share the same power supply.

Table 2-3 PG2L50H Decoupling Capacitor Recommendations

Power Supply	Package	100uF	47uF	4.7uF	0.47uF	0.1uF	Description
VCC	FBG484	3	0	6	8	5	Core logic power supply
	MBG324	3	0	6	8	5	
VCC_DRM	FBG484	1	0	0	2	2	DRM power supply
	MBG324	1	0	0	2	2	
VCCA	FBG484	0	1	3	5	2	Auxiliary power supply
	MBG324	0	1	3	4	2	
VCCIOCFG	FBG484	0	1	0	1	1	Configuration bank power supply
	MBG324	0	1	0	1	1	
VCCIO	FBG484	0	2	2	4	2	For bank power supplies, the 47uF capacitance can be appropriately reduced when multiple banks share the same power supply.
	MBG324	0	2	2	4	2	

Table 2-4 PG2L100H Decoupling Capacitor Recommendations

Power Supply	Package	100uF	47uF	4.7uF	0.47uF	0.1uF	Description
VCC	FBG484	3	0	6	8	5	Core logic power supply
	FBG676	3	0	6	8	5	
	MBG324	3	0	6	8	5	
VCC_DRM	FBG484	1	0	0	2	2	DRM power supply
	FBG676	1	0	0	2	2	
	MBG324	1	0	0	2	2	
VCCA	FBG484	0	1	3	5	2	Auxiliary power supply
	FBG676	0	1	3	5	2	
	MBG324	0	1	3	4	2	
VCCIOCFG	FBG484	0	1	0	1	1	Configuration bank power supply
	FBG676	0	1	0	1	1	
	MBG324	0	1	0	1	1	
VCCIO	FBG484	0	2	2	4	2	For bank power supplies, the 47uF capacitance can be appropriately reduced when multiple banks share the same power supply.
	FBG676	0	2	2	4	2	
	MBG324	0	2	2	4	2	

Table 2-5 PG2L200H Decoupling Capacitor Recommendations

Power Supply	Package	100uF	47uF	4.7uF	0.47uF	0.1uF	Description
VCC	FBB484	7	0	12	14	10	Core logic power supply
	FBB676	7	0	12	14	10	
	FFBG1156	7	0	12	14	10	
VCC_DRM	FBB484	1	0	0	5	5	DRM power supply
	FBB676	1	0	0	5	5	
	FFBG1156	1	0	0	5	5	
VCCA	FBB484	0	1	3	5	3	Auxiliary power supply
	FBB676	0	1	4	7	5	
	FFBG1156	0	1	5	9	7	
VCCIOCFG	FBB484	0	1	0	1	1	Configuration bank power supply
	FBB676	0	1	0	1	1	
	FFBG1156	0	1	0	1	1	
VCCIO	FBB484	0	2	2	4	2	For bank power supplies, the 47uF capacitance can be appropriately reduced when multiple banks share the same power supply.
	FBB676	0	2	2	4	2	
	FFBG1156	0	2	2	4	2	

Table 2-6 Decoupling Capacitor Parameter Description

Parameter	**100uF**	**47uF**	**4.7uF**	**0.47uF**	**0.1uF**
Package	1210	1210	0805	0402	0402
Tolerance	≥2V	≥6V	≥6V	≥6V	≥6V
ESL	≤1nH	≤1nH	≤0.5nH	≤0.5nH	≤0.5nH
ESR	≤40mΩ	≤40mΩ	≤20mΩ	≤20mΩ	≤20mΩ
Material	X5R	X5R	X7R	X7R	X7R

2.3 Other Descriptions

2.3.1 DRM Power Supply Description

The core power supply VCC and the dedicated power supply VCC_DRM can be connected to the same 1.0V power supply.

2.3.2 Multiplex Configuration Pin Power Supply Description

The power supplies of bank L4 and bank L5 must meet the supply voltage conditions listed in Table 2-1.

2.3.3 Design Power Consumption Description

For the design power consumption (including HSSTLP power consumption), please refer to the power estimation software (Pango Power Planner in the PDS (Pango Design Suite)).

Chapter 3 Configuration Description

3.1 Configuration Pin Description

For usage instructions for the Logos2 Family FPGA configuration-related pins, please refer to the "***UG040005 Logos2 Family FPGAs Configuration User Guide***". Please note that the SCBV pin state in the PDS project needs to be configured to be consistent with the design of the hardware. For definitions of configuration-related pins, please refer to the packaging manual of the relevant devices "***PK04xxx***", for example, "PK04001_PG2L100H_FBG676".

3.2 Configuration Mode Selection

MODE[2:0] is the configuration mode selection pin. When the INIT_N signal transitions from low to high, MODE[2:0] pins are sampled to determine the current configuration mode of the FPGA.

The correspondence for MODE[2:0] and configuration mode is as follows:

- 001: Master SPI configuration modes (X1/X2/X4/X8);
- 101: JTAG configuration mode (X1);
- 110: Slave parallel configuration mode (X8/X16/X32);
- 111: Slave serial configuration mode (X1).

Chapter 4 ADC Design Description

For ADC features, please refer to the "***DS04001 Logos2 Family FPGAs Device Data Sheet***". For ADC applications, please refer to the "***UG040009 Logos2 Family FPGAs Analog-to-Digital Converter (ADC) Module User Guide***".

Chapter 5 HSSTLP Design Description

When applying HSSTLP, please refer to the relevant instructions about HSSTLP in the "***DS04001 Logos2 Family FPGAs Device Data Sheet***".

5.1 HSSTLP Pin Description

Table 5-1 Logos2 Family FPGA HSSTLP Pin Description

Pin	Pin Type	Direction	Pin Description
HSSTAVCC	Dedicated	N/A	1.0V analog power pin connected to the internal transmitting and receiving circuits; When HSSTLP is not in use, handle it as floating and reserve a position for a grounding resistor.
HSSTAVCCPLL	Dedicated	N/A	1.2V analog power pin connected to the PLL; When HSSTLP is not in use, handle it as floating and reserve a position for a grounding resistor.
HSSTRREF_Q[R,L][7:0]	Dedicated	Input	Calibration resistor input pin for the terminal resistor calibration circuit; 1. The PG2L200H needs to be pulled up to HSSTAVCCPLL through a 100Ω calibration resistor (accuracy 1%); 2. Devices other than PG2L200H need to be pulled up to HSSTAVCC through a 200Ω calibration resistor (accuracy 1%); grounded when HSSTLP is not in use.
HSSTREFCLK[0,1]P_Q[R,L][7:0]	Dedicated	Input	Differential clock input pin P side, providing reference clock to HSSTLP. External addition of 100nF AC coupling required; Leave floating when HSSTLP is not in use.
HSSTREFCLK[0,1]N_Q[R,L][7:0]	Dedicated	Input	Differential clock input pin N side, providing reference clock to HSSTLP. External addition of 100nF AC coupling required; Leave floating when HSSTLP is not in use.
HSSTTX[0,1,2,3][P,N]_Q[R,L][7:0]	Dedicated	Output	Differential output of HSSTLP channel. Each HSSTLP has 4 pairs; Leave floating when HSSTLP is not in use.
HSSTRX[0,1,2,3][P,N]_Q[R,L][7:0]	Dedicated	Input	Differential input of HSSTLP channel. Each HSSTLP has 4 pairs; Grounded when HSSTLP is not in use.

5.2 HSSTLP Decoupling Capacitor Requirements

The recommended power supply for both groups of HSSTLP is to be provided by LDO, with the filtering capacitors requirements as follows:

Table 5-2 HSSTLP Decoupling Capacitor Requirements

Power Supply	Product Model	Package	4.7uF (X7R/10%)	0.1uF (X7R/10%)
HSSTAVCC	PG2L25H	MBG325	2	5
	PG2L50H	FBG484	2	5
	PG2L100H	FBG676	4	10
		FBG484	2	5
	PG2L200H	FBB484	2	5
		FBB676	4	10
		FFBG1156	8	20
HSSTAVCCPLL	PG2L25H	MBG325	2	6
	PG2L50H	FBG484	2	6
	PG2L100H	FBG676	4	12
		FBG484	2	6
	PG2L200H	FBB484	2	6
		FBB676	4	12
		FFBG1156	8	24

Notes:

1. Users may adjust the capacitance based on actual conditions, but the power ripple must be met.

5.3 Other Considerations

- The ripple for power supplies HSSTAVCC and HSSTAVCCPLL is less than 10mv.
- There is no timing requirements for power supply of HSSTAVCC and HSSTAVCCPLL. It is recommended to power on at the same time;
- PCIe X1 can be placed on any channel. PCIe X2 is limited to lane0/lane1 or lane2/lane3; for PCIe HSSTLP channel selection, please refer to the "***UG042004_Logos2_PCIe_IP_UserGuide***";
- When HSSTLP is not in use, HSSTLP power is left floating and a position for a grounding resistor is reserved. RX pins should be grounded. For details, please refer to Table 5-1;
- It is recommended to designed different power supplies separately;
- For PG2L100H, HSSTLP_QR3 is recommended as PCIe hard core;

Chapter 6 LVDS Design Description

- Each bank supports input and output, with a bank voltage of 2.5V;
- LVDS performance is affected by capacitive load size and line loss. Simulation evaluation is recommended;
- Differential IO includes a built-in 100Ω terminal matching resistor;
- Input clock is placed on the clock input pin;
- Pin delay information needs to be added during PCB layout.

Chapter 7 TMDS Design Description

- Each bank can support TMDS, with a bank voltage of 3.3V;
- The receiver requires external 50Ω resistors to be pulled up to the bank voltage;
- The receiver clock is placed on the clock input pin;
- Pin delay information needs to be added during PCB layout.

Chapter 8 DDR3 Design Description

8.1 Schematic Design Description

- The reference clock input pin GMCLK should be chosen from the bank with the same DDR interface or adjacent bank; For scenarios other than X16 single bank, the GMCLK of the bank with the command/address byte group should be chosen as the reference clock input to ensure minimal clock jitter; For X16 single bank scenarios, the clock pins are usually occupied, and it is recommended to choose the GMCLK of the adjacent bank as the reference clock input. The level standard selected for the reference clock pin must match the VCCIO voltage of the corresponding bank. For supported input level standards, please refer to the "***UG040006 Logos2 Family FPGAs Input and Output Interfaces (IO) User Guide***". The hardware circuit must meet the DC characteristics of the level standard specified in the "***DS04001 Logos2 Family FPGAs Device Data Sheet***". To meet the above requirements, refer to the AC coupling with DC bias circuit;
- Each bank only needs one external VREF reference voltage input, with a voltage value of half the bank voltage/DDR3 chip supply voltage; VREF can be generated by voltage dividing with two 1KΩ resistors or provided by a dedicated power supply chip;
- The CK must be connected to the P/N pair pins of a command/address byte group;
- The DQS signal must be connected to the dedicated DQS pin;
- DQ and DM must be connected to the corresponding DQS byte group pins;
- The span of a single DDR3 interface cannot exceed 3 adjacent banks on the same side. For a DDR3 interface spanning 3 banks, the command/address signals must be located in the middle bank, and all command/address signals must be within the same bank;
- Command/address signals must be connected to pins that are not used for data grouping (DQ, DM);
- RESET_N can be connected to any pin (the voltage level must meet the DDR3 requirements). preferably constrained to the bank where the DDR3 interface is located to improve timing. There is no need to terminate the pin and it can be pulled down to GND through a 4.7KΩ resistor, with a provision for a capacitance to GND;
- Signals within the byte group can be freely swapped (except for specific DQS pins), and byte groups within the bank can be swapped as a whole;

- Two single-ended pins in the corresponding bank of DDR3 can be used as command/address signals.

8.2 PCB Design Description

- During PCB layout, it is necessary to include Pin Delay information and activate it during routing, as well as considering the delay time of via;
- For Flyby topology, the CK trace length should not be shorter than the DQS trace of the first die, and the length difference should not be less than 1/4 CK cycle;
- The CK differential pair's internal difference should be less than 5mil, with a control impedance difference of 100ohm. A complete reference GND layer is required, with minimized layer changes, and symmetric accompanying GND vias should be added where vias are used to change layers;
- In Flyby topology, CK trace is equal in length between two DDR chips, with the trunk trace less than 2000mil, and branch trace (including the length of via) less than 120mil;
- The command/address signal trace should be of a length according to the CK trace, with the length difference of less than 200mil;
- Command/address signals require a complete reference layer, with GND accompanying vias for ODT, CS, CKE via. For others signals, there is at least one GND via next to every 3 to 6 command/address signals and at least one GND via next to every 3-6 signal vias for other signals;
- The DQS differential pair's internal difference should be less than 5mil, with a control impedance difference of 100Ω A complete reference GND layer is required with no more than twice layer changes, and symmetric accompanying GND vias should be added where vias are used to change layers;
- DQ signals require a complete reference layer, with at least one GND via accompanying every 2-4 signal vias;
- Within the same DQS byte group, the trace difference is controlled to be less than 50mil based on DQS, with a total length controlled within 1500mil;
- Traces for different DQS byte groups can be designed in unequal lengths of 200-300mil to reduce SSN impact; for example, groups 0 and 2 are of standard length, while groups 1 and 3 are 200mil longer in trace;
- Signals in the same group should be routed on the same layer to avoid signal timing being affected by changing layers. If layer changes are necessary, ensure the traces before and after the change are equal in length and try to avoid tracing on the surface;

- For serpentine wrapping, route single trace at 3W (where W is the trace width) and differential trace at 5W. Ensure that the spacing within each signal group is not less than 3H (where H is the distance from the trace to the main reference plane), the spacing between groups is not less than 5H, and the distance from DQS and clock to other signals is greater than 5H;
- The DDR power supply plane should be as large and wide as possible, with a target impedance controlled within 0.01Ω@100M;
- Decoupling capacitors should be placed as close as possible beneath the BGA Ball, ensuring that there is at least one decoupling capacitor beneath each power pin;
- The VTT power supply has high precision requirements and significant instantaneous current, necessitating the use of sufficient decoupling capacitors. VTT is concentrated at the termination resistors at the end, typically with copper plating on the surface facing the termination resistors, with a copper width greater than 120mil;
- The VREF power supply requires high precision, but power consumption is small, thus requiring less decoupling capacitors. VREF needs to be kept away from sources of interference;
- ZQ calibration resistors with 1% precision should be placed close to the corresponding pins, with widened traces and trace lengths less than 100mil.

Chapter 9 Other Descriptions

9.1 Clock Input Pin Description

Table 9-1 Logos2 Family FPGA Clock Input Pin Description

Pin	Pin Type	Direction	Pin Description
GMCLK	Clock multiplexing	Input	Multiplexed global multi-regional clock input pins; these clocks with input capability can directly drive regional clock buffers, IO clock buffers, global clock buffers, GPLL, and PPLL. They can also drive multi-regional clock buffers; when not used as clock inputs, they function as general IO. When the differential pair is connected to a single-ended clock source, only the P side of the differential pair is connected. When these pins are used as a single regional clock source, they can drive all IO clock buffers and regional clock buffers of this bank.
GSCLK	Clock multiplexing	Input	Multiplexed global single-regional clock input pins; these clocks with input capability can directly drive regional clock buffers, IO clock buffers, global clock buffers, GPLL, and PPLL. When not used as clock inputs, they function as general IO. When the differential pair is connected to a single-ended clock source, only the P side of the differential pair is connected. It can drive all IO clock buffers and regional clock buffers of this bank.

9.2 Other Special Pin Descriptions

Table 9-2 Logos2 Family FPGA Special Pin Description

Pin	Pin Type	Direction	Pin Description
VREF	Multi-function	N/A	As an input reference voltage pin. When an external reference voltage pin is not needed, it can function as user IO. For the usage of this pin when using DDR3, please refer to DDR3 Design Description.
VCCB	Dedicated	N/A	The backup battery supply voltage for the key memory is 1.0V~1.9V; when the key function is not in use, this PIN needs to be connected to ground or VCCA.

Notes:

1. For the usage instructions of TSDP/TSDN pins, please refer to the "***UG040009 Logos2 Family FPGAs Analog-to-Digital Converter (ADC) Module User Guide***".

9.3 Output Pin Description

Do not choose two single-ended pins in the bank for clock output pins. Most of the chip pins are in differential pairs. When one pin of the differential pair is used for clock output, it is recommended not to use the other pin of the differential pair as an input pin for general signals.

9.4 Pin Constraints Confirmation

After completing the schematic, run the project files to confirm whether the pin signal definitions are reasonable.

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