Compa Family PCB Design

User Guide

(UG030009, V1.1)

(16.10.2023)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.1	16.10.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
PCB	Printed Circuit Board
BGA	Ball Grid Array
FBG	F=1.0mm ball pitch, B= Ball Grid Array, G=Pb free
MBG	M=0.8mm ball pitch, B= Ball Grid Array, G= Pb free
SSBG	S=Special S=0.5mm ball pitch, B= Ball Grid Array, G= Pb free
UWG	U=0.4mm ball pitch, W= Wafer level chip scale package, G= Pb free
LPG	L=package thickness >1.2mm, P= QFP(Quad flat package) , G= Pb free

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Chapter 1 Overview

The Compa Family PCB Design User Guide is the recommended hardware design documentation for the Compa Family CPLD chips.

For details on Compa Family CPLD general introduction, device features , package information, and number of user IOs, please refer to "***DS03001_Compa Family CPLDs Device Datasheet***".

Chapter 2 Power

2.1 Voltage

The requirements on operating voltage are described in Table 2-1.

Table 2-1 Recommended Device Operating Conditions

Voltage	Description	Min.	Typ.	Max.
VCC[1]	Power supply voltage for L-type devices	1.14 V	1.2 V	1.26 V
	Power supply voltage for G-type/ D-type devices	2.375 V	2.5V/3.3 V	3.465 V
VCCIO[1,2]	I/O Bank voltage	1.14 V	--	3.465 V

Notes:

1. All power supply pins must be connected to the corresponding external power source;

2. The VCCIO pins of unused I/O Banks should be connected to VCC;

3. There are no requirements for power-up sequence; simultaneous power-up is allowed;

4. Power supply ripple must be within ±5% of the nominal voltage;

5. During device power-down, if the pull-up power supply externally connected to the bidirectional or unidirectional output IO does not power-down or there is a high-voltage input, it will cause current to backflow from the pad to the VCCIO power supply. This backflow will not affect the device's reliability. If the device completes the power-down process, then this backflow path is closed. If the VCCIO power supply of the device is combined with the VCC power supply, there might be residual voltage on VCC that prevents the device from fully power-down, causing the device and its IO to be in an abnormal operating state. In this scenario, users can choose one of the following methods for improvement: (1) Turn on the OPEN DRAIN function of the IO for applications that meet OPEN DRAIN scenarios; (2) Select VCCIO as the external pull-up power source or turn off high- voltage inputs during power-down; (3) V_{CC} and V_{CCIO} provides power separately.

Table 2-2 Device Power Supply Voltage Range

Power Supply Type / Chip Model	V_{CC}	V_{CCIO0}	V_{CCIO1}	V_{CCIO2}	V_{CCIO3}	V_{CCIO4}	V_{CCIO5}
PGC1KL_UWG36	1.2 V	1.2V-3.3 V[1]	--[2]	1.2V-3.3 V	1.2V-3.3 V	--	--
PGC2KL_UWG49	1.2 V	1.2V-3.3 V	--	1.2V-3.3 V	--	--	1.2V-3.3 V
PGC2KL_SSBG256	1.2 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC4KL_UWG81	1.2 V	1.2V-3.3 V	--	1.2V-3.3 V	1.2V-3.3 V	--	1.2V-3.3 V
PGC4KL_SSBG256	1.2 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC1KG_LPG100	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC1KG_LPG144	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC1KG_MBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC1KG_FBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC2KG_LPG100	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC2KG_LPG144	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V

Power Supply Type / Chip Model	V_{CC}	V_{CCIO0}	V_{CCIO1}	V_{CCIO2}	V_{CCIO3}	V_{CCIO4}	V_{CCIO5}
PGC2KG_MBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC2KG_FBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC4KD_MBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC4KD_MBG324	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC4KD_MBG332	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC4KD_MBG400	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC7KD_FBG484	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC7KD_MBG400	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC7KD_MBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC7KD_MBG332	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC7KD_LPG144	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V

Notes:

1. The 1.2V-3.3V voltage range includes 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V; the same below;
2. “--” It indicates that the corresponding chip does not have this Bank.

2.2 Power Consumption

Table 2-3 provides measured core current values for different CPLD devices as a reference for PCB design, and power consumption can also be assessed using the power evaluation software PPP. The current of the BANK is related to the packaging and can be evaluated using the power evaluation software PPP.

Table 2-3 Core Current of Compa Family Devices

Device	Resource Usage Rate	Core Current
1KL	80%, system clock at 125MHz	70mA
1KG	80%, system clock at 150MHz	80mA
2KL	80%, system clock at 125MHz	130mA
2KG	80%, system clock at 150MHz	150mA
4KL	80%, system clock at 125MHz	210mA
4KD	80%, system clock at 150MHz	260mA
7KD	80%, system clock at 150MHz	370mA

2.3 Power Trace

Power and ground trace should be short and thick, and it is recommended to design them in a plane form if conditions allow.

The chip's power supply pins and ground pins should be decoupled, with the decoupling capacitors placed as close as possible to the chip pins. It is advisable to place a 0.1uF decoupling capacitor at each power supply pin, one or two 10uF capacitors at each bank power supply, and one or two 10uF or one or two 22uF capacitors at the core power supply. Please refer to Figure 2-1 for reference.

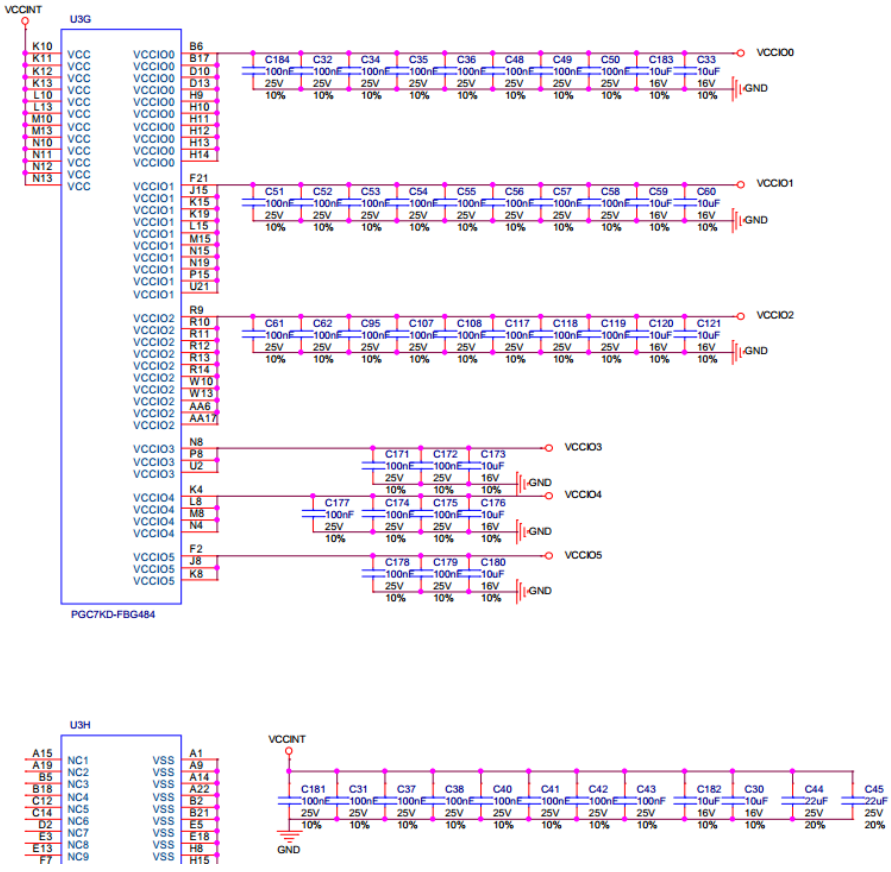

Figure 2-1 PGC Family CPLD Power Decoupling Diagram

Figure 2-2 is an actual PCB showing the placement of capacitors in a PGC7KD-MBG400.

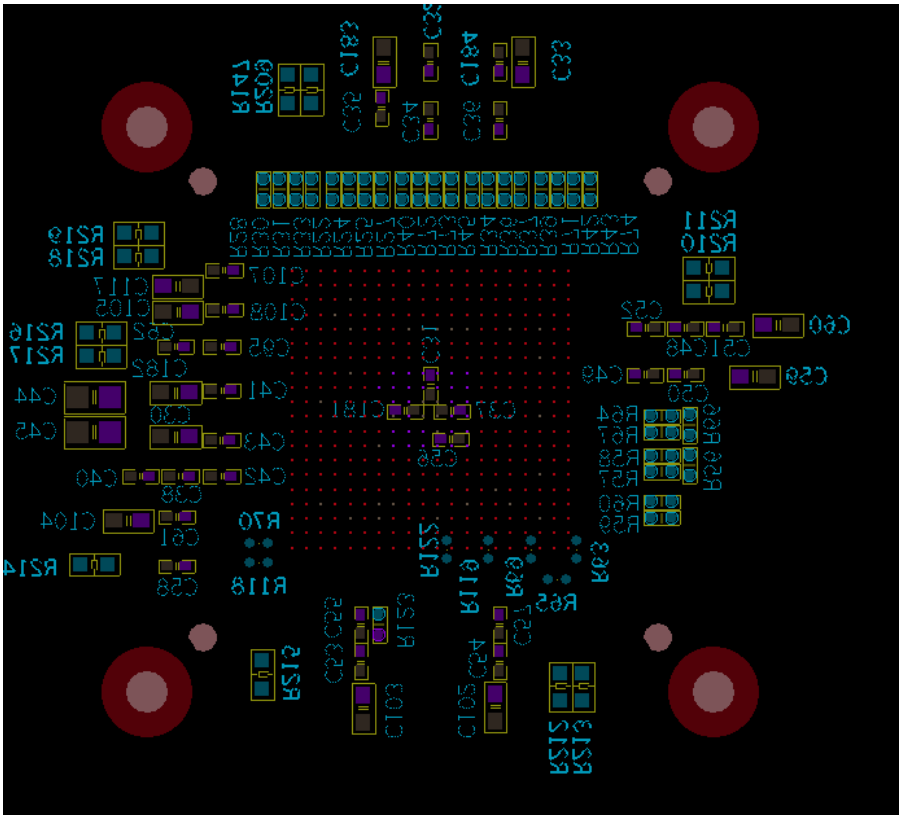

Figure 2-2 An Actual PCB Showing the Placement of Capacitors in a PGC7KD-MBG400.

Chapter 3 Package and FANOUT

The PCB pad diameter is generally designed to be the same as the CPLD ball diameter, but can be 20%-25% smaller in special cases. Below is a reference diagram for Fanout.

The details are shown in Figure 3-1. The central "cross" divides the BGA into 4 equal regions, with the fanout trace in each region extending outward from the BGA. The position of the "cross" can be asymmetrically adjusted as required for fanout. The cross can be used in the middle layers for power trace and trace with larger trace spacing, and in the bottom layer for placing filter capacitors. The 2 outermost rows of pads can be routed directly from the chip soldering surface, while the inner rows of pads should be routed outward in a radial pattern after layer change through via. Power trace and ground trace should be widened.

The number of traces between the surface pads should be maximized, yet it is crucial to avoid lengthy traces to prevent PCB processing defects and issues with surface mounting.

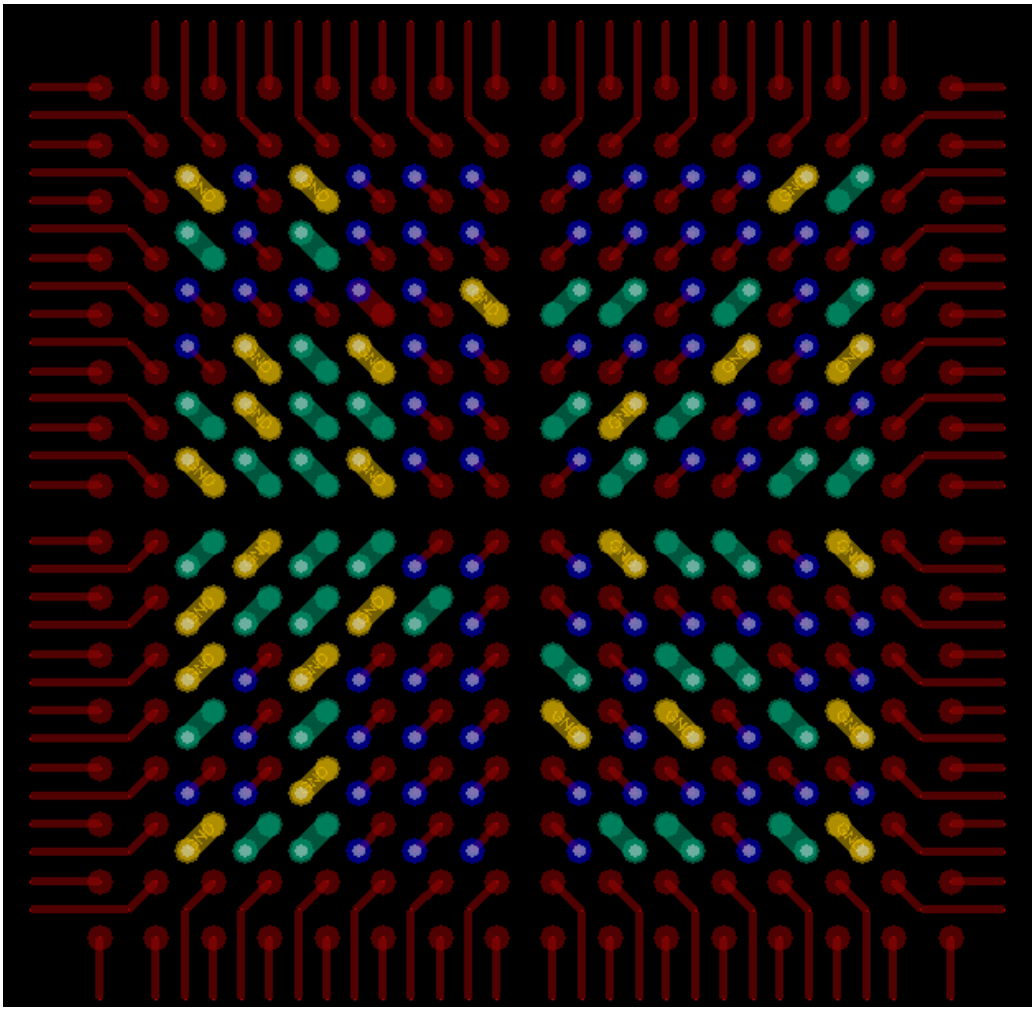

Figure 3-1 BGA Fanout Reference Diagram

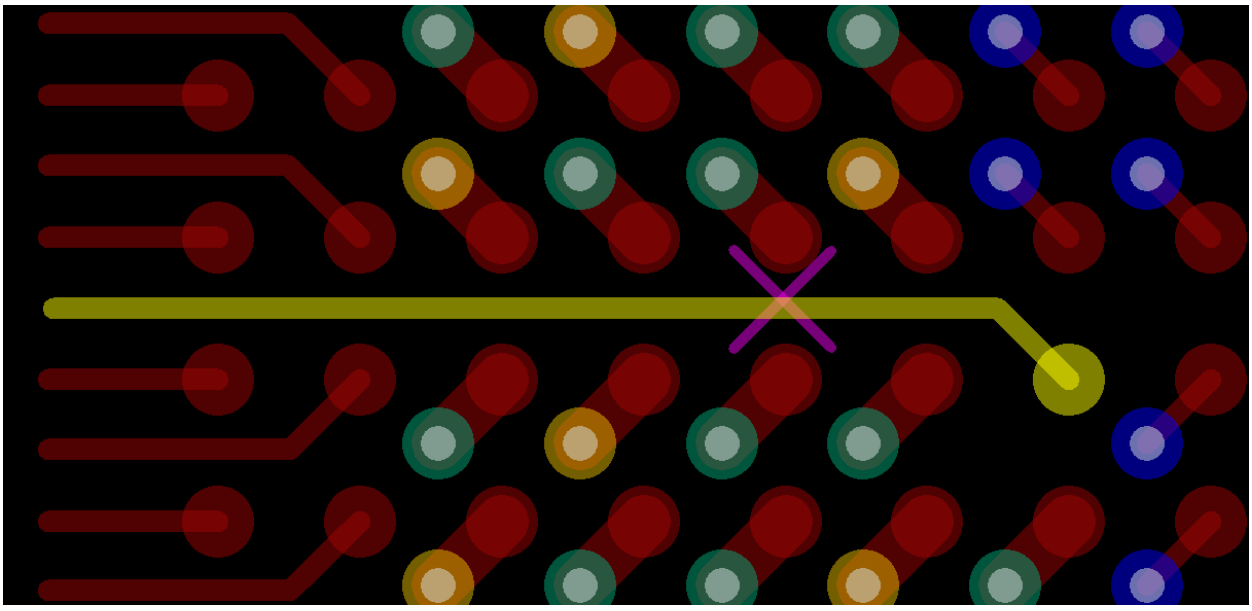

Figure 3-2 Diagram of Long Traces Between BGA Surface Pads

Long traces (yellow traces) between surface pads increase the risk of shorts between the traces and pads, and should be avoided.

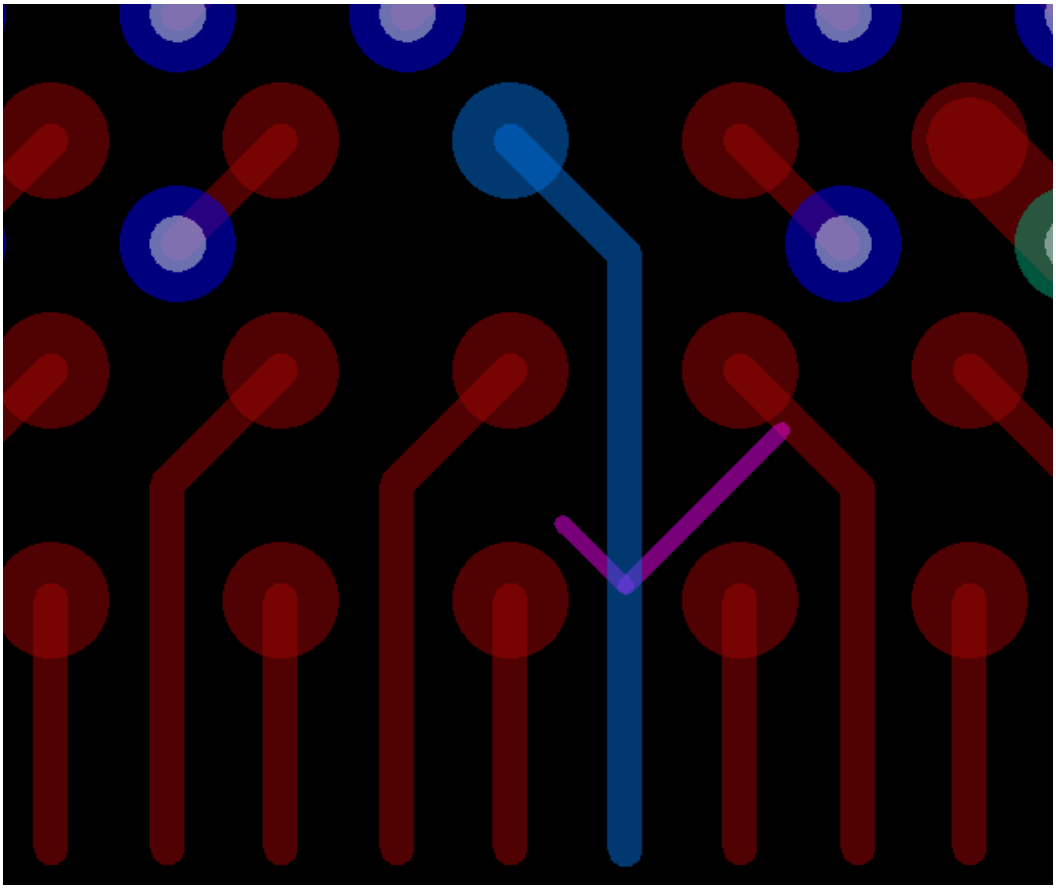

Figure 3-3 BGA Surface Routing Diagram

The 3rd row may have a pad with a trace (blue trace) leading out from the gap in the middle cross of the Fanout.

3.1 FBG

The Compa family CPLD currently has 2 types of FBG packages, FBG256 and FBG484, with a pad pitch of 1.0mm. For details on packages, please refer to the corresponding Packaging Manual.

The recommended pad and via sizes, and trace widths are as follows:

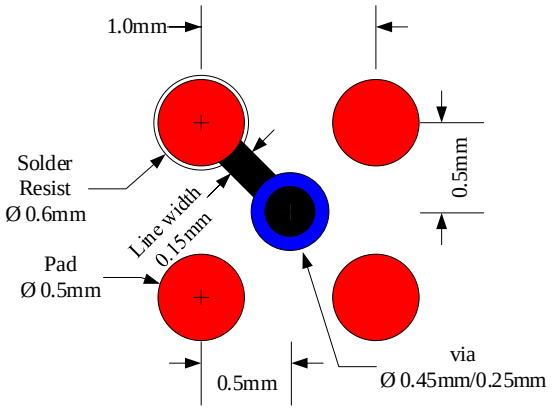

Figure 3-4 Diagram of Recommended FBG Packaging Pad and Via Sizes

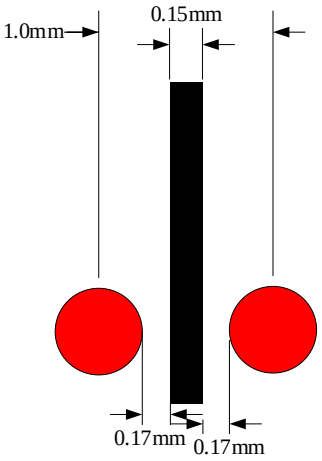

Figure 3-5 Diagram of Recommended Trace Sizes Between FBG Packaging Pads

3.2 MBG

The Compa family CPLD currently has 4 types of MBG packages, MBG256, MBG324, MBG332, and MBG400, with a pad pitch of 0.8mm. For details on packages, please refer to the corresponding Packaging Manual.

The recommended pad and via sizes, and trace widths are as follows:

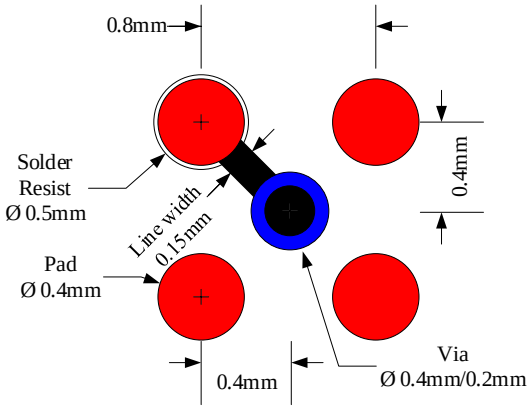

Figure 3-6 Diagram of Recommended MBG Packaging Pad and Via Sizes

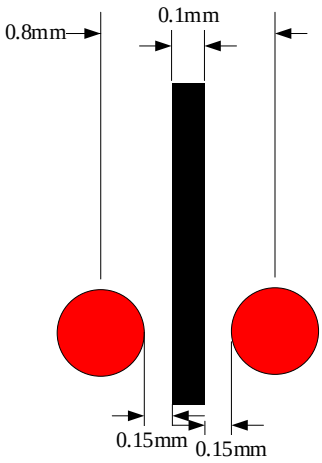

Figure 3-7 Diagram of Recommended Trace Sizes Between MBG Packaging Pads

3.3 SSBG

The Compa family CPLD currently only has 1 type of SSBG package, SSBG256, with a pad pitch of 0.5mm. For details on packages, please refer to the corresponding Packaging Manual.

The SSBG package has a small pad pitch, with insufficient space for traces between the pads, generally requiring the use of blind and buried vias in PCB design. When a smaller number of pins are used, through-hole vias can be employed if the pin position planning is reasonable, with the vias drilled directly on the pads.

Recommended pad and via sizes are as follows:

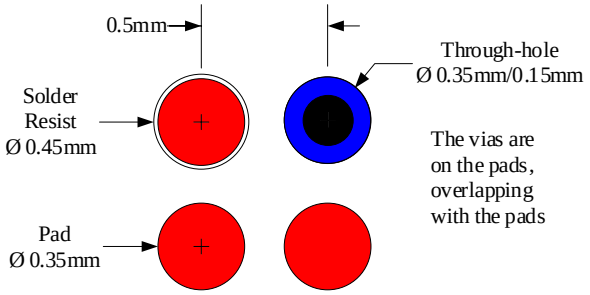

Figure 3-8 Diagram of Recommended SSBG Packaging Pad and Via Sizes

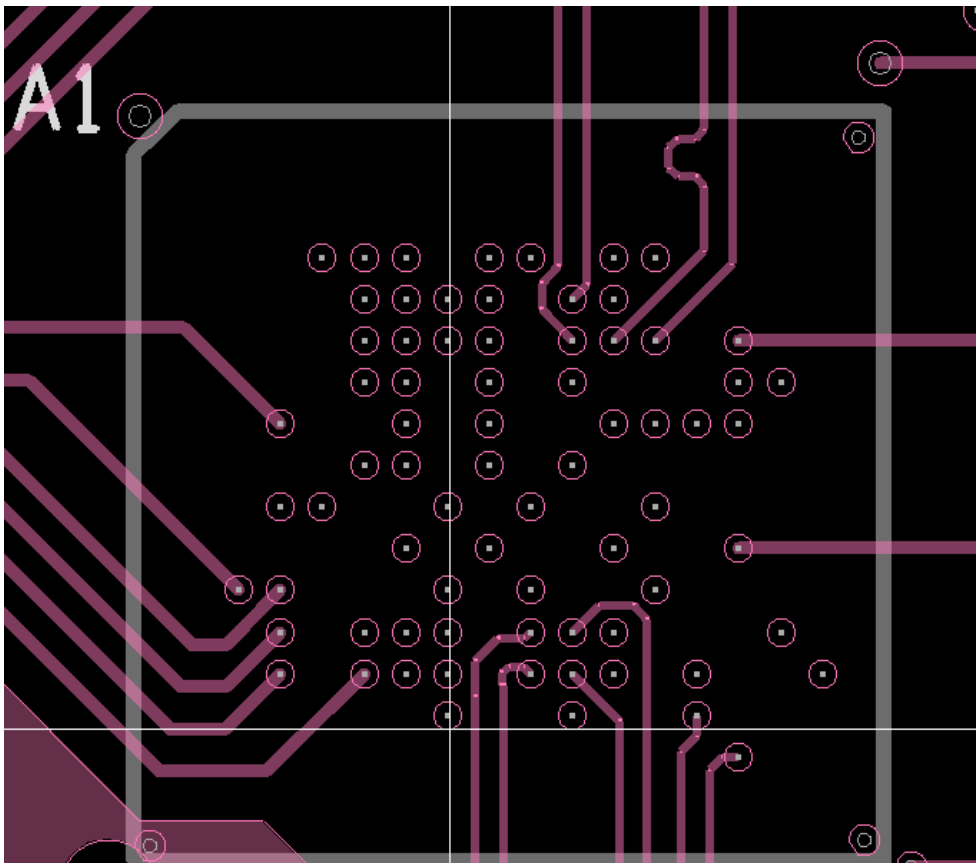

Figure 3-9 Routing Diagram 1 of PCB Inner Layer Corresponding to SSBG Package

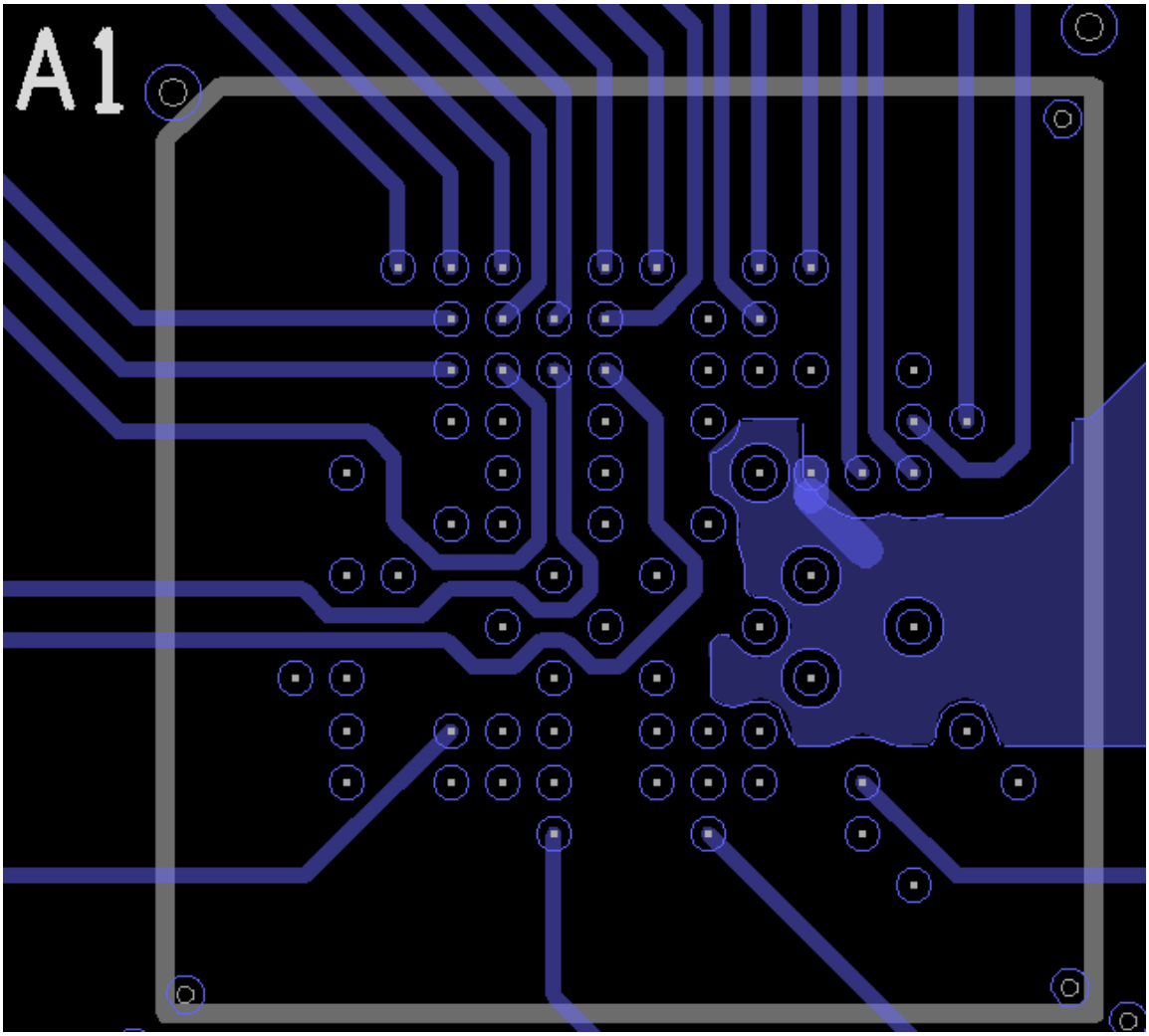

Figure 3-10 Routing Diagram 2 of PCB Inner Layer Corresponding to SSBG Package

3.4 UWG

The Compa family CPLD currently has 3 types of UWG packages, UWG36, UWG49, and UWG81, with a pad pitch of 0.4mm. For details on packages, please refer to the corresponding Packaging Manual.

The UWG package has a small pad pitch, with insufficient space for traces between the pads (with the exception of 2-layer flexible PCBs), generally requiring the use of blind and buried vias in PCB design.

Recommended pad and via sizes are as follows:

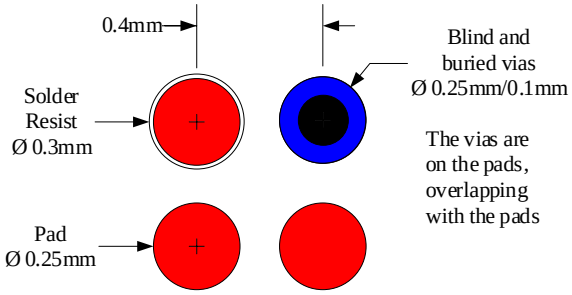

Figure 3-11 Diagram of Recommended MBG Packaging Pad and Via Sizes

For the UWG package, if a flexible board is used for PCB design, it is recommended that pad diameters be 0.2mm (including solder mask and solder layer both at 0.2mm), with a suggested trace width of 0.06mm, and a spacing of 0.06mm between traces and between traces and pads. The power traces should be appropriately widened after leading out. Differential traces should adhere to the principle of maintaining equal length and equal distance. An example of PCB design for UWG package is shown in Figure 3-12 below.

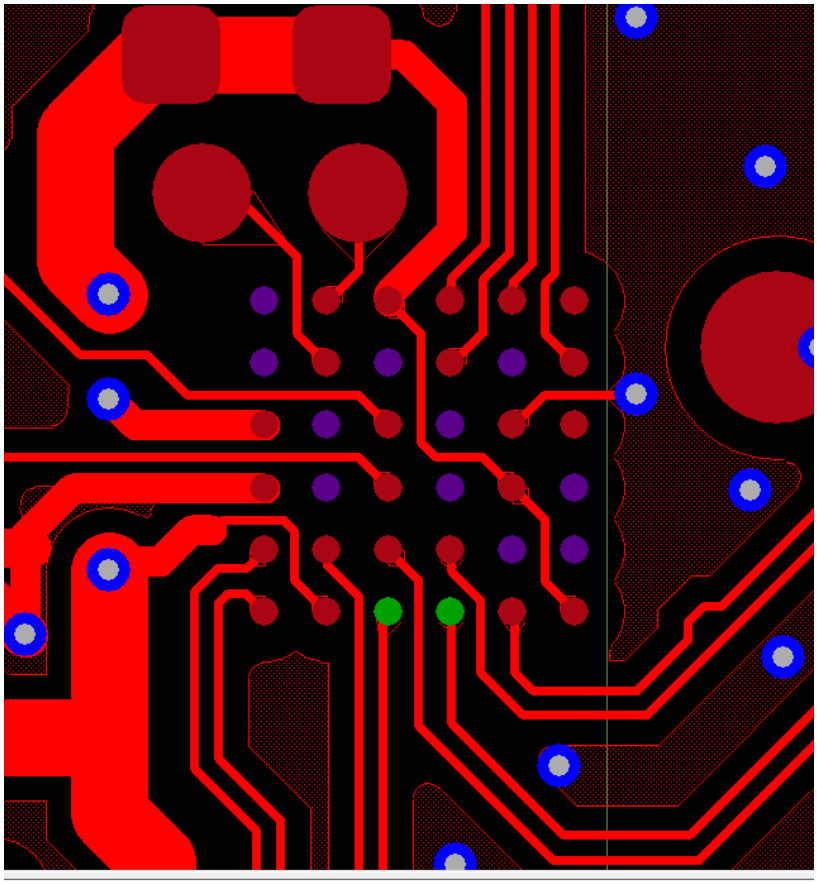

Figure 3-12 Diagram of Recommended UWG Packaging Pad and Via Sizes

3.5 LPG

The Compa family CPLD currently has two types of LPG packages, LPG100 and LPG144, both with a pad pitch of 0.5mm. For details on packages, please refer to the corresponding Packaging Manual.

LPG packaging is in the form of Quad Flat Package (QFP), with PCB packaging and trace designed according to QFP requirements.

Chapter 4 Configuration

For related configuration information, please refer to "***UG030004_Compa family CPLDs Configuration User Guide***". Additionally.

4.1 Configuration Pin Description

There are detailed descriptions on chip pins in the chip package documentation. In Table 4-1 below, some usage instructions for configuration pins that require special attention during PCB design are given.

Table 4-1 Compa Family CPLD Chip Configuration-Related Pin Usage Instructions

Pin Name	Pin Type	Usage Instructions
INIT_FLAG_N	Multi-Function Pin	When used as an initialisation complete indication signal, it is recommended to add an external pull-up resistor of 4.7KΩ to the power supply of the respective bank; It cannot drive an indicator light directly and should be driven through a triode or MOSFET;
CFG_DONE	Multi-Function Pin	When used as a configuration complete indication signal, it is recommended to add an external pull-up resistor of 4.7KΩ to the power supply of the respective bank; It cannot drive an indicator light directly and should be driven through a triode or MOSFET.
RSTN	Multi-Function Pin	When used for chip reset functionality, it is necessary to add an external pull-up resistor of 4.7KΩ to the power supply of the respective bank.
CFG_CLK	Multi-Function Pin	When using the Master SPI mode, it is required to add an external pull-up resistor of 1KΩ to the power supply of the respective bank.
TCK	Multi-Function Pin	It is required to externally pull down a 4.7KΩ resistor to ground.
JTAGEN	Multi-Function Pin	When the JTAG port is disabled, JTAGEN can be used as a dedicated pin. When the JTAGEN input receives logic 1, the JTAG port is enabled and acts as the configuration port. In this scenario, it is recommended to add an external pull-up resistor of 4.7KΩ to the power supply of its respective bank. When the JTAGEN input is set to logic 0, the 4 I/Os of the JTAG port act as user I/Os. In this scenario, it is recommended to add an external pull-down resistor of 4.7KΩ to the ground.

4.2 JTAG

In JTAG, the maximum operating frequency of the TCK signal is 50MHz, it is required to externally pull down a 4.7KΩ resistor to the ground. When using a backplate or other situations requiring bifurcating the JTAG signal into two, a series resistor should be connected to TCK to reduce the impact of stubs on the signal. As shown in Figure 4-1, resistors R1 and R2 are close to the signal bifurcation point.

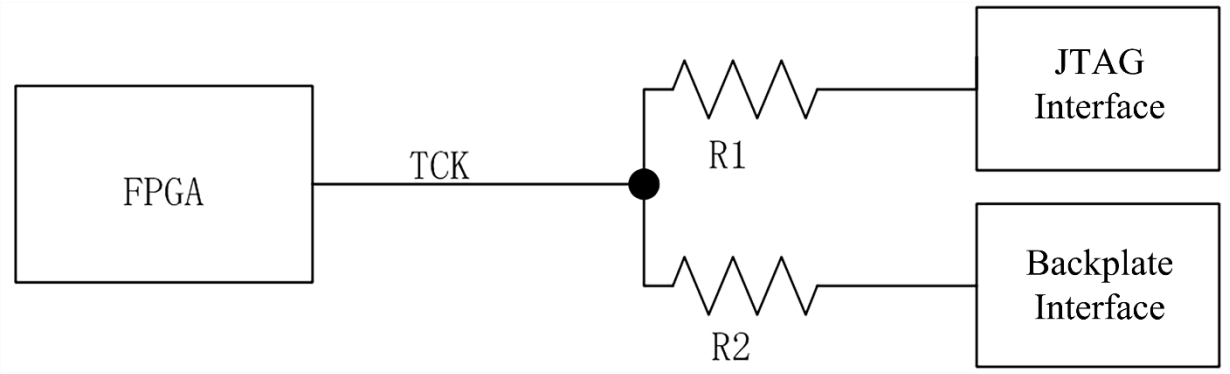

Figure 4-1 Diagram of JTAG Signal Bifurcating Resistors

4.3 SPI

When using the SPI configuration mode, It is recommended to connect a resistor in series with the source end of the SCK signal.

When using the Master SPI mode, for the CFG_CLK, it is recommended to externally pull up a 1KΩ resistor to the power supply of its bank. For the external SPI Flash chip select signal FCS_N, it is recommended to add an external pull-up resistor of 4.7KΩ to the power supply of its bank, ensure that the voltage of the bank with the SPI signals is consistent with the voltage of the Flash chip.

When using the Slave SPI mode, ensure that the voltage of the bank with the SPI signals is consistent with the port level of the master device.

4.4 Other Configuration Pins

Other commonly used configuration pins include RSTN, INIT_FLAG_N, and CFG_DONE. These pins are multi-function pins and the considerations for their use are explained in Table 4-1.

When multiplexing pins are used as general IO, it is necessary to ensure that they are not affected by circuits other than the configuration circuit during power-up configuration, and it is recommended to use them only for low-speed signal output.

When using IIC configuration mode, SCL and SDA require external pull-up resistors, with a recommended resistance of 2.2KΩ.

Chapter 5 LVDS

5.1 Chip Pin Selection Requirements

For the requirements of LVDS for the Compa family CPLD, please refer to "***DS03001_Compa Family CPLDs Device DataSheet***".

5.2 LVDS Routing Requirements

- The transmitter chip should be as close to the receiver chip as possible to minimize the length of the LVDS trace, with 45 °or arc trace corner;
- Differential trace impedance is 100ohm ±10%, the termination resistors should be close to the receiver, minimizing the distance to the receiver pins, and internal termination resistors at the receiver are preferred;
- Minimize the number of vias, with a recommendation of no more than two vias per trace;
- Traces should have a complete reference ground plane;
- All differential pairs within the same group are routed on the same layer;
- When changing signal layers, if the reference plane is also changed, the reference plane requires a via for layer change, and it should be adjacent to the signal via;
- The spacing between different differential pair traces must be greater than 5 times the trace width, and the spacing between differential traces and other signal traces must be greater than 5 times the trace width;
- The two traces within a differential pair should be strictly equal in length, with a length mismatch not exceeding 5mil; differential pairs within the same group should be equal in length, with a mismatch not exceeding 20mil; the principle for length compensation is to compensate where the mismatch occurs;
- For long LVDS traces with rate transmission requirements, the loss can be optimized through simulation, especially the loss caused by impedance discontinuities at PCB vias and connectors.

Chapter 6 MIPI

6.1 Chip Pin Selection Requirements

The Compa family CPLD supports MIPI input and output.

MIPI_Ctrl is the control pin for high-performance MIPI applications, When the pin is connected to a 2.5V or 3.3V source, the device supports high-performance MIPI; when it is connected to VSS or left floating, the device does not support high-performance MIPI. This pin is present in the PGC1KL\PGC2KL\PGC4KL device, but it is not present in the PGC1KG\PGC2KG\PGC4KD\PGC7KD device.

MIPI receive pins must select the odd-numbered differential pairs with differential ordering in Bank2 (as IDDRx4 is used in recommended applications, if IDDRx2 is used, this restriction is not necessary), with a Bank voltage of 1.2V. Using MIPI standard, unidirectional HS-MIPI input and bidirectional LP-MIPI can be achieved. The MIPI receiver is recommended to use a 2-wire arrangement, where unidirectional HS-MIPI input and bidirectional LP-MIPI share the same pair of I/O. At this time, internal termination resistors in the chip are needed.

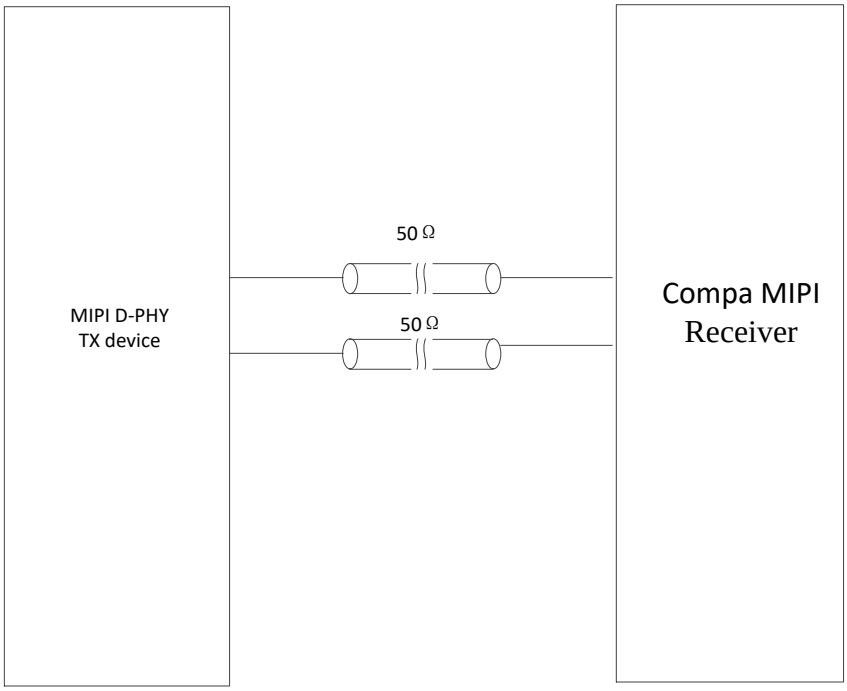

Figure 6-1 MIPI Input Diagram

The MIPI transmitter of the Compa family CPLD uses the LVCMOS25D standard with external resistors in a 4-wire scheme, implementing HS-MIPI and LP-MIPI outputs through 4 I/Os. The 2 I/Os corresponding to HS-MIPI output use LVCMOS25D standard, placed in Bank0 with a Bank voltage of 2.5V; the 2 I/Os corresponding to LP-MIPI output use LVCMOS12 standard, which are single-ended signals, and matching resistors need to be placed in pairs to minimize the impact on differential traces, with a corresponding Bank voltage of 1.2V.

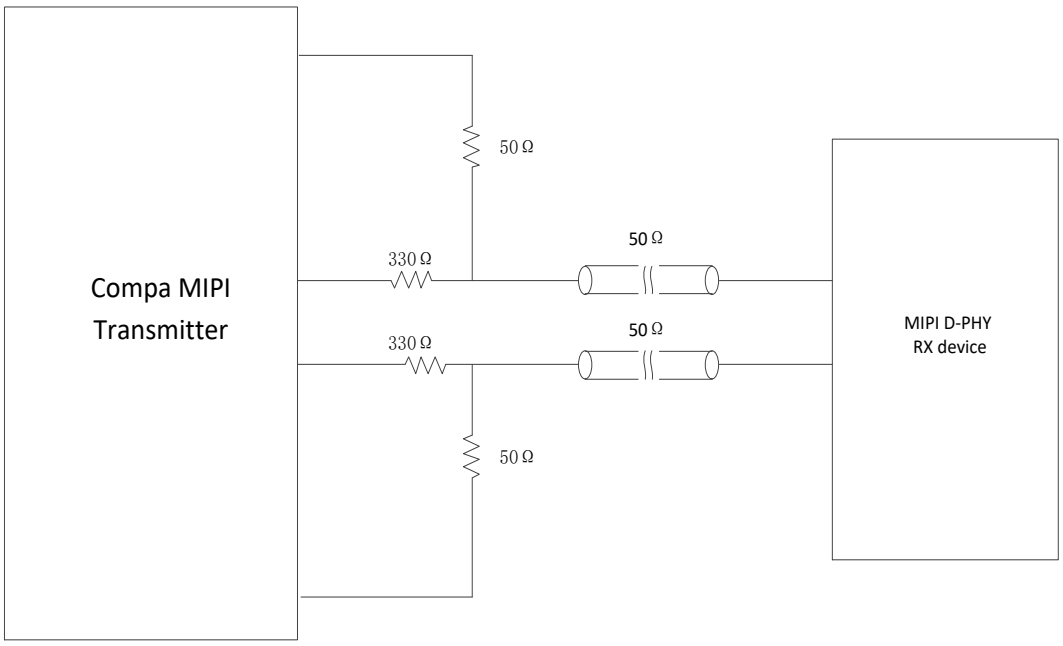

Figure 6.1.4 4-Wire MIPI Output Circuit Diagram

6.2 Routing Requirements

PCB trace shall be designed to ensure that 50 ohm discrete resistors have minimal impact on the differential traces, and route the low-speed signal trace in the 4-wire scheme as normal single-end signal traces. Other requirements are the same as those for LVDS trace.

Chapter 7 Pseudo-Differential Output

In applications of the Compa family CPLD, differential outputs such as LVPECL33, MLVDS, LVDS25E, and BLVDS require external resistors for connection. For diagrams and relevant descriptions, please refer to "***UG030005_Compa Family CPLDs Input/Output Interface (IO) User Guide***".

Chapter 8 Clock

8.1 Clock Pin

The Compa family CPLD features a number of global clock input pins and PLL clock input pins, supporting single-ended or differential inputs. For single-ended clock inputs, selecting the P side of the global clock differential pair ensures that the clock signal routes through the global clock dedicated traces. The input of oscillator clock and the synchronous clock will be connected into these pins. The output reference clock is not required to be connected to these dedicated pins. Moreover, these pins may be used as general I/O ports. The clock input pins can be referenced to the pin descriptions in the package user guide.

8.2 Clock Trace

- The clock circuit should be placed away from the edge of the board, with trace kept distant from signal trace to avoid running parallel with other signal trace.
- When the clock trace is shielded with a ground net, vias shall be set on the ground plane at regular intervals for the shield trace.
- Clock trace should have a complete reference ground plane with minimized layer changes.
- There should be ground vias next to clock vias, and a complete reference ground plane should be present after changing layers.
- Clock trace should maintain continuous impedance and avoid cross splits.
- Reserve a position for a series resistor at the source end of the clock trace.

8.3 Clock Edge

The maximum rise and fall times of the clock input signal depend on the system application; they vary with different system and device noises as well as timing margins on the interface. Due to this dependency, the Compa family CPLD cannot display the specific maximum rise and fall times of the clock input signal.

For clock input signals, slow clock edges can absorb a significant amount of switching noise from the PCB and the device itself, leading to glitches on the signal edges. To minimize noise effects on clock edges, the rise and fall times of the clock input signals should be kept as short as possible.

Chapter 9 Other Considerations

After FPGA pins are assigned, it is recommended that users use PDS software to confirm pin assignments.

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