Logos Family FPGAs Datasheet

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Revisions History

Document Revisions

Version	Date of Release	Description
V3.0	16.03.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
CLM	Configurable Logic Module
DRM	Dedicated RAM Storage Module
HMEMC	Hard IP Memory Controller, including DDRC and DDR PHY
DDRC	Double Data Rate Controller
DDR	Double Data Rate Synchronous Dynamic Random Access Memory
ADC	Analogue to Digital Converter
PLL	Phase Locked Loop
ESD	Electro Static Discharge
RAM	Random Access Memory
LVDS	Low Voltage Differential Signaling
HSTL	High-Speed Transceiver Logic
SSTL	Stub Series Terminated Logic
UID	Unique Identification
UI	Unit Interval
HSST	High-Speed Serial Transceiver
PCIe	Peripheral Component Interconnect Express

Related Documentation

The following documentation is related to this manual:

1. ***UG020001_Logos Family FPGAs Configurable Logic Module (CLM) User Guide***
2. ***UG020002_Logos Family FPGAs Dedicated RAM Module (DRM) User Guide***
3. ***UG020003_Logos Family FPGAs Arithmetic Processing Module (APM) User Guide***
4. ***UG020004_Logos Family FPGAs Clock Resources (Clock) User Guide***
5. ***UG020005_Logos Family FPGAs Configuration User Guide***
6. ***UG020006_Logos Family FPGAs Input/Output Interface (IO) User Guide***
7. ***UG020009_Logos Family FPGAs Analogue-to-Digital Converter (ADC) Module User Guide***
8. ***UG0200011_Logos Family Products HMEMC Use Case User Guide***
9. ***UG0200013_Logos Family FPGAs High-Speed Serial Transceiver (HSST) User Guide***

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This document mainly includes an overview of the features, product models and resource scale list, AC and DC characteristics of the Logos family FPGA devices from Shenzhen Pango Microsystems Co., Ltd. (hereinafter referred to as Pango Microsystems). It enables users to understand the features of the Logos family FPGAs devices, facilitating device selection.

The -5 parameters in this document apply only to the current PGL25G device.

Chapter 1 Overview of Logos Family FPGAs

Logos family programmable logic devices are brand-new low-power, low-cost FPGA products launched by Shenzhen Pango Microsystems Co., Ltd., featuring a full intellectual property architecture and mainstream 40nm process technology. The Logos Family FPGAs include innovative Configurable Logic Modules (CLM), dedicated 18Kb storage unit (DRM), Arithmetic Processing Units (APM), multi-function high-performance I/Os, extensive on-die clock resources and other modules. It also integrates hard core resources such as the Memory Controller (HMEMC) and Analogue-to-Digital Converter (ADC) modules, supports various configuration modes, and provides functions like Bit stream Encryption and Device Unique ID (UID) to secure user's design. Based on the above functions, the Logos Family FPGAs are widely applicable to various application areas such as video, industrial control, automotive electronics, and consumer electronics.

1.1 Features of Logos Family FPGAs Products

- **Low-cost and Low-power Consumption**
  - Low power consumption, mature 40nm CMOS process
  - Core voltage down to 1.1V
- **IO with Multiple Standards**
  - Up to 498 user IOs, supports 1.2V, 1.5V, 1.8V, 2.5V, 3.3V I/O standards
  - HSTL, SSTL memory interface standards supported
  - MIPI D-PHY interface standard supported
  - LVDS, MINI-LVDS, SUB-LVDS, SLVS (MIPI two-wire level standard), TMDS (applicable for HDMI, DVI interfaces) and other differential standards supported
  - Programmable IO BUFFER, high-performance IO LOGIC
- **Flexible Programmable Logic Module CLM**
  - LUT5 logic architecture
  - Each CLM contains 4 multi-function LUT5s and 6 registers
  - Fast arithmetic carry logic supported
  - Distributed RAM mode supported
  - cascade chains supported

➢ **DRM with Multiple Write Modes**

- A single DRM provides 18Kb of memory space, configurable as 2 independent 9Kb storage blocks
- Various working modes supported, including single-port (SP) RAM, dual-port (DP) RAM, simple dual-port (SDP) RAM, ROM, and FIFO mode
- Dual-port RAM and simple dual-port RAM support mixed bit width for both ports
- Three write modes: Normal-Write, Transparent-Write, and Read-before-Write[1]
- Byte Write function supported

➢ **Efficient Arithmetic Processing Unit (APM)**

- Each APM supports one 18*18 operation or two 9*9 operations
- Input register and output register supported
- 48-bit Post-adder supported
- "Signed" and "Unsigned" data operations supported

➢ **Integrated Hard Core Memory Controller HMEMC**

- DDR2, DDR3, LPDDR supported
- A single HMEMC supports x8, x16 data widths
- Standard AXI4 bus protocol supported
- DDR3 write leveling and DQS gate training supported
- DDR3 rate up to 800Mbps

➢ **Integrated ADC Hard Core**

- 10bit resolution, 1MSPS (independent ADC operation) sampling rate
- Up to 12 input channels
- Integrated temperature sensors

➢ **Extensive Clock Resources**

- 3 types of clock networks supported, configurable with flexibility
- Region-based global clock network
- Each region has 4 regional clocks, supports vertical cascading
- High-speed IO clock, supports IO clock division
- Optional data address hold, output registers
- Integrates multiple PLLs, each PLL supports up to 5 clock outputs

➢ **Flexible Configuration Methods**

- Multiple programming modes supported
- JTAG mode Compliant with IEEE 1149.1 and IEEE 1532 standards
- Master SPI can select up to 8bit data width, effectively increasing programming speed
- BPI x8/x16, Slave Serial, Slave Parallel modes supported
- AES-256 bit stream encryption supported[2], supports 64bit UID protection
- Supports SEU error detection and correction
- Supports multi-version bit stream fallback function
- Supports watchdog timeout detection
- Supports programming/downloading
- Supports internal debugging

- **High-performance High-speed Serial Transceiver HSST**
- Data Rate up to 6.375Gbps supported
- Flexibly configurable PCS supports protocols such as PCIe GEN1/GEN2, Gigabit Ethernet, CPRI, SRIO, etc.

Note

1: Does not support configuring both ports to Read-before-Write mode simultaneously.

2: PGL25G does not support AES-256 bit stream encryption.

1.2 Logos Family FPGAs Resource Scale and Packaging Information

The resource scale and packaging information of the Logos Family FPGAs are as shown in Table 1-1 and Table 1-2.

Table 1-1 Logos FPGA Resource Count

Device	CLM[1,2]				18Kb DRM (units)	APM (units)	PLL (units)	ADC (units)	HME MC (units)	MAX USER IO (units)	HSST LANE	PCIE GNE2 X4 CORE
	LUT5 (units)	Equivalent LUT4 (units)	FF (units)	Distributed RAM (bits)								
PGL12G	10400	12480	15600	84480	30	20	4	1	0	160	0	0
PGL22G	17536	21043	26304	71040	48	30	6	1	2	240	0	0
PGL22GS[3]	17536	21043	26304	71040	48	30	6	0	0	140	0	0
PGL25G	22560	27072	33840	242176	60	40	4	0	0	308	0	0
PGL50G	42800	51360	64200	544000	134	84	5	0	0	341	0	0
PGL50H	42800	51360	64200	544000	134	84	5	0	0	304	4	1
PGL100H	85392	102470	128088	1013504	286	188	8	0	0	498	8	1

Note

1. Each CLM contains 4 multi-function LUT5s and 6 registers; each multi-function LUT5 is equivalent to 1.2 LUT4s.
2. The CLMs in the chip include CLMA and CLMS, only CLMS can be configured as Distributed RAM.
3. PGL22GS-176 includes a maximum of 140 IOs, comprising 68 differential pairs and 4 single-ended IOs; 140 MAX USER IOs indicates the number of IO pins available outside the chip, there are additional pins inside the chip for connection to SDRAM.

Table 1-2 Logos FPGA Package Information and User IO Count

Package	FBG256	FBG484	FBG900	MBG484	MBG324	LPG176	LPG144
Size (mm)	17×17	23×23	31×31	19×19	15×15	22x22	22x22
Pitch (mm)	1.0	1.0	1.0	0.8	0.8	0.4	0.5
Device	User IO	User IO	User IO	User IO	User IO	User IO	User IO
PGL12G	160	-	-	-	-	-	103
PGL22G	186	-	-	-	240	-	-
PGL22GS	-	-	-	-	-	140	-
PGL25G	186	308	-	-	226	-	-
PGL50G	-	332	-	341	218	-	-
PGL50H	-	296	-	304	190	-	-
PGL100H	-	-	498	-	-	-	-

1.3 Brief Description of Logos Family FPGAs

1.3.1 CLM

CLM (Configurable Logic Module) is the basic logic unit of Logos Family products, mainly composed of multi-function LUT5, registers, and expansion function selectors. CLMs are distributed in columns in Logos Family products and come in two forms: CLMA and CLMS. Both CLMA and CLMS support logic functions, arithmetic functions, and register functions, but only CLMS supports the Distributed RAM function. CLMs are interconnected with each other and with other on-die resources through the signal interconnect module.

Each CLMA contains 4 LUT5s, 6 registers, multiple expansion function selectors, and 4 independent cascade chains, among others. CLMS is an extension of CLMA, adding support for Distributed RAM on top of all functions supported by CLMA. CLMS can be configured as single-port RAM or simple dual-port RAM.

1.3.2 DRM

A single DRM has 18K bits of storage unit, which can be independently configured as 2x9K or 1x18K, supporting various working modes including dual-port RAM, simple dual-port RAM, single-port RAM or ROM mode, as well as FIFO mode. DRM supports configurable data widths and supports dual-port mixed data widths in DP RAM and SDP RAM modes. For PGL12G, ROM is not supported. For detailed usage of DRM, please refer to the "Logos Family FPGAs Dedicated RAM Module (DRM) User Guide".

1.3.3 APM

Each APM consists of I/O Unit, Preadder, Mult, and Postadder functional units, supporting output from each register stage. Each APM can implement one 18*18 multiplier or two 9*9 multipliers, supporting pre-addition function; it can also implement one 48-bit Postadder or two 24-bit Postadders. The APMs of Logos FPGA support cascading, enabling applications such as filters and high-bit-width multipliers.

1.3.4 Input/Output

- **IOB**

The IOs of Logos FPGA are distributed by Bank, with each Bank powered by an independent IO

power supply. IOs are flexibly configurable, supporting 1.2V to 3.3V power supply voltages and various single-ended and differential interface standards, to accommodate different application scenarios. All user IOs are bidirectional, containing IBUF, OBUF, and tri-state control TBUF. The powerful IOBs of Logos FPGA have flexible configuration options for interface standards, Output Drive, Slew Rate, Input Hysteresis, etc. For detailed IO characteristics and usage, please refer to the "Logos Family FPGAs Input/Output Interface (IO) User Guide".

- **IOL**

The IOL module is located between the IOB and the core, managing signals to be input to and output from the FPGA Core.

IOL supports various high-speed interfaces, in addition to supporting direct data input/output and IO register input/output modes; it also supports the following functions:

- ISERDES: For high-speed interfaces, it supports 1:2; 1:4; 1:7; 1:8 input Serial-to-Parallel Converter.
- OSERDES: For high-speed interfaces, it supports 2:1; 4:1; 7:1; 8:1 output Parallel-to-Serial Converter.
- Built-in IO delay function, which can dynamically/statically adjust input/output delay.
- Built-in input FIFO, mainly used for clock domain conversion from external non-continuous DQS (for DDR memory interface) to internal continuous clock and compensating for the phase difference between the sampling clock and internal clock in some special Generic DDR applications.

1.3.5 Memory Controller System

PGL DDR Memory Controller System provides users with a complete DDR memory controller solution, with flexible configuration options.

PGL22G integrates HMEMC, and has the following functions:

- LPDDR, DDR2, DDR3 supported
- x8, x16 Memory Device supported
- Standard AXI4 bus protocol (does not support fixed burst type) supported
- Three AXI4 Host Ports in total, one 128-bit, two 64-bit
- AXI4 Read Reordering supported
- BANK Management supported
- Low Power Mode, Self-refresh, Power down, Deep Power Down supported

- Bypass DDRC and Bypass HMEMC supported
- DDR3 Write Leveling and DQS Gate Training supported
- DDR3 rate up to 800 Mbps

PGL12G, PGL25G, PGL50G, PGL50H, PGL100H can only use soft core to implement control of DDR memory, with the following functions:

- DDR3 supported
- x8, x16 Memory Device supported
- A maximum data width of 16 bits supported
- Trimmed AXI4 bus protocol supported
- One AXI4 128-bit Host Port
- Self-refresh, Power down supported
- Bypass DDRC supported
- DDR3 Write Leveling and DQS Gate Training supported
- DDR3 rate up to 800 Mbps

1.3.6 ADC

Each ADC has a resolution of 10 bits, a sampling rate of 1MSPS, and 12 channels, 10 of which are Analogue Inputs multiplexed with GPIO, and an additional 2 use dedicated analogue input pins. The scanning mode of the 12 channels is fully controlled by the FPGA with flexibility, and users can determine the number of channels that share the 1MSPS ADC sampling rate by User Logic.

The ADC provides monitoring functions for on-die voltage and temperature. It can detect VCC, VCCAUX, VDDM (internal LDO output voltage); see Table 6-1 for detailed characteristics parameters.

1.3.7 Clock Resources

Logos Family products are divided into different numbers of regions, offering extensive on-die clock resources, including PLL and three types of clock networks: global clock, regional clock, and I/O clock. Among them, the I/O clock has the characteristics of high frequency, small clock skew, and short delay time. See Table 1-3 for details on clock resources.

Table 1-3 Clock Resources of Logos Family Products

Features	**PGL12G**	**PGL22G**	**PGL25G**	**PGL50H** **PGL50G**	**PGL100H**
Number of Regions	4	6	4	6	10
Number of Global Clocks	20	20	20	30	30
Number of Global Clocks Supported by Each Region	16	12	16	16	16
Number of Regional Clocks Supported by Each Region	4	4	4	4	4
Number of IO BANKs	4	6	4	4	6
Number of IO Clocks Supported by Each IO BANK	2	2	4	BANK0/2: 4 BANK1/3: 6	BANK0/2: 4 BANK1/3: 10
Total Number of IO Clocks	8	12	16	20	28
Number of PLLs	4	6	4	5	8

Logos FPGAs embed multiple PLLs, each with up to 5 clock outputs, supporting frequency synthesis, phase adjustment, dynamic configuration, clock source synchronization, zero delay buffering, and more. Additionally, PLLs support Power Down, allowing users to turn off the PLL to reduce power consumption when it is not in use.

To increase clock performance, Logos FPGA also offers special IO related to CLK, including four types: clock input pins, PLL reference clock input pins, PLL feedback input clock pins, and PLL clock output pins. Compared with general IO, using these clock input/output pins can avoid interference from standard routing resources, thus achieving better clock performance. When not used as clock inputs/outputs, these clock pins can be used as general IOs. For detailed information on clock usage, please refer to the "Logos Family FPGAs Clock Resources (Clock) User Guide".

1.3.8 Configuration

Configuration is the process of programming the FPGA. Logos FPGA uses SRAM cells to store configuration data, which must be reconfigured after every power up; the configuration data can be actively obtained by the chip from external flash or downloaded into the chip via an external processor or controller.

Logos FPGA supports multiple configuration modes, including JTAG mode, Master SPI mode, Slave SPI mode, Slave Parallel mode, Slave Serial mode, and Master BPI mode. The supported configuration modes for each device are shown in Table 1-4.

Table 1-4 Configure Mode

Mode	Data Bit width	PGL12G		PGL22G		PGL22GS	PGL25G	PGL50H PGL50G	PGL 100H
		LPG144	FBG 256	FBG256	MBG324	LPG176	FBG256 MBG324 FBG484	FBG484 MBG484 MBG324	FBG900
JTAG	1	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
Master SPI	1	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
	2	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
	4	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
	8	Supported	Supported	Supported	Supported	Supported	Not supported	Not supported	Not supported
Slave SPI	1	Supported	Supported	Supported	Supported	Not supported	Not supported	Not supported	Not supported
Slave Parallel	8	Supported	Supported	Supported	Supported	Not supported	Supported	Supported	Supported
	16	Supported	Supported	Supported	Supported	Not supported	Supported	Supported	Supported
	32	Supported	Supported	Not supported	Supported	Not supported	Not supported	Not supported	Not supported
Slave Serial	1	Supported	Supported	Supported	Supported	Not supported	Supported	Supported	Supported
Master BPI	8 (Asynchronous)	Not supported	Not supported	Not supported	Supported	Not supported	Not supported	Not supported	Supported
	16 (Asynchronous)	Not supported	Not supported	Not supported	Supported	Not supported	Not supported	Not supported	Supported
	16 (Synchronous)	Not supported	Not supported	Not supported	Supported	Not supported	Not supported	Not supported	Not supported

The configuration-related functions of Logos FPGA are as follows:

- Supports configuration data stream compression, effectively reducing the size of the bit stream, saving memory space and programming time
- Supports SEU 1-bit error correction and 2-bit error detection through the internal parallel interface
- Watchdog timeout detection function supported
- Supports configuration bit stream version fallback function in Master BPI/Master SPI modes

To protect user designs, Logos FPGA also provides the UID function. Each FPGA device has a unique identification number that is uniquely determined at the factory. Users can read the identification number via the UID interface and JTAG interface, and incorporate the results into the programming data stream after processing with their own unique encryption algorithm. Every time the data stream is reloaded, the FPGA enters user mode, where the user logic will first read the UID and process it with a unique encryption algorithm to compare with the results in the previous programming data stream; if there is a discrepancy, the FPGA will not function properly.

1.3.9 HSST

PGL50H and PGL100H have built-in high-speed serial interface modules with line rates up to 6.375Gbps, known as HSST. In addition to the PMA, HSST also integrates a rich set of PCS

functions, which can be flexibly applied to various serial protocol standards. Internally, each HSST supports 1 to 4 full-duplex transmit and receive LANEs. The key features of HSST include:

- Supported line rates are shown in Table 7-4
- Flexible reference clock selection
- Programmable output swing and de-emphasis
- Adaptive equalizer at receiver side
- The data channels support 8bit only, 10bit only, 8b10b 8bit, 16bit only, 20bit only, 8b10b 16bit, 32bit only, 40bit only, 8b10b 32bit, 64b66b/64b67b 16bit, and 64b66b/64b67b 32bit modes
- The PCS is flexibly configurable and supports protocols such as PCI Express GEN1, PCI Express GEN2, XAUI, Gigabit Ethernet, CPRI, SRIO, etc.
- Flexible byte alignment function
- RxClock Slip function is supported to ensure a fixed receive delay
- Protocol standard 8b10b encoding/decoding supported
- Protocol standard 64b66b/64b67b data adaptation function supported
- Flexible CTC scheme
- x2 and x4 channel bonding supported
- HSST configuration supports dynamic modification
- Near-end loopback and far-end loopback
- Built-in PRBS Function

1.3.10 Logos Family FPGAs Reference Materials

Section 1.3 provides a brief description of the various Logos FPGA modules, as well as the clock and configuration system. For detailed information on the respective modules, please refer to the user guide documents related to Logos FPGA, as shown in Table 1-5 below.

Table 1-5 Logos Family FPGAs User Guide Documents

Document Number	Document Name	Content of the Document
UG020001	Logos Family FPGAs Configurable Logic Module (CLM) User Guide	Functional description of Logos Family FPGAs Configurable Logic Module
UG020002	Logos Family FPGAs Dedicated RAM Module (DRM) User Guide	Functional description of Logos Family FPGAs Dedicated RAM Module
UG020003	Logos Family FPGAs Arithmetic Processing Module (APM) User Guide	Functional description of Logos Family FPGAs Arithmetic Processing Module
UG020004	Logos Family FPGAs Clock Resources (Clock) User Guide	Logos Family FPGAs Clock Resources, including the function and usage of PLL
UG020005	Logos Family FPGAs Configuration User Guide	Description of the configuration interface, configuration modes, and configuration process in Logos Family FPGAs
UG020006	Logos Family FPGAs Input/Output Interface (IO)	Functional description of Logos Family FPGAs

Document Number	Document Name	Content of the Document
	User Guide	Input/Output Interface
UG020009	Logos Family FPGAs Analogue-to-Digital Converter (ADC) Module User Guide	Functional description of Logos Family FPGAs Analogue-to-Digital Converter
UG020011	Logos Family Products HMEMC Use Case User Guide	Description of the use cases for Logos Family FPGAs Memory Control System
UG020013	Logos Family FPGAs High-Speed Serial Transceiver (HSST) User Guide	Description of the applications for Logos Family FPGAs High-Speed Serial Transceiver

1.4 Logos Family FPGAs Ordering Information

Content and meaning of Logos Family FPGAs product model numbers are shown in Figure 1-1.

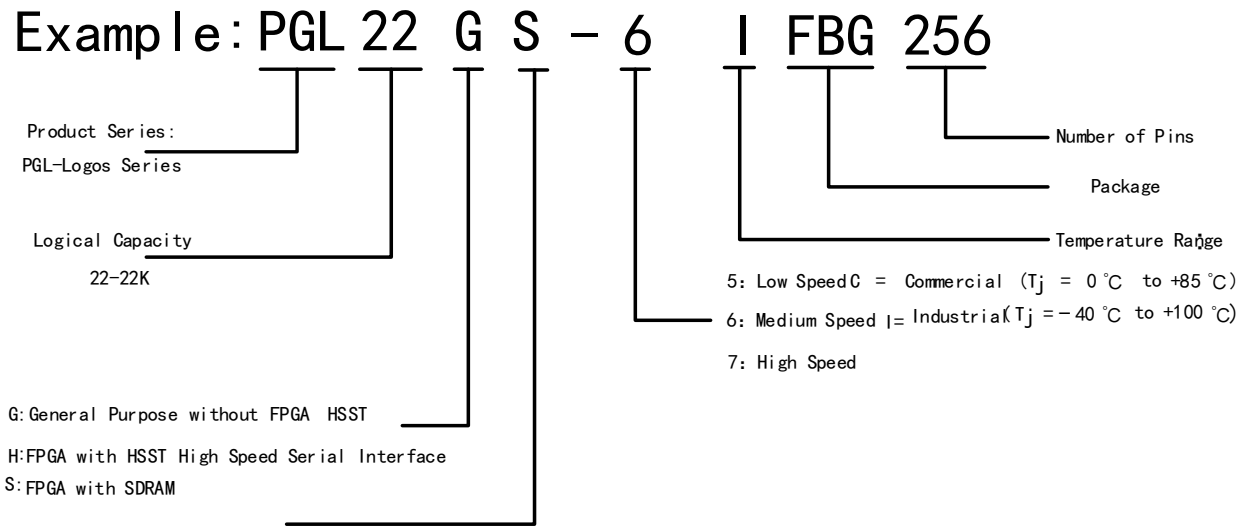

Figure 1-1 Content and Meaning of Logos Family FPGAs Product Model Numbers

Descriptions of the product quality grades are shown in Table 1-6.

Table 1-6 Descriptions of the Product Quality Grades

Product Family	Device	Speed Grade and Temperature Range	
		Commercial (C) 0 ℃ to 85 ℃	Industrial (I) -40 ℃ to 100 ℃
Logos	PGL12G	-6C	-6I
	PGL22G	-6C	-6I
	PGL25G	-5C	-5I
		-6C	-6I
	PGL50G	-6C	-6I
	PGL50H	-6C	-6I
	PGL100H	-6C	-6I

Chapter 2 Operating Conditions

2.1 Absolute Voltage Limits of the Device

Table 2-1 Absolute Maximum Voltage of the Device

Symbol	Description	Min.	Max.	Unit
VCC	Core Power Supply Voltage	-0.16	1.32	V
VCCAUX	Auxiliary Power Voltage (for powering IOB, LDO, etc.)	-0.16	3.63	V
VCCAUX_A	Auxiliary Power Voltage (for powering ADC, POR, Bandgap, etc.)	-0.16	3.63	V
VCCIO	BANK IO Power Supply Voltage	-0.16	3.63	V
VCCEFUSE	Efuse Programming Voltage	-0.16	3.63	V
VCCIOCFG	BANKCFG Power Supply Voltage	-0.16	3.63	V
VI	IO DC Input Voltage	-0.16	3.63	V

Note: Exceeding the above voltage limits may cause permanent damage to the device. Operating within the voltage limits will not damage the device, but does not guarantee normal function at these limits. Long-term operation of the device at the voltage limits will drastically impact its reliability.

2.2 V_I AC Overshoot Limit Value

Table 2-2 IO Input AC Overshoot Voltage Limit Values

Input Pin	Overshoot Voltage	Specification	Temperature	Condition	Limit Value	Unit
I/O input voltage, with respect to ground	OVERSHOOT	Industrial	-40 ℃~100 ℃	100%UI	4.02	V
				55%UI	4.07	V
				30%UI	4.12	V
				17%UI	4.17	V
				9.5%UI	4.22	V
				5.5%UI	4.27	V
				3.1%UI	4.32	V
				1.7%UI	4.37	V
				1.0%UI	4.42	V
				0.5%UI	4.47	V
				0.3%UI	4.52	V
				0.2%UI	4.57	V
				0.1%UI	4.62	V
	UNDERSHOOT	Industrial	-40 ℃~100 ℃	100%UI	-0.16	V
				72%UI	-0.21	V
				55%UI	-0.26	V

Input Pin	Overshoot Voltage	Specification	Temperature	Condition	Limit Value	Unit
				40%UI	-0.31	V
				30%UI	-0.36	V
				22%UI	-0.41	V
				17%UI	-0.46	V
				12%UI	-0.51	V
				10%UI	-0.56	V
				8%UI	-0.61	V
				6%UI	-0.66	V
				4%UI	-0.71	V
				3%UI	-0.76	V

Note: UI width is less than 15μs.

2.3 Device Quiescent Current

Table 2-3 Quiescent Current

Symbol	Description	Device	Speed Grade		Unit
			-5	-6	
I_{vcc}	Core voltage quiescent current	PGL12G	--	13	mA
		PGL22G	--	19	mA
		PGL25G	28	28	mA
		PGL50G	--	45	mA
		PGL50H	--	48	mA
		PGL100H	--	92	mA
I_{vccio}	BANK voltage quiescent current	PGL12G	--	3	mA
		PGL22G	--	3	mA
		PGL25G	3	3	mA
		PGL50G	--	3	mA
		PGL50H	--	3	mA
		PGL100H	--	6	mA
I_{vccaux_a}	Auxiliary voltage VCCAUX_A quiescent current	PGL12G	--	2	mA
		PGL22G	--	2	mA
I_{vccaux}	Auxiliary voltage VCCAUX (3.3V) quiescent current	PGL12G	--	11	mA
		PGL22G	--	32	mA
		PGL25G	9	9	mA
		PGL50G	--	8	mA
		PGL50H	--	8	mA
		PGL100H	--	9	mA
$I_{VCCA\_PLL\_0}$	HSST PLL0 single quad analogue power supply	PGL50H	--	0.9	mA

Symbol	Description	Device	Speed Grade		Unit
			-5	-6	
	quiescent current	PGL100H	--	0.9	mA
$I_{VCCA\_PLL\_1}$	HSST PLL1 single quad analogue power supply quiescent current	PGL50H	--	0.9	mA
		PGL100H	--	0.9	mA
I_{VCCA_LANE}	HSST single quad analogue power supply quiescent current	PGL50H	--	6.11	mA
		PGL100H	--	6.11	mA

Note:

1. The above quiescent current values are measured at standard pressure, Tj=25℃. For Tj=100℃, the PPP and PPC analysis tools can be used for evaluation.
2. The above data is measured with a blank device, no output current load, no internal pull-up resistors, and all I/Os in a tri-state.

2.4 Recommended Operating Conditions for the Device

Table 2-4 Recommended Operating Conditions for PGL12G, PGL22G

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Core Power Supply Voltage	1.045	1.1	1.155	V
VCCAUX	Auxiliary Power Voltage (for powering IOB, LDO, etc.)	3.135	3.3	3.465	V
VCCAUX_A	Auxiliary Power Voltage (for powering ADC, POR, Bandgap, etc.)	3.135	3.3	3.465	V
VCCIO	BANK IO Power Supply Voltage	1.14	--	3.465	V
VCCEFUSE	Efuse Programming Voltage	3.135	3.3	3.465	V
VCCIOCFG	BANKCFG Power Supply Voltage	1.425	--	3.465	V
T_J (Commercial)	Commercial chip junction temperature	0	--	85	℃
T_J (Industrial)	Industrial chip junction temperature	-40	--	100	℃

Note: Recommended operating voltage is within ±5% of the typical operating voltage.

Table 2-5 Recommended Operating Conditions for PGL25G

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Core Power Supply Voltage	1.14	1.2	1.26	V
VCCAUX	Auxiliary power supply voltage, including BANK configuration voltage, Efuse programming voltage, etc.	3.135	3.3	3.465	V
VCCIO	BANK IO Power Supply Voltage	1.14	--	3.465	V
T_J (Commercial)	Commercial chip junction temperature	0	--	85	℃
T_J (Industrial)	Industrial chip junction temperature	-40	--	100	℃

Note: Recommended operating voltage is within ±5% of the typical operating voltage.

Table 2-6 Recommended Operating Conditions for PGL50G, PGL50H, and PGL100H

Symbol	Description		Min.	Typ.	Max.	Unit
VCC	Core Power Supply Voltage		1.14	1.2	1.26	V
VCCAUX	Auxiliary power supply voltage, including BANK configuration voltage, etc.	VCCAUX=3.3V	3.135	3.3	3.465	V
		VCCAUX=2.5V	2.375	2.5	2.625	V
VCCIO	BANK IO Power Supply Voltage		1.14	--	3.465	V
VCCEFUSE	Efuse Programming Voltage		3.135	3.3	3.465	V
T_J (Commercial)	Commercial chip junction temperature		0	--	85	℃
T_J (Industrial)	Industrial chip junction temperature		-40	--	100	℃

Note: Recommended operating voltage is within ±5% of the typical operating voltage.

2.5 DC Characteristics of the Device Under Recommended Operating Conditions

Table 2-7 DC Characteristics of the Device under Recommended Operating Conditions

Identification	Min.	Typ.	Max.	Description
I_{PU}	80uA	--	200uA	PAD pull-up current (V_{IN}=0; V_{CCIO}=3.3V)
	40uA	--	120uA	PAD pull-up current (V_{IN}=0; V_{CCIO}=2.5V)
	60uA	--	190uA	PAD pull-up current (V_{IN}=0; V_{CCIO}=1.8V)
	60uA	--	190uA	PAD pull-up current (V_{IN}=0; V_{CCIO}=1.5V)
	30uA	--	120uA	PAD pull-up current (V_{IN}=0; V_{CCIO}=1.2V)
I_{PD}	30uA	--	225uA	PAD pull-down current (V_{IN}=3.3V)
	30uA	--	220uA	PAD pull-down current (V_{IN}=2.5V)
	30uA	--	240uA	PAD pull-down current (V_{IN}=1.8V)
	30uA	--	240uA	PAD pull-down current (V_{IN}=1.5V)
	30uA	--	260uA	PAD pull-down current (V_{IN}=1.2V)

2.6 Power-up/Power-down Sequences

1. Recommended power-up sequence to ensure I/Os are tri-stated during power-up: VCC, VCCA_LANE, VCCA_PLL0, VCCA_PLL1 >VCCAUX, VCCAUX_A, VCCIOCFG, VCCEFUSE > VCCIO;
2. The recommended power-down sequence is the reverse of the Power-up sequence;
3. Recommended power-up timing is shown in Figure 2-1;
4. Recommended Power-down timing is shown in Figure 2-2;
5. When the amplitude of VCCIO voltage is same as VCCAUX, VCCAUX_A, VCCIOCFG, VCCEFUSE, they can share the same power supply.

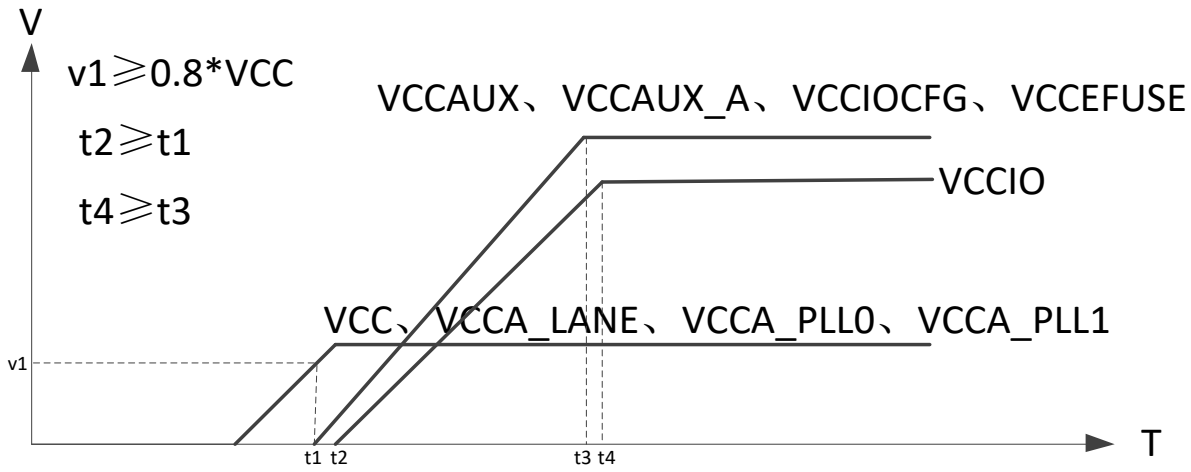

Figure 2-1 Recommended Power-up Timing

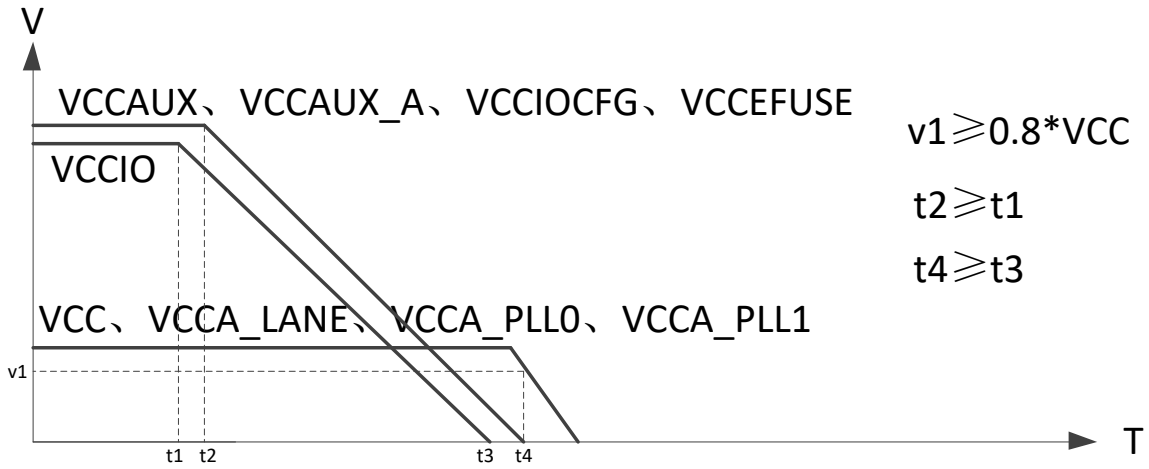

Figure 2-2 Recommended Power-down Timing

6. Power Supply Ramp Rate

Table 2-8 Power Supply Ramp Rate

Identification	Description	Min.	Max.	Unit
$T_{VCC\ RAMP}$	VCC Power Supply Ramp Rate	0.006	6	V/ms
$T_{VCCAUX\ RAMP}$	VCCAUX=3.3V Power Supply Ramp Rate	0.0165	6.6	V/ms
	VCCAUX=2.5V Power Supply Ramp Rate	0.0125	5	V/ms
$T_{VCCIO\ RAMP}$	VCCIO Power Supply Ramp Rate	0.0165	6.6	V/ms
$T_{VCCEFUSE\ RAMP}$	VCCEFUSE Power Supply Ramp Rate	0.0165	6.6	V/ms
$T_{VCCA\_LANE\ RAMP}$	VCCA LANE Power Supply Ramp Rate	0.024	2.4	V/ms
$T_{VCCA\_PLL\_0\ RAMP}$	VCCA PLL0 Power Supply Ramp Rate	0.024	2.4	V/ms
$T_{VCCA\_PLL\_1\ RAMP}$	VCCA PLL1 Power Supply Ramp Rate	0.024	2.4	V/ms

Note: The power supply ramp rate must be monotonic.

For PGL12G, PGL22G, PGL22GS, if the recommended power-up sequence is not followed, and there is a discrepancy between VCCAUX and VCCIO voltages, then during the power-up process, all available IO pins cannot remain in high-impedance state.

For PGL25G, PGL50G, PGL50H, PGL100H, if the recommended power-up sequence is not followed, and there is a discrepancy between VCCAUX and VCCIO voltages, then during the power-up process, the IO pins of BANK0 and BANK2 cannot remain in high-impedance state.

If EFuse is configured, the VCCEFUSE voltage must follow the recommended power-up and power-down sequences, otherwise it may lead to misconfiguration of EFuse. For specific EFuse applications please refer to the EFuse section in "UG02005 Logos Family FPGAs Configuration User Guide".

2.7 Hot Plug

2.7.1 Hot Plug Specification

Table 2-9 Hot Plug Leakage Current Specifications

Symbol	Parameter Description	Max.
I_{DK} (DC)[1]	DC Current, per I/O	1mA
I_{DK} (AC)[2]	AC Current, per I/O	6mA

Note:

1. When the chip is not powered-up, apply voltage to the hot pluggable I/O and test the maximum current flowing into the chip from the I/O.
2. Apply voltage to the hot-pluggable I/O and then test the maximum current flowing into the chip from the I/O during the power-up/down process following the recommended sequence.

2.7.2 Hot Plug Application Restrictions

To fulfill hot plug requirement, the following conditions must be met:

1. Power-up/Power-down must be performed according to the chip's recommended sequence.
2. To ensure application requirements are met, the user must choose appropriate external circuitry (such as pull-up/pull-down resistors and series resistors) etc.

2.8 ESD (HBM, CDM), Latch-Up Specifications

Table 2-10 ESD, Latch-Up Specifications

Human Body Model (HBM)	Charge Device Model (CDM)	Latch-up
±2000V	±500V	±100mA

Chapter 3 DC Characteristics

3.1 Input/Output Pin DC Characteristics

The input and output voltage range of each single-ended IO level standard is shown in Table 3-1 below.

Table 3-1 Input and Output Voltage Range of Single-Ended IO Level Standard

Single-Ended IO	VIL(V)		VIH(V)		VOL (V)	VOH(V)
	Min.	Max.	Min.	Max.	Max.	Min.
LVTLL33 LVCMOS33	-0.16	0.8	2	3.465	0.4	VCCIO-0.4
LVCMOS25	-0.16	0.7	1.7	3.465	0.4	VCCIO-0.4
LVCMOS18	-0.16	0.35VCCIO	0.65VCCIO	3.465	0.4	VCCIO-0.4
LVCMOS15	-0.16	0.35VCCIO	0.65VCCIO	3.465	0.4	VCCIO_0.4
LVCMOS12	-0.16	0.35VCCIO	0.65VCCIO	3.465	0.4	VCCIO-0.4
SSTL25_I	-0.16	VREF -0.18	VREF +0.18	3.465	0.54	VCCIO-0.62
SSTL25_II	-0.16	VREF -0.18	VREF +0.18	3.465	0.35	VCCIO-0.43
SSTL18_I	-0.16	VREF -0.125	VREF +0.125	3.465	0. 4	VCCIO-0.4
SSTL18_II	-0.16	VREF -0.125	VREF +0.125	3.465	0.28	VCCIO-0.28
SSTL15_I SSTL15_I _CAL	-0.16	VREF-0.1	VREF+0.1	3.465	0.31	VCCIO-0.31
SSTL15_II SSTL15_II_CAL	-0.16	VREF-0.1	VREF+0.1	3.465	0.31	VCCIO-0.31
HSTL18_I	-0.16	VREF-0.1	VREF+0.1	3.465	0. 4	VCCIO-0.4
HSTL18_II	-0.16	VREF-0.1	VREF+0.1	3.465	0. 4	VCCIO-0.4
HSTL15_I HSTL15_I_CAL	-0.16	VREF-0.1	VREF+0.1	3.465	0. 4	VCCIO-0.4

Note: Only PGL22G supports CAL.

For the output current of each single-ended IO level standard, see the table below.

Table 3-2 Output Current of Single-Ended IO Level Standard

Single-Ended IO	IOL(mA)	IOH(mA)	VREF(V)	VTT(V)
LVTTL33 LVCMOS33	4	-4	-	-
	8	-8	-	-
	12	-12	-	-
	16	-16	-	-
	24	-24	-	-
LVCMOS25	4	-4	-	-
	8	-8	-	-
	12	-12	-	-

Single-Ended IO	IOL(mA)	IOH(mA)	VREF(V)	VTT(V)
	16	-16	-	-
LVCMOS18	4	-4	-	-
	8	-8	-	-
	12	-12	-	-
LVCMOS15	4	-4	-	-
	8	-8	-	-
LVCMOS12	2	-2	-	-
	6	-6	-	-
SSTL25_I	8.1	-8.1	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
SSTL25_II	16.2	-16.2	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
SSTL18_I	6.7	-6.7	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
SSTL18_II	13.4	-13.4	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
SSTL15_I SSTL15_I_CAL	7.5	-7.5	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
SSTL15_II SSTL15_II_CAL	8.8	-8.8	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
HSTL18_I	8	-8	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
HSTL18_II	16	-16	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
HSTL15_I HSTL15_I_CAL	8	-8	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO

Note: Only PGL22G supports CAL, PGL22GS_LPG176 L0 BANK does not support all level standards that use VREF.

Table 3-3 Bank Support Description for Input IO Level Standard

	Mode	IO Standard	Device							
			PGL22G		PGL12G		PGL25G/PGL50G /PGL50H		PGL100H	
			BANK L0 BANK L1 BANK L2	BANKR0 BANKR1 BANKR2	BANKL0 BANKL1	BANKR0 BANKR1	BANK0 BANK2	BANK1 BANK3	BANK0 BANK2	BANK1 BANK3 BANK4 BANK5
Input	Single-Ended	LVCMOS12 LVCMOS15 LVCMOS18 LVCMOS25 LVCMOS33 LVTTL33 SSTL15_I SSTL15_II SSLT18_I SSTL18_II HSLT18_I HSTL18_II SSTL25_I SSTL25_II	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
		SSTL15_I_CAL SSTL15_II_CAL HSTL15_I_CAL	Supported	Supported	Not supported	Not supported	Not supported	Not supported	Not supported	Not supported
	Differential	LVPECL LVDS25 LVDS33 SLVS MINI-LVDS SUB-LVDS TMDS	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
		RSDS PPDS SSTL15D_I SSTL15D_II SSTL18D_I SSTL18D_II SSTL25D_I SSTL25D_II HSTL15D_I HSTL18D_I HSTL18D_II	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
		SSTL15D_I_CAL SSTL15D_II_CAL HSTL15D_I_CAL	Supported	Supported	Not supported	Not supported	Not supported	Not supported	Not supported	Not supported

Table 3-4 Bank Support Description for Output IO Level Standard

	Mode	IO Standard	Device							
			PGL22G		PGL12G		PGL25G/PGL50G/ PGL50H		PGL100H	
			BANKL0 BANKL1 BANKL2	BANKR0 BANKR1 BANKR2	BANKL0 BANKL1	BANKR0 BANKR1	BANK0 BANK2	BANK1 BANK3	BANK0 BANK2	BANK1 BANK3 BANK4 BANK5
Output	Single-Ended	LVCMOS12 LVCMOS15 LVCMOS18 LVCMOS25 LVCMOS3 LVTTL33 SSTL15_I SSTL15_II SSLT18_I SSTL18_II HSLT18_I HSTL18_II SSTL25_I SSTL25_II	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
		SSTL15_I_CAL SSTL15_II_CAL HSTL15_I_CAL	Supported	Supported	Not supported	Not supported	Not supported	Not supported	Not supported	Not supported
	Differential	LVDS25 LVDS33 SLVS MINI-LVDS SUB-LVDS TMDS	Supported	Supported	Not supported	Supported	Supported	Not supported	Supported	Not supported
		PPDS RSDS LVPECL SSTL15D_I SSTL15D_II SSTL18D_I SSTL18D_II SSTL25D_I SSTL25D_II HSTL15D_I HSTL18D_I HSTL18D_II	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported

Table 3-5 Bank Support Description for Bidirectional IO Level Standard

	Mode	IO Standard	Device							
			PGL22G		PGL12G		PGL25G/PGL50G/ PGL50H		PGL100H	
			BANK L0 BANK L1 BANK L2	BANKR0 BANKR1 BANKR2	BANKL0 BANKL1	BANKR0 BANKR1	BANK0 BANK2	BANK1 BANK3	BANK0 BANK2	BANK1 BANK3 BANK4 BANK5
Bi-Directional	Single-Ended	LVCMOS12 LVCMOS15 LVCMOS18 LVCMOS25 LVCMOS33 LVTTL33 SSTL15_I SSTL15_II SSLT18_I SSTL18_II HSLT18_I HSTL18_II SSTL25_I SSTL25_II	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
		SSTL15_I_CAL SSTL15_II_CAL HSTL15_I_CAL	Supported	Supported	Not supported	Not supported	Not supported	Not supported	Not supported	Not supported
	Differential	LVDS25 LVDS33 MINI-LVDS SUB-LVDS SLVS TMDS	Not supported	Not supported	Not supported	Not supported	Not supported	Not supported	Not supported	Not supported
		PPDS RSDS SSTL15D_I SSTL15D_II SSTL18D_I SSTL18D_II SSTL25D_I SSTL25D_II HSTL15D_I HSTL18D_I HSTL18D_II LVPECL	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
		SSTL15D_I_CAL SSTL15D_II_CAL HSTL15D_I_CAL	Supported	Supported	Not supported	Not supported	Not supported	Not supported	Not supported	Not supported

The main electrical characteristics of the differential IO level standards are defined in the following figure, with the input and output voltage ranges as shown in Table 3-6 and Table 3-7.

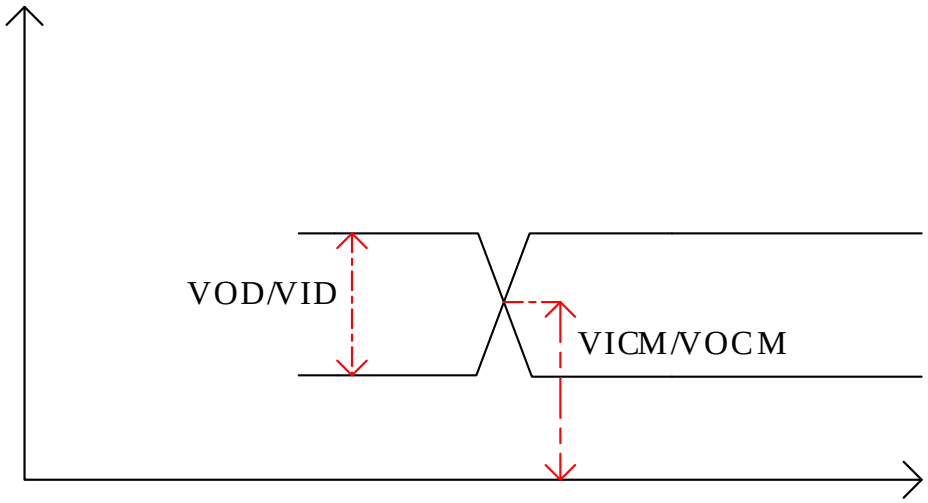

Figure 3-1 Differential Electrical Characteristics Parameters

Table 3-6 Parameter Requirements for Differential Input Standard

Standard	**VICM**			**VID**		
	Input Common Mode Voltage (V)			**Input Differential Mode Voltage (V)**		
	min	**typ**	**max**	**min**	**typ**	**max**
LVDS25	0.5	1.2	1.9	0.1	0.35	0.5
LVDS33	0.5	1.2	1.9	0.1	0.35	0.5
MINI-LVDS	0.4	--	1.9	0.2	0.4	0.6
SUB-LVDS	0.6	0.9	1.2	0.08	0.1	0.2
SLVS	0.07	--	0.3	0.08	--	0.46
LVPECL	0.5	--	1.9	0.3	--	1.1

Table 3-7 Parameter Requirements for Differential Output Standard

Standard	**VOCM**			**VOD**		
	Output Common-Mode Voltage (V)			**Output Differential Mode Voltage (V)**		
	min	**typ**	**max**	**min**	**typ**	**max**
LVDS25	1	1.25	1.4	0.25	0.35	0.45
LVDS33	1	1.25	1.4	0.25	0.35	0.45
MINI-LVDS	1	1.2	1.4	0.3	--	0.6
SUB-LVDS	0.8	0.9	1	0.1	0.15	0.2
SLVS	0.15	0.2	0.25	0.14	0.2	0.27

Chapter 4 AC Characteristics

This chapter primarily lists the AC characteristics of each logic unit of the Logos Family FPGAs under recommended operating conditions.

4.1 IO AC Characteristics Parameters

The switching characteristics of the IOB are as shown in Table 4-1.

Table 4-1 IOB Input and Output Delays

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Unit
	-5	-6	-5	-6	-5	-6	
LVTTL33,4mA,Slow	1.725	1.50	3.289	2.86	3.289	2.86	ns
LVTTL33,8mA,Slow	1.725	1.50	3.174	2.76	3.174	2.76	ns
LVTTL33,12mA,Slow	1.725	1.50	3.059	2.66	3.059	2.66	ns
LVTTL33,16mA,Slow	1.725	1.50	2.944	2.56	2.944	2.56	ns
LVTTL33,24mA,Slow	1.725	1.50	2.829	2.46	2.829	2.46	ns
LVTTL33,4mA,Fast	1.725	1.50	3.22	2.80	3.22	2.80	ns
LVTTL33,8mA,Fast	1.725	1.50	3.105	2.70	3.105	2.70	ns
LVTTL33,12mA,Fast	1.725	1.50	2.99	2.60	2.99	2.60	ns
LVTTL33,16mA,Fast	1.725	1.50	2.875	2.50	2.875	2.50	ns
LVTTL33,24mA,Fast	1.725	1.50	2.76	2.40	2.76	2.40	ns
LVCMOS33,4mA,Slow	1.725	1.50	3.289	2.86	3.289	2.86	ns
LVCMOS33,8mA,Slow	1.725	1.50	3.174	2.76	3.174	2.76	ns
LVCMOS33,12mA,Slow	1.725	1.50	3.059	2.66	3.059	2.66	ns
LVCMOS33,16mA,Slow	1.725	1.50	2.944	2.56	2.944	2.56	ns
LVCMOS33,24mA,Slow	1.725	1.50	2.829	2.46	2.829	2.46	ns
LVCMOS33,4mA,Fast	1.725	1.50	3.22	2.80	3.22	2.80	ns
LVCMOS33,8mA,Fast	1.725	1.50	3.105	2.70	3.105	2.70	ns
LVCMOS33,12mA,Fast	1.725	1.50	2.99	2.60	2.99	2.60	ns
LVCMOS33,16mA,Fast	1.725	1.50	2.875	2.50	2.875	2.50	ns
LVCMOS33,24mA,Fast	1.725	1.50	2.76	2.40	2.76	2.40	ns
LVCMOS25,4mA,Slow	2.07	1.80	3.404	2.96	3.404	2.96	ns
LVCMOS25,8mA,Slow	2.07	1.80	3.289	2.86	3.289	2.86	ns
LVCMOS25,12mA,Slow	2.07	1.80	3.174	2.76	3.174	2.76	ns
LVCMOS25,16mA,Slow	2.07	1.80	3.059	2.66	3.059	2.66	ns
LVCMOS25,4mA,Fast	2.07	1.80	3.335	2.90	3.335	2.90	ns
LVCMOS25,8mA,Fast	2.07	1.80	3.22	2.80	3.22	2.80	ns
LVCMOS25,12mA,Fast	2.07	1.80	3.105	2.70	3.105	2.70	ns

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Unit
	-5	-6	-5	-6	-5	-6	
LVCMOS25,16mA,Fast	2.07	1.80	2.99	2.60	2.99	2.60	ns
LVCMOS18,4mA,Slow	3.335	2.90	3.749	3.26	3.749	3.26	ns
LVCMOS18,8mA,Slow	3.335	2.90	3.519	3.06	3.519	3.06	ns
LVCMOS18,12mA,Slow	3.335	2.90	3.289	2.86	3.289	2.86	ns
LVCMOS18,4mA,Fast	3.335	2.90	3.68	3.20	3.68	3.20	ns
LVCMOS18,8mA,Fast	3.335	2.90	3.45	3.00	3.45	3.00	ns
LVCMOS18,12mA,Fast	3.335	2.90	3.22	2.80	3.22	2.80	ns
LVCMOS15,4mA,Slow	4.14	3.60	3.864	3.36	3.864	3.36	ns
LVCMOS15,8mA,Slow	4.14	3.60	3.634	3.16	3.634	3.16	ns
LVCMOS15,4mA,Fast	4.14	3.60	3.795	3.30	3.795	3.30	ns
LVCMOS15,8mA,Fast	4.14	3.60	3.565	3.10	3.565	3.10	ns
LVCMOS12,2mA,Slow	7.36	6.40	5.129	4.46	5.129	4.46	ns
LVCMOS12,6mA,Slow	7.36	6.40	4.209	3.66	4.209	3.66	ns
LVCMOS12,2mA,Fast	7.36	6.40	5.06	4.40	5.06	4.40	ns
LVCMOS12,6mA,Fast	7.36	6.40	4.14	3.60	4.14	3.60	ns
SSTL25_I	1.38	1.20	3.22	2.80	3.22	2.80	ns
SSTL25_II	1.38	1.20	3.22	2.80	3.22	2.80	ns
SSTL18_I	1.495	1.30	3.45	3.00	3.45	3.00	ns
SSTL18_II	1.495	1.30	3.45	3.00	3.45	3.00	ns
SSTL15_I	1.84	1.60	3.45	3.00	3.45	3.00	ns
SSTL15_II	1.84	1.60	3.45	3.00	3.45	3.00	ns
SSTL135	2.07	1.80	3.795	3.30	3.795	3.30	ns
HSTL18_I	1.495	1.30	3.45	3.00	3.45	3.00	ns
HSTL18_II	1.495	1.30	3.45	3.00	3.45	3.00	ns
HSTL15_I	1.84	1.60	3.45	3.00	3.45	3.00	ns
LVDS25	1.38	1.20	2.76	2.40	2.76	2.40	ns
LVDS33	1.38	1.20	2.76	2.40	2.76	2.40	ns
MINI_LVDS	1.38	1.20	2.76	2.40	2.76	2.40	ns
SUB_LVDS	1.38	1.20	2.76	2.40	2.76	2.40	ns
SLVS	1.38	1.20	2.76	2.40	2.76	2.40	ns
TMDS	1.38	1.20	2.76	2.40	2.76	2.40	ns
PPDS	1.38	1.20	2.76	2.40	2.76	2.40	ns
LVPECL	1.38	1.20	2.76	2.40	2.76	2.40	ns
RSDS	1.38	1.20	2.76	2.40	2.76	2.40	ns
BLVDS	1.38	1.20	2.76	2.40	2.76	2.40	ns
SSTL25D_I	1.38	1.20	3.22	2.80	3.22	2.80	ns
SSTL25D_II	1.38	1.20	3.22	2.80	3.22	2.80	ns
SSTL18D_I	1.495	1.30	3.45	3.00	3.45	3.00	ns

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Unit
	-5	-6	-5	-6	-5	-6	
SSTL18D_II	1.495	1.30	3.45	3.00	3.45	3.00	ns
SSTL15D_I	1.84	1.60	3.45	3.00	3.45	3.00	ns
SSTL15D_II	1.84	1.60	3.45	3.00	3.45	3.00	ns
SSTL135D	2.3	2.00	3.795	3.30	3.795	3.30	ns
HSTL18D_I	1.495	1.30	3.45	3.00	3.45	3.00	ns
HSTL18D_II	1.495	1.30	3.45	3.00	3.45	3.00	ns
HSTL15D_I	1.84	1.60	3.45	3.00	3.45	3.00	ns

Note: The parameters in the table are only applicable to PGL22G, PGL25G; for parameters of other devices in the Logos Family, please refer to the PDS timing report.

T_{IOPI}: Delay from the IOB Pad through IBUF to the DIN of the IOBUFFER.

T_{IOOP}: Delay from the DO of the IOBUFFER through OBUF to the IOB Pad.

T_{IOTP}: Delay from the TO of the IOBUFFER through OBUF to the IOB Pad.

Table 4-2 Output Switching Characteristics when IOB tri-state is Enabled

Symbol	Characteristic Parameter Description	Speed Grade		Unit
		-5	-6	
T_{IOTPHZ}	T input to Pad high-impedance	3.105	2.7	ns

Note: The parameters in the table are only applicable to PGL22G, PGL25G; for parameters of other devices in the Logos Family, please refer to the PDS timing report. T_{IOTPHZ} parameter: Delay from the TO of the IOBUFFER through OBUF to the IOB Pad when tri-state is enabled.

The AC characteristics of the IOL are as shown in Table 4-3 to Table 4-5.

Table 4-3 IOL Register AC Parameters

Symbol	AC Characteristics Parameters Description		Value		Unit	Comment
			-5	-6		
IFF		Setup Time/Hold Time				
	CE -> CLK setup/hold	Rising Edge	0.151/-0.051	0.131/-0.044	ns	
		Falling Edge	0.074/-0.036	0.064/-0.031	ns	
	LRS -> CLK setup/hold	Rising Edge	0.319/-0.114	0.277/-0.099	ns	
		Falling Edge	0.251/-0.102	0.218/-0.089	ns	
	DIN -> CLK setup/hold	Rising Edge	0.061/-0.014	0.053/-0.012	ns	
		Falling Edge	-0.005/-0.003	-0.004/-0.003	ns	
		Combinatorial Logic Delay				
	DIN -> RX_DATA_DD	0 -> 1	0.173	0.150	ns	Bypass Mode
		1 -> 0	0.173	0.150	ns	
		Sequential Delays Timing Delay				

Symbol	AC Characteristics Parameters Description		Value		Unit	Comment
			-5	-6		
	DIN -> RX_DATA	0 -> 1	0.273	0.237	ns	Latch Mode
		1 -> 0	0.268	0.233	ns	
	CLK -> Q Output	0 -> 1	0.413	0.359	ns	
		1 -> 0	0.434	0.377	ns	
	LRS -> Q Output	0 -> 1	0.620	0.539	ns	
		1 -> 0	0.620	0.539	ns	
OFF/TSFF		Setup Time/Hold Time				
	TX_DATA -> CLK setup/hold	Rising Edge	0.164/-0.053	0.143/-0.046	ns	
		Falling Edge	0.085/-0.037	0.074/-0.032	ns	
	CE -> CLK setup/hold	Rising Edge	0.194/-0.067	0.169/-0.058	ns	
		Falling Edge	0.141/-0.060	0.123/-0.052	ns	
	TS_CTRL -> CLK setup/hold	Rising Edge	0.140/-0.067	0.122/-0.058	ns	
		Falling Edge	0.085/-0.061	0.074/-0.053	ns	
		Sequential Delays Timing Delay				
	TX_DATA -> DO	0 -> 1	0.416	0.362	ns	Latch Mode
		1 -> 0	0.424	0.369	ns	
	CLK -> OFF Q/TSFF Q	0 -> 1	0.415	0.361	ns	
		1 -> 0	0.426	0.370	ns	
	LRS -> OFF Q Output/TSFF Q Output	0 -> 1	0.641	0.557	ns	
		1 -> 0	0.641	0.557	ns	

Note: The parameters in the table are only applicable to PGL22G, PGL25G; for parameters of other devices in the Logos Family, please refer to the PDS timing report..

Table 4-4 Input Deserializer Switching Parameters

Symbol	Characteristic Parameter Description		Speed Grade		Unit
			-5	-6	
IDDR		Signal Setup Time/Hold Time			
	PADI -> RCLK	Rising Edge	-0.001/0.025	-0.001/0.022	ns
		Falling Edge	0.012/0.016	0.010/0.014	ns
		Sequential Delays Timing Delay			
	RCLK -> Q Side	Rising Edge	0.298	0.259	ns
		Falling Edge	0.302	0.263	ns
	Maximum Frequency of RCLK		266	266	MHz

Note: The parameters in the table are only applicable to PGL22G, PGL25G; for parameters of other devices in the Logos Family, please refer to the PDS timing report.

Table 4-5 Output Serializer Switching Parameters

Symbol	Characteristic Parameter Description			Speed Grade		Unit
				-5	-6	
ODDR		Signal Setup Time/Hold Time				
	D -> RCLK		Rising Edge	0.240/-0.109	0.209/-0.095	ns
			Falling Edge	0.208/-0.041	0.181/-0.036	ns
	T -> RCLK		Rising Edge	0.254/-0.112	0.221/-0.097	ns
			Falling Edge	0.210/-0.041	0.183/-0.036	ns
		Sequential Delays Timing Delay				
	RCLK -> PADO Side/PADT Side		Rising Edge	0.728	0.633	ns
			Falling Edge	0.784	0.682	ns
	Maximum Frequency of RCLK			266	266	MHz

Note: The parameters in the table are only applicable to PGL22G, PGL25G; for parameters of other devices in the Logos Family, please refer to the PDS timing report.

CLM AC Characteristics Parameters

Table 4-6 CLM Module AC Characteristics

NO.	Parameter Description	Value		Property	Unit
		-5	-6		
Logic Delay					
1	LUT5 input Ax/Bx/Cx/Dx to Y0/Y1/Y2/Y3 delay	0.590	0.513	Max.	ns
2	LUT5 input Ax/Bx/Cx/Dx and M0/M1 to Y6AB/Y6CD delay	0.449	0.39	Max.	ns
3	LUT5 input Ax/Bx/Cx/Dx and M0/M1/M2 to Y1 (LUT7) delay	0.621	0.54	Max.	ns
4	LUT5 input Ax/Bx/Cx/Dx and M0/M1/M2/M3 to Y3 (LUT8) delay	0.673	0.585	Max.	ns
5	LUT input Ax to cout delay	0.426	0.37	Max.	ns
6	LUT input Bx to cout delay	0.445	0.387	Max.	ns
7	LUT input Cx to cout delay	0.501	0.436	Max.	ns
8	LUT input Dx to cout delay	0.496	0.431	Max.	ns
9	CIN input to cout delay	0.231	0.201	Max.	ns
10	CIN input to Y0/Y1/Y2/Y3 delay	0.319	0.277	Max.	ns
Timing Parameter					
11	CLK input with respect to TCO of Q0/Q1/Q2/Q3	0.300	0.261	Max.	ns
12	CLK input with respect to TCO of Y0 (QP0)/Y2 (QP1)	0.374	0.325	Max.	ns
13	Ax/Bx/Cx/Dx with respect to DFF setup/hold	0.056/-0.030	0.049/-0.026	Min.	ns
14	M with respect to DFF setup/hold	0.029/-0.003	0.025/-0.003	Min.	ns

NO.	Parameter Description	Value		Property	Unit
15	CE with respect to DFF setup/hold	0.213/-0.186	0.185/-0.162	Min.	ns
16	RS with respect to DFF setup/hold	0.213/-0.186	0.185/-0.162	Min.	ns
17	CIN with respect to DFF setup/hold	0.030/-0.005	0.0263/-0.004	Min.	ns
18	SHIFTIN with respect to DFF setup/hold	0.213/-0.186	0.185/-0.162	Min.	ns
19	Minimum pulse width of RS	1.035	0.9	Min.	ns
Distributed RAM Timing Parameters					
20	CLK -> Y0/Y1/Y2/Y3 mem read delay	0.828	0.72	Max.	ns
21	CLK -> RS (as WE) timing check, setup/hold	0.213/-0.186	0.185/-0.162	Min.	ns
22	CLK -> M0/M1/M2/M3 address timing check, setup/hold	-0.239/0.267	-0.208/0.232	Min.	ns
23	CLK -> AD/BD/CD/DD data timing check, setup/hold	-0.239/0.267	-0.208/0.232	Min.	ns

Note: The parameters in the table are only applicable to PGL22G, PGL25G; for parameters of other devices in the Logos Family, please refer to the PDS timing report.

DRM AC Characteristics Parameters

Table 4-7 DRM Module AC Characteristics

Symbol	AC Characteristics Parameters Description	Value		Property	Unit
		-5	-6		
Tco_9k	CLKA/CLKB->QA/QB (Output register disabled, 9K mode)	2.682	2.351	Max.	ns
Tco_9k_reg	CLKA/CLKB->QA/QB (Output register enabled, 9K mode)	0.796	0.698	Max.	ns
Tco_18k	CLKA/CLKB->QA/QB (Output register disabled, 18K mode & FIFO mode)	2.682	2.351	Max.	ns
Tco_18k_reg	CLKA/CLKB->QA/QB (Output register enabled, 18K mode & FIFO mode)	0.796	0.698	Max.	ns
Tco_flag_full	CLKA->FULL(ALMOST_FULL) Flag	1.205	1.058	Max.	ns
Tco_flag_empty	CLKB->EMPTY(ALMOST_EMPTY) Flag	0.874	0.766	Max.	ns
Tsu_9k_ad/ Thd_9k_ad	Address Input Setup/Hold Time (9K mode)	-0.150/0.212	-0.130/0.184	Min.	ns
Tsu_9k_d/ Thd_9k_d	Data Input Setup/Hold Time (9K mode)	-0.110/0.171	-0.096/0.149	Min.	ns
Tsu_9k_ce/ Thd_9k_ce	CE Input Setup/Hold Time (9K mode)	0.081/-0.021	0.070/-0.018	Min.	ns
Tsu_9k_we/ Thd_9k_we	WE Input Setup/Hold Time (9K mode)	0.032/-0.030	0.028/-0.026	Min.	ns
Tsu_9k_be/ Thd_9k_be	BE Input Setup/Hold Time (9K mode)	-0.036/0.098	-0.031/0.085	Min.	ns
Tsu_9k_oe/ Thd_9k_oe	OCE Input Setup/Hold Time (9K mode)	-0.046/0.099	-0.040/0.086	Min.	ns
Tsu_9k_rst/ Thd_9k_rst	Synchronous Reset Input Setup/Hold Time (9K mode)	0.025/0.026	0.022/0.023	Min.	ns
Tsu_18k_ad/ Thd_18k_ad	Address Input Setup/Hold Time (18K mode)	-0.225/0.288	-0.196/0.250	Min.	ns

Symbol	AC Characteristics Parameters Description	Value		Property	Unit
		-5	-6		
Tsu_18k_d/ Thd_18k_d	Data Input Setup/Hold Time (18K mode)	-0.118/0.181	-0.103/0.157	Min.	ns
Tsu_18k_ce/ Thd_18k_ce	CE Input Setup/Hold Time (18K mode)	0.070/-0.012	0.061/-0.010	Min.	ns
Tsu_18k_we/ Thd_18k_we	WE Input Setup/Hold Time (18K mode)	0.046/0.015	0.040/0.013	Min.	ns
Tsu_18k_be/ Thd_18k_be	BE Input Setup/Hold Time (18K mode)	0.048/0.014	0.042/0.012	Min.	ns
Tsu_18k_oe/ Thd_18k_oe	OCE Input Setup/Hold Time (18K mode)	-0.064/0.106	-0.056/0.092	Min.	ns
Tsu_18k_rst/ Thd_18k_rst	Synchronous Reset Input Setup/Hold Time (18K mode)	0.044/0.009	0.038/0.008	Min.	ns
Tsu_fifo_wctl/ Thd_fifo_wctl	WREOP(WRERR) Input Setup/Hold Time	0.095/-0.043	0.083/-0.037	Min.	ns
Tsu_fifo_rctl/ Thd_fifo_rctl	RDNAK Input Setup/Hold Time	0.067/-0.015	0.058/-0.013	Min.	ns
Tmpw_norm	CLKA/CLKB MPW (NW/TW)	1.328	1.643	Min.	ns
Tmpw_rbw	CLKA/CLKB MPW (RBW)	1.772	2.350	Min.	ns
Tmpw_fifo	CLKA/CLKB MPW (FIFO)	2.018	1.766	Min.	ns

Note: The parameters in the table are only applicable to PGL22G, PGL25G; for parameters of other devices in the Logos Family, please refer to the PDS timing report.

4.2 APM AC Characteristics Parameters

Table 4-8 APM Module AC Characteristics

AC Characteristics Parameters Description	Pre-adder	Multiplier	Post-adder	Value		Unit
				-5	-6	
Data/Control Pin to Input Register CLK Setup and Hold Time						
Z -> preadd unit register CLK setup/hold	Yes	NA	NA	3.034/-0.819	2.638/-0.712	ns
X -> preadd unit register CLK setup/hold	Yes	NA	NA	2.995/-0.605	2.604/-0.526	ns
Z-> input unit register CLK setup/hold	NA	NA	NA	0.978/-0.101	0.850/-0.088	ns
X-> input unit register CLK setup/hold	NA	NA	NA	1.002/-1.139	0.871/-0.99	ns
Y-> input unit register CLK setup/hold	NA	NA	NA	1.007/-0.099	0.876/-0.086	ns
MODEX-> preadd unit register CLK setup/hold	Yes	NA	NA	1.635/-0.423	1.422/-0.368	ns
Data Pin to Pipeline Register CLK Setup and Hold Time						
Y-> Multiplier unit register CLK setup/hold	NA	Yes	No	2.198/-0.438	1.911/-0.381	ns
X-> Multiplier unit register CLK setup/hold	Yes	Yes	No	2.777/-0.682	2.415 / -0.593	ns
X-> Multiplier unit register CLK setup/hold	No	Yes	No	2.213/-0.509	1.924 / -0.443	ns
Z-> Multiplier unit register CLK setup/hold	Yes	Yes	No	2.819/-0.759	2.451/-0.660	ns
Data/Control Pin to Output Register CLK Setup and Hold Time						
Y-> postadd unit register CLK setup/hold	NA	Yes	Yes	2.997/-0.783	2.606/-0.681	ns

AC Characteristics Parameters Description	Pre-adder	Multiplier	Post-adder	Value		Unit
				-5	-6	
X-> postadd unit register CLK setup/hold	NO	Yes	Yes	3.039/-0.806	2.643/-0.701	ns
X-> postadd unit register CLK setup/hold	Yes	Yes	Yes	3.598/-0.966	3.129/-0.840	ns
Z-> postadd unit register CLK setup/hold	Yes	Yes	Yes	3.640/-1.071	3.165/-0.931	ns
Z-> postadd unit register CLK setup/hold	NA	NA	Yes	3.120/-0.477	2.713/-0.415	ns
CPI -> postadd unit register CLK setup/hold	NA	NA	Yes	2.530/-0.260	2.200/-0.226	ns
From Each Stage of Register CLK to APM Output Pin Time						
postadd unit register CLK ->P output	NA	NA	NA	1.114	0.884	ns
Multiplier unit register CLK -> Poutput	NA	NA	Yes	1.110	0.881	ns
pretadd unit register CLK -> DPO output	Yes	Yes	Yes	3.224	2.559	ns
Z input unit register CLK -> DPO output	No	No	Yes	2.177	1.728	ns
From Data/Control Pin to APM Output Pin Combinational Logic Delay						
Y-> Poutput	NA	Yes	NO	3.117	2.474	ns
Y->P output	NA	Yes	Yes	3.866	3.068	ns
X ->P output	No	Yes	No	2.638	2.094	ns
X ->P output	Yes	Yes	NO	3.117	2.474	ns
X -> Poutput	Yes	Yes	Yes	3.866	3.068	ns
Z -> P output	Yes	Yes	Yes	3.866	3.068	ns
CPI -> P output	NA	NA	Yes	2.655	2.107	ns

Note: The parameters in the table are only applicable to PGL22G, PGL25G; for parameters of other devices in the Logos Family, please refer to the PDS timing report.

4.3 PLL AC Characteristics Parameters

Table 4-9 PLL AC Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Fin	PLL Input Reference Frequency	5		625	MHz
t_{RST_PLL}	PLL Initialization High-Level Reset Signal Width	0.3			MS
F_{pfd}	PFD Input Frequency	5		320	MHz
F_{sw}	Frequencies supported by PLL input reference clock when the auto-switching function of the input clock is supported			320	MHz
F_{out}	PLL Output Clock Frequency	1.172		625	MHz
F_{vco}	VCO Operating Range	600		1250	MHz
t_{fpa}	Fine Adjustment Phase Error (All Settings for CLKOUT1)	-50	0	50	ps
t_{OPW}	Output Clock Width (High or Low)	0.8			ns
t_{OPJIT}	Output Clock Period Jitter (fOUT >= 100MHz)			300	ps p-p
	Output Clock Period Jitter (fOUT < 100MHz)			0.03	UIPP

Parameter	Description	Min.	Typ.	Max.	Unit
t_{OPJIT_cyc}	Output Clock Cycle-to-Cycle Jitter (fOUT >=100MHz)			300	ps p-p
	Output Clock Cycle-to-Cycle Jitter (fOUT < 100MHz)			0.03	UIPP
t_{LOCK}	Lock time(5 – 320 MHz)			200	us
Input Clock Requirements					
t_{IPJIT_cyc}	Input Clock Cycle-to-Cycle Jitter (fPFD >=100MHz)			0.15	UIPP
	Input Clock Cycle-to-Cycle Jitter (fPFD <100MHz)			750	ps p-p
IN DUTY CYCLE	Input Clock Duty Cycle	40%		60%	-
OUT DUTY CYCLE	Output Clock Duty Cycle (CLKOUT1, at 50% Setting)	45%	50%	55%	-

4.4 DQS AC Characteristics Parameters

Single-step phase offset values of DQS phase adjustment are shown in the following table:

Table 4-10 DQS AC Characteristics

Symbol	Speed Grade	AC Characteristics Parameters Description			Unit
		Min.	Typ.	Max.	
DQS	-6	15	25	34	ps

4.5 Global Clock Network AC Characteristics Parameters

Table 4-11 Global Clock Network AC Characteristics

Symbol	Description	Maximum Frequency		Maximum SKEW	
		-5	-6	-5	-6
GLOBAL CLK	Global Clock Network	340MHZ	400MHZ	235PS	200PS

4.6 Regional Clock Network AC Characteristics Parameters

Table 4-12 Regional Clock Network AC Characteristics

Symbol	Description	Maximum Frequency		Maximum SKEW	
		-5	-6	-5	-6
REGIONAL CLK	Regional Clock Network	340MHZ	400MHZ	235PS	200PS

4.7 IO Clock Network AC Characteristics Parameters

Table 4-13 IO Clock Network AC Characteristics

Symbol	Description	Maximum Frequency		Maximum SKEW	
		-5	-6	-5	-6
IO CLK	IO Clock Network	400MHZ	470MHZ	71PS	60PS

4.8 Configuration and Programming of AC Characteristics Parameters

4.8.1 Power-up Timing Characteristics

Figure 4-1 Device Power-up Timing Characteristics

Note: Pulling "VCC/VCCAUX/VCCIOCFG" signal high indicates that all three power supplies have been powered up. If the recommended power-up sequence VCC>VCCAUX/VCCIOCFG is followed, then VCCAUX/VCCIOCFG has been powered up at the starting point of T_{POR}.

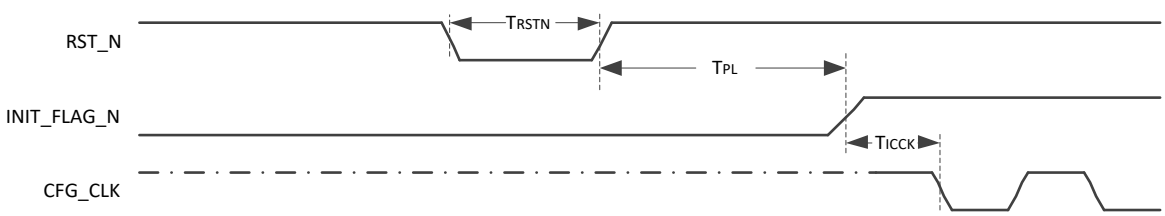

Figure 4-2 Device Reset and Reconfiguration of Timing Characteristics

Table 4-14 Power-up Timing Characteristics Parameters

Symbol	Description	Value	Property	Unit
T_{PL}	Program Latency	4.5	Max.	ms
T_{POR}	Power-up Reset	15	Max.	ms
T_{ICCK}	CFG_CLK Output Delay	400	Max.	ns
T_{RSTN}	RST_N Low Pulse Width	800	Min.	ns

Note: T_{ICCK} indicates the latest time by which the peer device, namely Flash, must ensure data can be read.

4.8.2 AC Characteristics of Each Download Mode

Table 4-15 AC Characteristics of Download Modes Supported by Logos Family FPGAs

Symbol	Symbol	AC Characteristics Parameters Description	Value	Unit	Property
JTAG	F_{TCK}	TCK Frequency	15	MHz	Max.
	T_{TCKH}	TCK Low Pulse Width	33	ns	Min.
	T_{TCKL}	TCK High Pulse Width	33	ns	Min.
	T_{TMSSU}/T_{TDISU}	TMS/TDI Setup Time (TCK Rising Edge)	4	ns	Min.
	T_{TMSH}	TMS Hold Time (TCK Rising Edge)	2	ns	Min.
	T_{TDIH}	TDI Hold Time (TCK Rising Edge)	7	ns	Min.
	$T_{TCK2TDO}$	TCK Falling Edge to TDO Output Valid	7	ns	Max.
Slave Serial	F_{SSCLK}	CFG_CLK Frequency	80	MHz	Max.
		CFG_CLK Frequency (Daisy Chain)	50	MHZ	Max.
	T_{SSCLKL}	CFG_CLK Low Pulse Width	6.25	ns	Min.
	T_{SSCLKH}	CFG_CLK High Pulse Width	6.25	ns	Min.
	$T_{SSINIT2CLK}$	INIT_FLAG_N Rising Edge to CLK Valid Time	200	us	Min.
	T_{SSDSU}	D[1] Setup Time (CFG_CLK Rising Edge)	2.5	ns	Min.
	T_{SSDH}	D[1] Hold Time (CFG_CLK Rising Edge)	1.5	ns	Min.
	T_{SSDSUF}	D[1] Setup Time (CFG_CLK Falling Edge)	2.5	ns	Min.
	T_{SSDHF}	D[1] Hold Time (CFG_CLK Falling Edge)	1.5	ns	Min.
	$T_{SSCLK2DOUT}$	CFG_CLK Falling Edge to DOUT_BUSY Output Valid	2/7.5	ns	Min./Max.
Slave Parallel	F_{SPCLK}	CFG_CLK Frequency	50	MHz	Max.
	T_{SPCLKL}	CFG_CLK Low Pulse Width	10	ns	Min.
	T_{SPCLKH}	CFG_CLK High Pulse Width	10	ns	Min.
	$T_{SPINIT2CS}$	INIT_FLAG_N Rising Edge to CS_N Pull Low Time	200	us	Min.
	T_{SPDSU}	D[31:0] Setup Time (CFG_CLK Rising Edge)	4.5	ns	Min.
	T_{SPDH}	D[31:0] Hold Time (CFG_CLK Rising Edge)	1.5	ns	Min.
	T_{SPCRSU}	CS_N/RDWR_N Setup Time (CFG_CLK Rising Edge)	3.5	ns	Min.
	T_{SPCRH}	CS_N/RDWR_N Hold Time (CFG_CLK Rising Edge)	1.5	ns	Min.
	$T_{SPCLK2D}$	CFG_CLK Rising Edge to D[31:0] Output Valid	9	ns	Max.

Symbol	Symbol	AC Characteristics Parameters Description	Value	Unit	Property
	$T_{SPCS2BUSY}$	CFG_CLK Rising Edge to BUSY Output Valid	8	ns	Max.
	$T_{SPCS2CSO}$	CS_N to CSO_N Output Delay	7	ns	Max.
Slave SPI	$F_{SSPICLK}$	CFG_CLK Frequency	100	MHz	Max.
	$T_{SSPICLKL}$	CFG_CLK Low Pulse Width	2.5	ns	Min.
	$T_{SSPICLKH}$	CFG_CLK High Pulse Width	2.5	ns	Min.
	$T_{SSPIINIT2CS}$	INIT_FLAG_N Rising Edge to CS_N Pull Low Time	200	us	Min.
	$T_{SSPICDSU}$	CS_N/D[3]/D[0] Setup Time (CFG_CLK Rising Edge)	3	ns	Min.
	$T_{SSPICDH}$	CS_N/D[3]/D[0] Hold Time (CFG_CLK Rising Edge)	1	ns	Min.
	$T_{SSPICLK2D}$	CFG_CLK Falling Edge to d[1] Output Valid	8	ns	Max.
	$T_{SSPICLK2DO}$	CFG_CLK Falling Edge to daisy_o Output Valid	8	ns	Max.
Master SPI	F_{MCLK}	CFG_CLK Frequency	50	MHz	Max.
	T_{MCLKD}	CFG_CLK Duty Cycle	45%/55%		Min./Max.
	$F_{MCLKTOL}$	CFG_CLK Frequency Deviation	20%		Max.
	T_{MDSU}	D[7:0] Setup Time (CFG_CLK Rising Edge)	8	ns	Min.
	T_{MDH}	D[7:0] Hold Time (CFG_CLK Rising Edge)	0	ns	Min.
	T_{MDSUF}	D[7:0] Setup Time (CFG_CLK Falling Edge)	8	ns	Min.
	T_{MDHF}	D[7:0] Hold Time (CFG_CLK Falling Edge)	0	ns	Min.
	T_{MCLK2D}	CFG_CLK Falling Edge to d[0]/d[4] Output Valid	2	ns	Max.
	$T_{MCLK2CS}$	CFG_CLK Falling Edge to fcs_n/fcs2_n Output Valid	2	ns	Max.
	$T_{MCLK2DOUT}$	CFG_CLK Falling Edge to daisy_o Output Valid	1	ns	Max.
Master BPI	F_{MBCLK}	CFG_CLK Frequency (Asynchronous Low Speed)	10	MHz	Max.
		CFG_CLK Frequency (Asynchronous High Speed)	33	MHz	Max.
		CFG_CLK Frequency (Synchronous Low Speed)	25	MHz	Max.
		CFG_CLK Frequency (Synchronous High Speed)	50	MHz	Max.
	T_{MBCLKD}	CFG_CLK Duty Cycle	45%/55%		Min./Max.
	$F_{MBCLKTOL}$	CFG_CLK Frequency Deviation	20%		Max.
	T_{MBDSU}	d[15:0] Setup Time (CFG_CLK Rising Edge)	8	ns	Min.
	T_{MBDH}	d[15:0] Hold Time (CFG_CLK Rising Edge)	0	ns	Min.
	T_{MBDSUF}	d[15:0] Setup Time (CFG_CLK Falling Edge)	8	ns	Min.
	T_{MBDHF}	d[15:0] Hold Time (CFG_CLK Falling Edge)	0	ns	Min.
	$T_{MBCLK2D}$	CFG_CLK Falling Edge to d[31:0]/adr[31:16] Output Valid	3	ns	Max.
	$T_{MBCLK2F}$	CFG_CLK Falling Edge to fce_n/fwe_n/foe_n/adv_n Output Valid	2	ns	Max.
	$T_{MBCLK2DO}$	CFG_CLK Falling Edge to daisy_o Output Valid	1	ns	Max.
Internal Parallel Slave Mode	F_{IPCLK}	IPAL_CLK Frequency	100	MHz	Max.
	T_{IPCLKL}	IPAL_CLK Low Pulse Width	2.5	ns	Min.
	T_{IPCLKH}	IPAL_CLK High Pulse Width	2.5	ns	Min.
	T_{IPDSU}	IPAL_CS_N/IPAL_RDWR_N/IPAL_DIN[31:0]	2	ns	Min.

Symbol	Symbol	AC Characteristics Parameters Description	Value	Unit	Property
		Setup Time (IPAL_CLK Rising Edge)			
	T_{IPDH}	IPAL_CS_N/IPAL_RDWR_N/IPAL_DIN[31:0] Hold Time (IPAL_CLK Rising Edge)	1	ns	Min.
	$T_{IPCLK2D}$	IPAL_CLK Rising Edge to IPAL_DOUT[31:0]/IPAL_BUSY Output Valid	4	ns	Max.
	$T_{IPCLK2V}$	IPAL_CLK Rising Edge to RBCRC_VALID/SEU_VALID Output Valid	2	ns	Max.
Master Internal SPI Mode	F_{IMCLK}	CFG_I_FCLK Frequency	70	MHz	Max.
	T_{IMCLKD}	CFG_I_FCLK Duty Cycle	45%/55%		Min./Max.
	$F_{IMCLKTOL}$	CFG_I_FCLK Frequency Deviation	20%		Max.
	T_{IMDSU}	i_d[3:0] Setup Time (CFG_I_FCLK Rising Edge)	6	ns	Min.
	T_{IMDH}	i_d[3:0] Hold Time (CFG_I_FCLK Rising Edge)	0	ns	Min.
	T_{IMDSUF}	i_d[3:0] Setup Time (CFG_I_FCLK Falling Edge)	6	ns	Min.
	T_{IMDHF}	i_d[3:0] Hold Time (CFG_I_FCLK Falling Edge)	0	ns	Min.
	$T_{IMCLK2D}$	CFG_I_FCLK Falling Edge to i_d[0] Output Valid	1	ns	Max.
	$T_{IMCLK2CS}$	CFG_I_FCLK Falling Edge to i_fcs_n Output Valid	1	ns	Max.

Chapter 5 Performance Parameters

This chapter lists the performance characteristics of common applications for Logos Family FPGAs.

5.1 LVDS Performance Parameters

Table 5-1 LVDS Performance

Description	IO Resources	Maximum Rate		Unit
		-5	-6	
DDR LVDS Transmitter	OSERDES(DATA _WIDTH =4,7TO 8)	680	800	Mbps
DDR LVDS Receiver	ISERDES(DATA _WIDTH =4,7 TO 8)	680	800	Mbps

5.2 MIPI Performance Parameters

Table 5-2 MIPI Performance

Description	Maximum Rate		Unit
	-5	-6	
MIPI Receiver	680	800	Mbps
MIPI Transmitter	680	800	Mbps

5.3 Memory Interface Performance Parameters

Table 5-3 Memory Interface Performance

Symbol	Description	Maximum Rate of Hard Core		Maximum Rate of Soft Core		Unit
		-5	-6	-5	-6	
DDR3	DDR3 Interface	667	800	667	800	Mbps
DDR2	DDR2 Interface	--	667	--	--	Mbps
DDR	DDR Interface	--	533	--	--	Mbps
LPDDR	LPDDR Interface	--	300	--	--	Mbps

5.4 DRM Performance Parameters

Table 5-4 DRM Performance

Symbol	Mode Description	Maximum Performance (MHz)	
		-5	-6
$F_{max\_DRM9K\_NW}$	DRM (NW mode & read register enabled) @ 9K memory mode	255	300
$F_{max\_DRM9K\_TW}$	DRM (TW mode & read register enabled) @ 9K memory mode	255	300
$F_{max\_DRM9K\_RBW}$	DRM (RBW mode & read register enabled) @ 9K memory mode	170	200
$F_{max\_DRM18K\_NW}$	DRM (NW mode & read register enabled) @ 18K memory mode	255	300
$F_{max\_DRM18K\_TW}$	DRM (TW mode & read register enabled) @ 18K memory mode	255	300
$F_{max\_DRM18K\_RBW}$	DRM (RBW mode & read register enabled) @ 18K memory mode	170	200
$F_{max\_DRM\_AFIFO}$	DRM (asynchronous FIFO mode & read register enabled)	233	275
$F_{max\_DRM\_SFIFO}$	DRM (synchronous FIFO mode & read register enabled)	233	275

5.5 APM Performance Parameters

Table 5-5 APM Performance

Condition	Maximum Performance (MHz)	
	-5	-6
All registers used (using registers at every stage of APM)	300	400
Only use INREG and PREG (only use APM's input and output registers)	170	200
No register used (no registers used)	85	100

Chapter 6 ADC Characteristics Parameters

This chapter mainly introduces the characteristic parameters of the ADC Hard core for Logos Family FPGAs, as shown in Table 6-1.

Table 6-1 ADC Hard Core Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
VCCAUX_A	Analogue Supply Voltage	2.97	3.3	3.63	V
VCC	Digital Supply Voltage	0.99	1.1	1.21	V
IVCCAUXA	Analogue Supply Current		1.5		mA
Resolution	Resolution		10		bit
Sample Rate	1M Mode		1		MSPS
	Default Scan Mode			0.015	MSPS
Channel	Channel			12	
Voltage Reference	Reference Voltage (Internal or External)		2.5		V
Offset Error	Offset Error (Bipolar)		±4		LSB
Gain Error	Gain Error (External Reference Voltage)		±0. 3		%FS
DNL	Differential Nonlinearity (when FS>=1V)		±1		LSB
INL	Integeral Nonlinear		±3		LSB
SNR	Signal to Noise Ratio (Bipolar Fully Differential Mode)	52			dB
Temperature Measurement	Temperature Sensing		-40~85 ℃: ±4; 85~105 ℃: ±6; 105~125 ℃: ±8;		℃

Note: The ADC's 1.1V digital power supply draws less current.

Chapter 7 High-Speed Serial Transceiver (HSST) Characteristics

This chapter mainly introduces the characteristics of the HSST Hard Core for Logos Family FPGAs, including absolute voltage/current rating limits, recommended operating conditions, AC/DC characteristics, and features under typical protocol operating modes.

7.1 HSST Hard Core Absolute Voltage Limits

Table 7-1 HSST Absolute Voltage Limits

Symbol	Min.	Max.	Unit	Description
VCCA_LANE	–0.16	1.32	V	HSST analogue power supply 1.2V voltage
VCCA_PLL_0	–0.16	1.32	V	HSST PLL analogue power supply 1.2V voltage
VCCA_PLL_1	–0.16	1.32	V	HSST PLL analogue power supply 1.2V voltage

Note: Exceeding the above ratings limits may cause permanent damage to the device.

7.2 Recommended Operating Conditions for HSST Hard Core

The following table shows the recommended operating voltages for the HSST Hard core of Logos Family FPGAs.

Table 7-2 Recommended Operating Conditions for HSST Hard Core

Symbol	Min.	Typ.	Max.	Unit	Description
Voltage Values					
VCCA_LANE	1.14	1.2	1.26	V	HSST analogue power supply 1.2V voltage
VCCA_PLL_0	1.14	1.2	1.26	V	HSST PLL analogue power supply 1.2V voltage
VCCA_PLL_0	1.14	1.2	1.26	V	HSST PLL analogue power supply 1.2V voltage

7.3 HSST Hard Core DC Characteristics Parameters

Table 7-3 HSST Hard Core DC Characteristics

Symbol	Min.	Typ.	Max.	Unit	Condition	Description
Input and Output Signals DC Characteristics						
HSST_VDINPP	300	-	1000	mV	External AC coupled	Differential input peak-to-peak voltage
HSST_VDIN	0	-	VCCA_LANE	mV	DC coupled, VCCA_LANE =1.2V	Input absolute voltage values

Symbol	Min.	Typ.	Max.	Unit	Condition	Description
HSST_VINCM	-	2/3 VCCA_LANE	-	mV	DC coupled, VCCA_LANE =1.2V	Common mode input voltage value
HSST_VDOUTPP	800	-	-	mV	Swing set to maximum	Differential output peak-to-peak voltage
HSST_VOUTCMDC	VCCA_LANE–HSST_VDOUTPP /4			mV	DC common mode output voltage, when the transmitter side is floating	
HSST_RDIN	-	100	-	Ω	Differential input resistance	
HSST_RDOUT	-	100	-	Ω	Differential output resistance	
HSST_TXSKEW	-	-	14	ps	Skew between P and N sides of TX output	
HSST_CDEXT	-	100	-	nF	Recommended external AC coupling capacitor value	
Reference Clock Input DC Characteristics						
HSST_VRCLKPP	400	-	1000	mV	Differential input peak-to-peak voltage	
HSST_RRCLK	-	100	-	Ω	Differential input resistance	
HSST_CRCLKEXT	-	100	-	nF	Recommended external AC coupling capacitor value	

7.4 High-Speed Serial Transceiver (HSST) AC Characteristics

The AC characteristics of the HSST Hard Core are shown in Table 7-4 to Table 7-9.

Table 7-4 HSST Hard Core Performance Parameters

Symbol	Grades	Unit	Description
	-6		
HSST_Fmax	6.375	Gbps	Maximum data rate of HSST
HSST_Fmin	0.6	Gbps	Minimum data rate of HSST
HSST_Fpllmax	3.1875	GHz	Maximum frequency of HSST PLL
HSST_Fpllmin	1	GHz	Minimum frequency of HSST PLL

The HSST reference clock switching characteristics are shown in the following table.

Table 7-5 HSST Hard Core Reference Clock Switching Characteristics

Symbol	Value			Unit	Condition	Description
	Min.	Typ.	Max.			
HSST_FREFCLK	60	-	625	MHz	Reference clock frequency range	
HSST_TRCLK	-	200	-	ps	20%-80%	Reference clock rise time
HSST_TFCLK	-	200	-	ps	80%-20%	Reference clock fall time
HSST_TRATIO	45	50	55	%	PLL	Reference clock duty cycle

Table 7-6 HSST Hard Core PLL/Lock Time Characteristics

Symbol	Value			Unit	Condition	Description
	Min.	Typ.	Max.			
HSST_TPLLLOCK	-	-	1.5	ms	From reset release to lock	PLL Lock Time
HSST_TCDRLOCK	-	60,000	2,500,000	UI	From PLL locking the reference clock and having data input to data lock	CDR Lock Time

The HSST Hard Core user clock switching characteristics are shown in the following table

Table 7-7 HSST Hard Core User Clock Switching Characteristics

Symbol	Frequency		Unit	Description
Data Interface Clock Switching Characteristics				
HSST_FT2C	160	MHz	Maximum frequency of P_CLK2CORE_TX	
HSST_FR2C	160	MHz	Maximum frequency of P_CLK2CORE_RX	
HSST_FTFC	160	MHz	Maximum frequency of P_TX_CLK_FR_CORE	
HSST_FRFC	160	MHz	Maximum frequency of P_RX_CLK_FR_CORE	
APB Dynamic Configuration Interface Clock Switching Characteristics				
HSST_FAPB	100	MHz	Maximum frequency of APB CLK	

The HSST Hard Core Transmitter side switch characteristics are shown in the following table.

Table 7-8 HSST Hard Core Transmitter Side Switching Characteristics

Symbol	Min.	Typ.	Max.	Unit	Condition	Description
HSST_T_{TXR}	-	100	-	ps	20%-80%	TX Rising Time
HSST_T_{TXF}	-	100	-	ps	80%-20%	TX Falling Time
HSST_T_{CHSKEW}	-	-	500	ps	-	TX channel-to-channel skew
HSST_$V_{TXIDLEAMP}$	-	-	30	mV	-	Electrical idle amplitude
HSST_$V_{TXIDLETIME}$	-	-	150	ns	-	Electrical idle transition time
HSST_$TJ_{0.6G}$	-	-	0.1	UI	0.6Gbps	Total Jitter
HSST_$DJ_{0.6G}$	-	-	0.05	UI		Deterministic Jitter
HSST_$TJ_{1.25G}$	-	-	0.15	UI	1.25Gbps	Total Jitter
HSST_$DJ_{1.25G}$	-	-	0.07	UI		Deterministic Jitter
HSST_$TJ_{2.5G}$	-	-	0.3	UI	2.5Gbps	Total Jitter
HSST_$DJ_{2.5G}$	-	-	0.15	UI		Deterministic Jitter
HSST_$TJ_{3.125G}$	-	-	0.3	UI	3.125Gbps	Total Jitter
HSST_$DJ_{3.125G}$	-	-	0.15	UI		Deterministic Jitter
HSST_$TJ_{5.0G}$	-	-	0.35	UI	5.0Gbps	Total Jitter
HSST_$DJ_{5.0G}$	-	-	0.17	UI		Deterministic Jitter
HSST_$TJ_{6.375G}$	-	-	0.4	UI	6.375Gbps	Total Jitter

Symbol	Min.	Typ.	Max.	Unit	Condition	Description
HSST_DJ$_{6.375G}$	-	-	0.15	UI		Deterministic Jitter

The HSST Hard Core Receiver side switching characteristics are shown in the following table.

Table 7-9 HSST Hard Core Receiver Side Switching Characteristics

Symbol	Min.	Typ.	Max.	Unit	Description
HSST_T$_{RXIDLETIME}$	-		255	TREFCLK	Time from RXELECIDLE state to LOS signal response
HSST_RX$_{VPPSIGDET}$	50	-	300	mV	Differential input signal detection threshold peak-to-peak value
HSST_RX$_{TRACK}$	-5000	-	0	ppm	Receiver spread spectrum following, 33kHz modulation frequency
HSST_RX$_{LENGTH}$	-	-	150	UI	Support for the length of RX continuous long 0 or long 1
HSST_RX$_{TOLERANCE}$	-1500	-	1500	ppm	Frequency deviation tolerance of data/reference clock
Sinusoidal jitter tolerance					
HSST_SJ_1.25	0.42	-	-	UI	Sinusoidal jitter[1], 1.25Gbps
HSST_SJ_2.5	0.42	-	-	UI	Sinusoidal jitter[1], 2.5Gbps
HSST_SJ_3.125	0.4	-	-	UI	Sinusoidal jitter[1], 3.125Gbps
HSST_SJ_5.0	0.4	-	-	UI	Sinusoidal jitter[1], 5.0Gbps
HSST_SJ_6.375	0.3	-	-	UI	Sinusoidal jitter[1], 6.375Gbps

Note:

1. The frequency of the injected sinusoidal jitter is 80MHz.

Chapter 8 PCIe Hard Core Features

Table 8-1 PCIe Performance Parameters

Symbol	Value	Unit	Description
Fpclk	250	MHz	Maximum Clock Frequency of PCIe Core
Fpclk_div2	125	MHz	Maximum Clock Frequency of User Interface

Note: For PCIe applications, the PCIe receiver differential input peak-to-peak voltage must meet the HSST_VDINPP value range.

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