Logos2 Family FPGAs Analog-to-Digital Converter (ADC) ModuleUser Guide

(UG040009, V1.6)

(19.07.2023)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.6	19.07.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
ADC	Analog to Digital Converter
SAR	Successive Approximation Register
N/A	Not Applicable
DRP	Dynamic Reconfiguration Port
MSPS	Mega Sample Per Second
APB	Advanced Peripheral Bus
JTAG	Joint Test Action Group
JDRP	JTAG Dynamic Reconfiguration Port
FS	Full-Scale
LSB	Least Significant Bit
OT	Over Temperature
IOB	Input Output Buffer

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Chapter 1 General Introduction

The Logos2 Family FPGA products provide an Analog-to-Digital Converter (ADC) module which includes two 12-bit SAR-ADC resources. The two ADC resources share up to 17 pairs of external input ports, including 16 pairs of analog input pins multiplexed with IOB and 1 pair of dedicated analog input pin. The scanning of 17 pairs of external input ports is flexibly controlled by the FPGA. Users can read and write the ADC's control register and read the ADC's status register through user logic. Meanwhile, the ADC can also monitor 4 sets of internal voltages in real-time, and the built-in temperature sensor can detect the chip junction temperature (Tj) in real-time, outputting overtemperature alarms based on preset thresholds. Below are some parameters of the ADC:

- Resolution: 12-bits;
- Sample rate: 1MSPS;
- Up to 17 pairs of external analog channels, including 16 pairs of analog input channels multiplexed with IOB and 1 pair of dedicated analog input channel (refer to the respective package manual for details)
- Internal and external reference voltage supported
- Integrated temperature sensor
- Integrated power supply sensor
- For detailed ADC characteristics parameters, please refer to the ADC section in the "DS04001 Logos2 Family FPGA Device Data Sheet"

ADC Module Analog Pin Description:

Table 1-1 Logos2 Family FPGA ADC Pin Description

Pin Name	Pin Type	Pin Description
VCCADC	Dedicated	ADC analog power supply 1.8V, connected to VCCA when ADC is not used
VSSADC	Dedicated	ADC AGND, connected to VSS when ADC is not used
VAADC_P	Dedicated	ADC dedicated analog differential input (Positive), left floating or connected to VSS when ADC is not used
VAADC_N	Dedicated	ADC dedicated analog differential input (Negative), left floating or connected to VSS when ADC is not used
VREFADC_P	Dedicated	1.255V reference voltage input, connected to VSS when not in use
VREFADC_N	Dedicated	1.255V reference ground input, connected to VSS when not in use
VAA[0,..,15]P, VAA[0,..,15]N	Multi-function	Multiplexed ADC differential analog input channels 0-15
TSDP	Dedicated	Anode pin of the temperature sensor diode; when the temperature diode is not used, connect to VSS; if the temperature sensor diode is used, an appropriate external temperature monitoring chip is required
TSDN	Dedicated	Cathode pin of the temperature sensor diode; when the temperature diode is not used, connect to VSS

Chapter 2 Detailed Introduction

2.1 ADC Structure Block Diagram

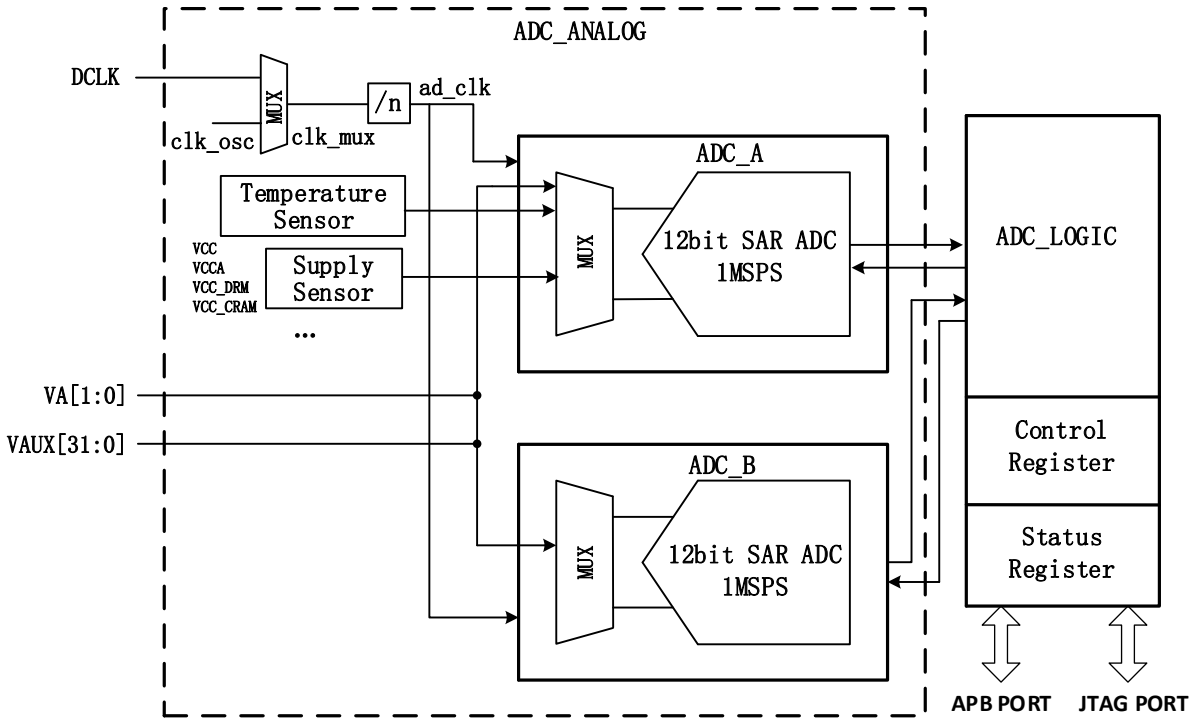

Figure 2-1 ADC Structure Block Diagram

The ADC includes up to 17 pairs of user-connectable analog input channels (where VAUX[31:0] is multiplexed with IOB and VA[1:0] are dedicated analog input channels). VAUX[1] and VAUX[0] correspond to the P and N sides of channel 0, so VAUX[31] and VAUX[30] correspond to the P and N sides of channel 15. For specific ports and description, please refer to Table 2-2 GTP_ADC_E2 Port List.

In Figure 2-1, the ADC_ANALOG module samples the analog input signal, converts it into 12-bit data, and transmits it to the ADC_LOGIC module. Users can read and write registers in ADC_LOGIC through the APB interface to control the ADC's working mode and read the ADC's status and conversion values.

2.2 Features

Table 2-1 List of ADC Features

Function	Description

Function	Description
Access registers via JTAG	Users can access and operate registers via JDRP
Access registers via APB	Users can access and operate registers via APB
Error calibration	Calibrate the ADC conversion values, including offset errors and gain errors
Chip monitoring	Monitor several on-chip power supply voltages and on-chip temperatures
Channel Scan	Sequentially scan and convert multiple ADC channels
Unipolar and Bipolar mixed scanning	The channels scanned by the ADC can be arbitrarily selected as unipolar, or bipolar
Result averaging	The ADC can average the obtained results
User event-driven	Users can control the sampling of the ADC through event-driven control
Single channel control	Users can arbitrarily select a channel for individual configuration
Chip monitoring during programming	Monitor the chip's voltage and temperature during programming

2.3 ADC Port Description

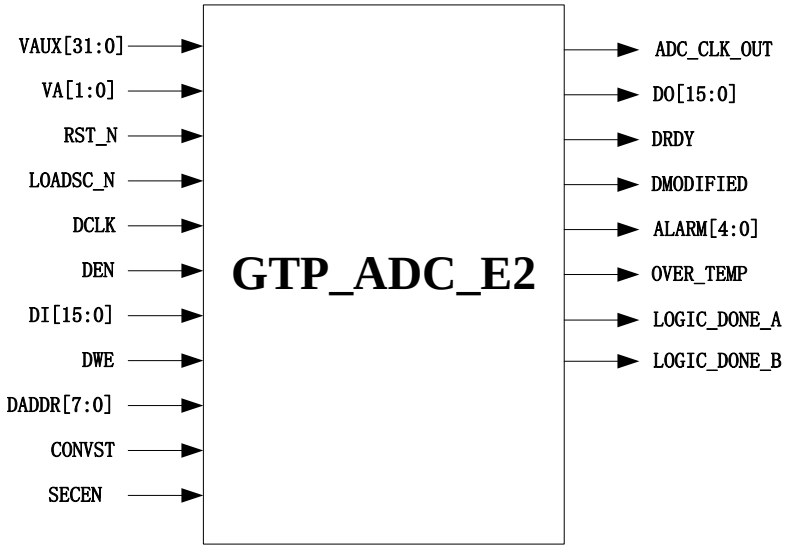

Figure 2-2 GTP_ADC_E2 Interface Diagram

The list of ADC GTP ports is as follows:

Table 2-2 GTP_ADC_E2 Port List

Port Name	I/O	Description
VA[1:0]	I	Dedicated analog input ports VA[1] and VA[0] form a differential pair, VA[0] is the N side, and VA[1] is the P side
VAUX[31:0]	I	Multiplexed analog differential input ports (Multiplexing IOB); IOB must be constrained to 1.8V power standard, and VAUX[2*n+1] and VAUX[2*n] form a differential pair, corresponding to the P and N sides of port n.
DCLK	I	APB interface clock
DADDR[7:0]	I	APB operation address bit

Port Name	I/O	Description
SECEN	I	Operation enable; initiates a read/write operation when active high
DEN	I	Data transfer enable signal
DWE	I	Write operation enable: 0 for read, 1 for write
DI[15:0]	I	APB data input
DO[15:0]	O	APB data output
DRDY	O	APB read/write complete flag
CONVST	I	Event-driven control signal, which triggers sampling in event-drive mode
RST_N	I	System reset signal, active-low
OVER_TEMP	O	OT (over temperature) indicator signal
LOGIC_DONE_A	O	ADC status register update signal
LOGIC_DONE_B	O	ADC status register update signal
LOADSC_N	I	Enable control register loaded into static configuration value signal, active low Triggers internal reconfiguration of the ADC control register. For specific usage, please refer to Figure 2-3
ADC_CLK_OUT	O	ADC working clock ad_clk output port
DMODIFIED	O	Control register modification flag, indicating that the control register has been written by JTAG and the user has not yet performed APB operation. After JTAG completes the write operation, the DMODIFIED signal is pulled high. The subsequent APB read/write operations will reset the DMODIFIED signal.
ALARM[4:0]	O	Alarm indicator signal ALARM[0] is the temperature alarm signal; ALARM[1] is the VCC alarm signal; ALARM[2] is the VCCA alarm signal; ALARM[3] is the VCC_CRAM alarm signal; ALARM[4] is the VCC_DRM alarm signal

Note: The timing of the LOADSC_N signal is shown in the following diagram:

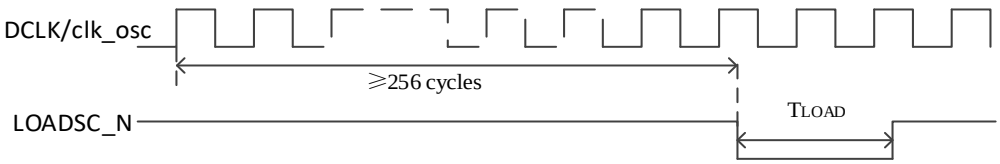

Figure 2-3 Timing Diagram of LOADSC_N Signal and DCLK/clk_osc

After at least 256 stable clock cycles, the LOADSC_N signal must held low for two or more clock cycles before pulling high, as shown in Figure 2-3.

The ADC clock can be selected through configuration registers. For details, please refer to CLKSW control bits.

When the ADC uses DCLK, the LOADSC_N signal must be pulled low to trigger ADC configuration loading. The time T_{LOAD} for which LOADSC_N is held low must be at least 2 DCLK cycles.

When the ADC uses internal clk_osc, the ADC configuration can be automatically loaded; if

reloading is needed, LOADSC_N must be pulled low for a time T_{LOAD} of at least 80ns.

2.4 ADC Analog Input

The ADC analog input uses differential sampling to reduce the impact of common-mode noise. All analog input channels are inherently differential, requiring the positive input (VP) and negative input (VN) of the ADC to be driven in differential mode.

When using dedicated ADC channels, the corresponding pins do not need to be constrained. Multi-funtion analog channel (VAUX[31:0]) pins are shared with general IO. When using multi-funtion analog channels, these pins cannot be used as general IO and must be constrained to the 1.8V level standard. Unused multiplexed analog channel pins can be used as general IO.

When detecting all on-chip sensors, the ADC operates in Unipolar mode; users may configure external analog input channels in either Unipolar or Bipolar mode. The Unipolar mode is shown in Figure 2-4:

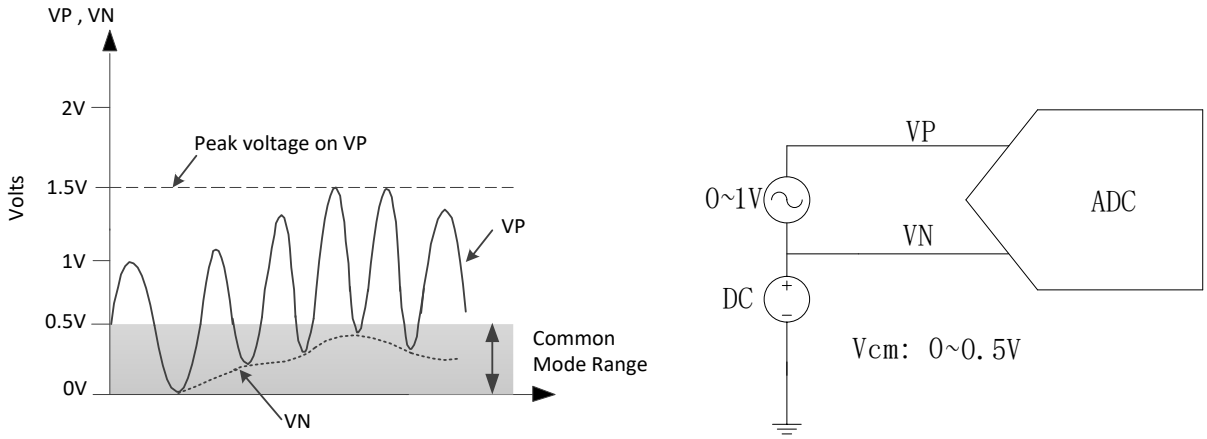

Figure 2-4 Unipolar Mode Input Diagram

In Unipolar mode, VP≥VN, VN input range is 0–0.5V, and 0V≤VP–VN≤1V.

The bipolar mode includes pseudo-differential and true differential, each illustrated in Figure 2-5, Figure 2-6:

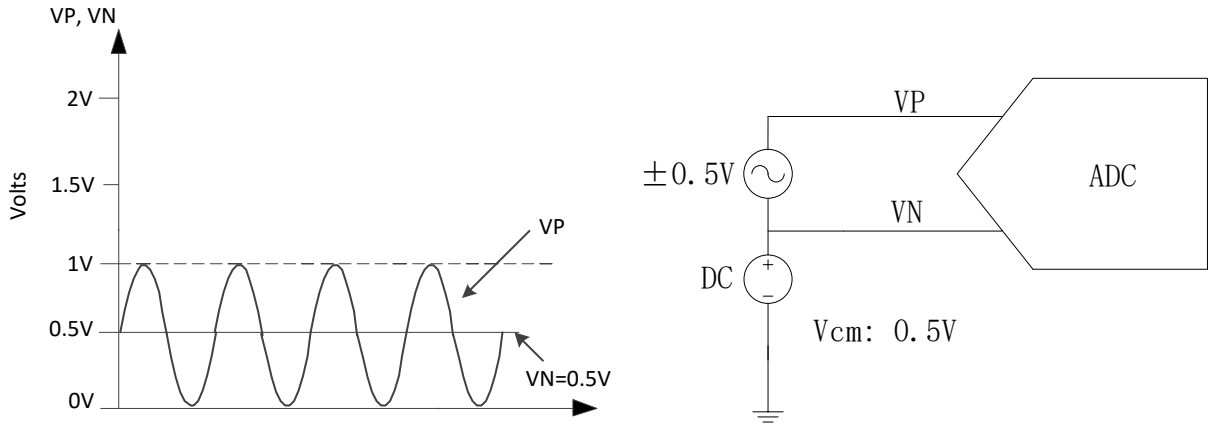

Figure 2-5 Bipolar Mode Pseudo-Differential Input Diagram

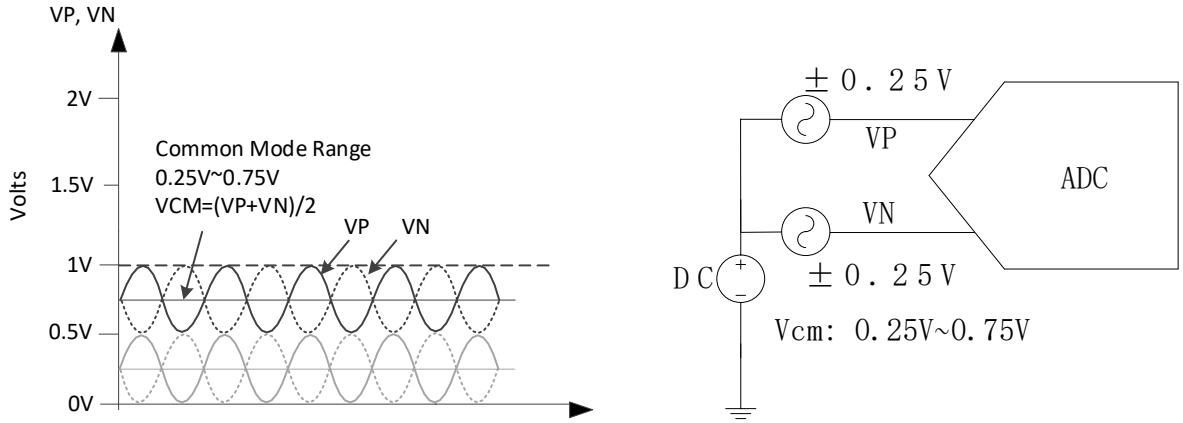

Figure 2-6 Bipolar Mode True Differential Input Diagram

To ensure proper conversion, the signal requirements for the above input modes are as follows:

Table 2-3 ADC Analog Input Signals

Mode	**VP**	**VN**
Unipolar	VN~(VN+1V)	0~0.5V
Bipolar (pseudo-differential)	0~1V	0.5V
Bipolar (true differential)[1]	Vcm+(±0.25V)	Vcm-(±0.25V)

Note:

1. Vcm refers to the common-mode voltage of the external input signal.

The mode configuration of different channels is implemented through the sequence register. For details, please refer to Table 2-9 Sequence Register List.

2.5 ADC Signal Conversion

The ADC can operate in different modes (Unipolar, Bipolar) with a default full-scale (FS) of 1V (non-adjustable). If various errors (including Offset error and Gain error) are not considered, the ADC conversion characteristics are as shown in the figure below:

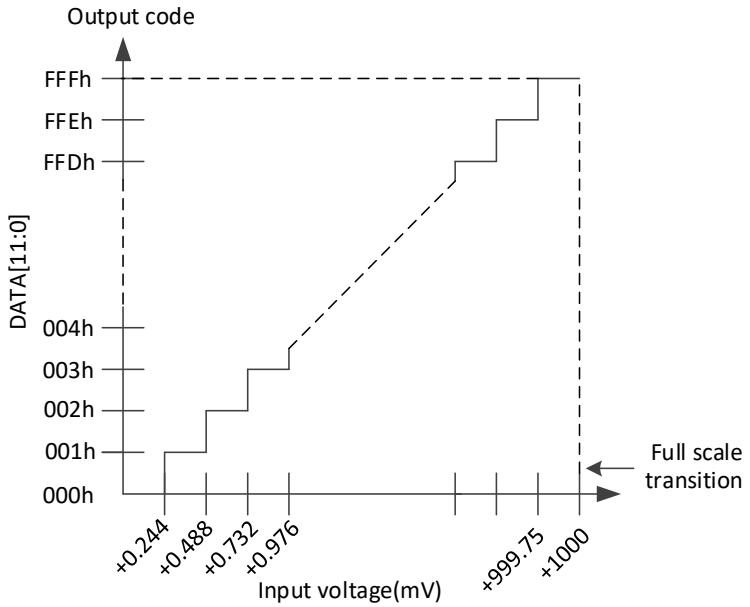

Figure 2-7 ADC Analog-to-Digital Conversion Chart in Unipolar Mode

Figure 2-7 shows the conversion curve under the measurement range of 0 to +1V (FS=1V) in unipolar mode. In this mode, the conversion code is an unsigned number, and LSB=1V/4096=0.244mV. Since the input channels are differential, the VP and VN terminals require differential signal driving. When the input voltage (VP-VN) is 0V, the output code is 000h (if Vp<Vn, then the output is 000h); when the input voltage (VP-VN) is 1V, the output code is FFFh (if Vp-Vn>1V, the output is FFFh).

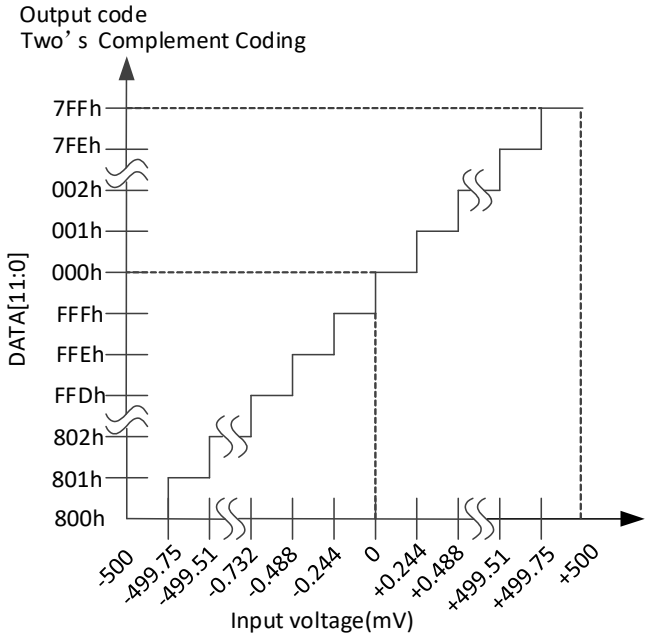

Figure 2-8 ADC Analog-to-Digital Conversion Chart in Bipolar Mode

Figure 2-8 shows the conversion curve in bipolar mode with a measurement range of -0.5V to +0.5V (FS=1V), where LSB=1V/4096=0.244mV. In this mode, the ADC conversion code is output as a two's complement. When the input voltage (VP-VN) is -500mV, the output code is 800h (the output is 800h when VP-VN< -500mV); when the input voltage is 0V (VP-VN=0V), the output code is 000h; when the input voltage (VP-VN) is +500mV, the output code is 7FFh (the output is 7FFh when VP-VN>500mV).

2.6 Temperature Monitoring

The ADC provides on-chip temperature monitoring function, with temperature detection achieved by measuring the voltage difference between two differently biased PN junctions. Its output voltage is:

$$V_{temp} = 6 * \ln(48) * \frac{kT}{q}$$

$k = 1.38 \times 10^{-23} J/K$ denotes the Boltzmann constant

$T = ℃ + 273.15$ denotes temperature in Kelvin

$q = 1.6 \times 10^{-19} C$ is electronic charge

When the temp sensor is operating, ADC_A samples the voltage output from the temp sensor by default; As a backup ADC, ADC-B does not perform sampling on the temp sensor; the ADC defaults to operating in Unipolar mode at this time, storing the conversion results at the 40h address bit in the status register.

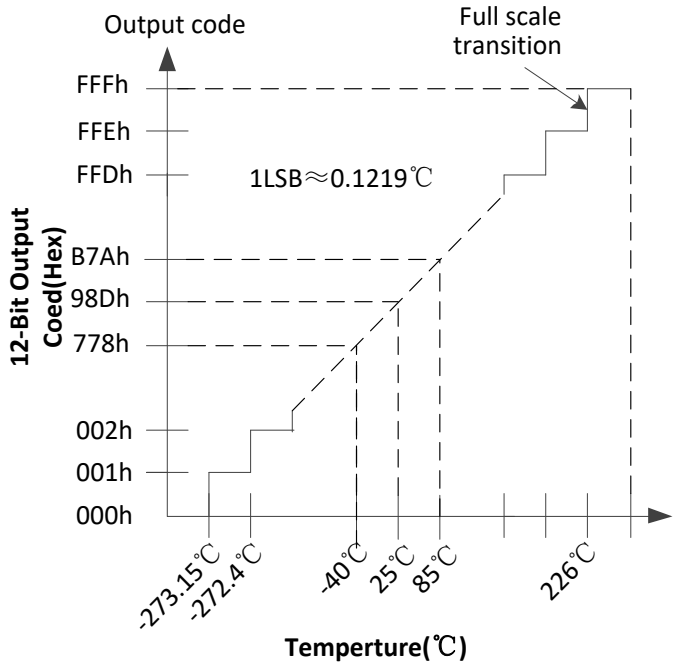

Figure 2-9 Temperature Sensor Conversion Characteristics

The temperature sensor inputs a voltage that is linearly related to the temperature to the ADC, converting it into an ADC output code, as shown in the figure above.

The on-chip temperature corresponding to the ADC output code is:

Temperature(℃) = ADC Code * 0.1219 – 273.15 (The ADC code is represented in hexadecimal format)

2.6.1 Over-temperature Alarm Function

When the internal temperature sensor reading exceeds the upper limit set in the alarm control register creg_20h, the ALARM [0] signal pulls high from 0 to 1 until the detected temperature value drops below the lower limit set in creg_21h, at which point the ALARM [0] signal pulls down from 1 to 0. The OT (over_temperature) signal is triggered in a manner similar to the ALARM [0] signal, with the difference that the temperature upper and lower limits for OT are generally larger than the upper and lower limits for ALARM [0] (corresponding to the temperature alarm), as shown in Figure 2-10.

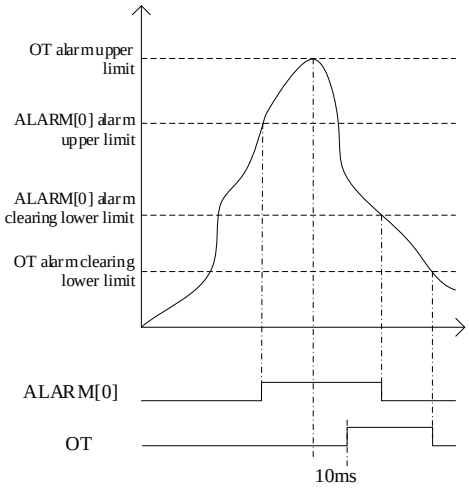

Figure 2-10 Overview of Over-temperature Alarm Function

To eliminate OT glitches, after the signal indicating over-temperature in the module is pulled high (continuous high level), an internal counter operating in the clk_mux clock domain begins counting, and OT only outputs a high level after counting to approximately 10ms. For control registers DB0 to DB2 (00h), please refer to the debounce counter description.

The default threshold upper limit for the over-temperature alarm is 125 ℃ (creg_2Ah=12'hCC2) and the lower limit is 50 ℃ (creg_2Bh=12'h A5B). Specific settings can be referred to in Table 2-11 Alarm Register List.

2.6.2 Temperature Calibration Function

The ADC of each device will undergo temperature offset calibration during the production testing phase of the Logos2 FPGA. The temperature sensor calibration must be conducted strictly at 25 ℃. The ADC first performs detection on the temperature sensor (two sampling settings of Avg=16 or 64 can be chosen, and the clock division is adjustable). The value tested under the current 25 ℃ condition is temp25, and the ADC calculates the Offset value: Offset_temp=98Eh-temp25. This Offset_temp value is written to the efuse via an internal configuration bus. Under normal operating conditions, when the ADC is performing temperature sensor monitoring, the ADC first detects the current temperature CODE, and then reads the Offset_temp value of the temperature sensor from the efuse. The actual result of the ADC's monitored temperature is: CODE_T=CODE – Offset_temp, and this value is sent to the user and software, with the final conversion result being:

Temperature(℃)=0.1219*(CODE_T)-273.15 (CODE_T is in hexadecimal format)

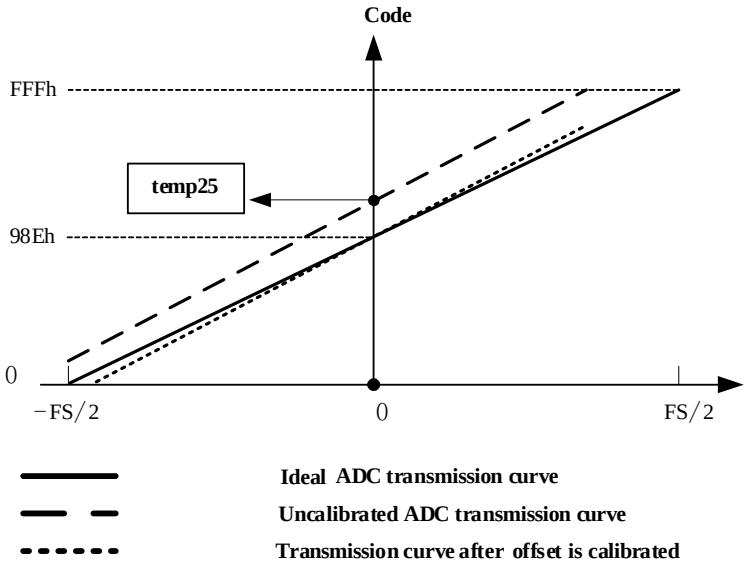

Figure 2-11 Temperature Offset Calibration Diagram

Under normal operating conditions, temperature calibration is performed automatically after power-up, and production devices provide temperature values after calibration.

2.7 Supply Voltage Monitoring

The ADC provides detection of on-chip voltages. The testable voltages are VCC, VCCA, VCC_DRM, and VCC_CRAM, with standard input values of 1V±5%, 1.8V±5%, 1V±5%, and 1.25V±5%, respectively; therefore, voltage division is required before testing.

Table 2-4 Typical Voltage Monitored by Voltage Sensor

on-chip Voltage	Value Before Voltage Dividing (V)			Value After Voltage Dividing (V)			Voltage Dividing Ratio
	Min	Typical	Max	Min	Typical	Max	
VCC	0.950	1.000	1.050	0.316	0.333	0.350	1/3
VCCA	1.710	1.800	1.890	0.570	0.600	0.630	1/3
VCC_DRM	0.950	1.000	1.050	0.316	0.333	0.350	1/3
VCC_CRAM	1.200	1.250	1.300	0.400	0.417	0.430	1/3

Operate in Unipolar mode by default. The ADC divides the input supply voltage by 1/3. The conversion formula is:

Voltage=ADC Code/4096*3V

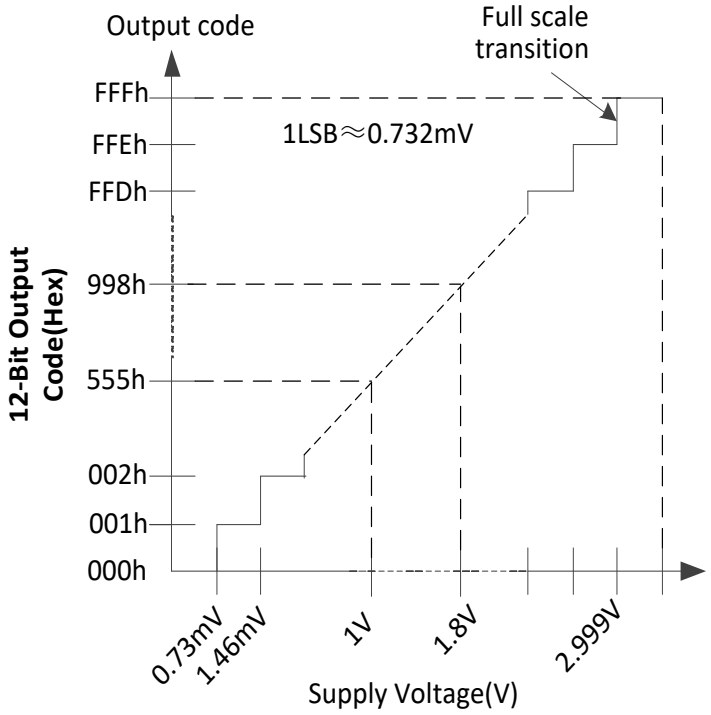

Figure 2-12 Ideal Voltage Sensor Conversion Characteristics

2.8 Register Description

Figure 2-13 shows the register interface for the ADC. There are two types of registers in the ADC: control registers and status registers. The value of the control register can be configured with initial values via parameters, and all registers can be accessed through APB or JTAG. The control register contains various control operations for the ADC and can be read and written; the status register stores the results of the ADC conversion calculations and is read-only.

After loading, the ADC will import user-configured parameters into the corresponding control registers, which can be accessed and modified via the APB interface or JTAG.

The default values of each register are based on the "UG040007 Logos2 Family Products GTP User Guide".

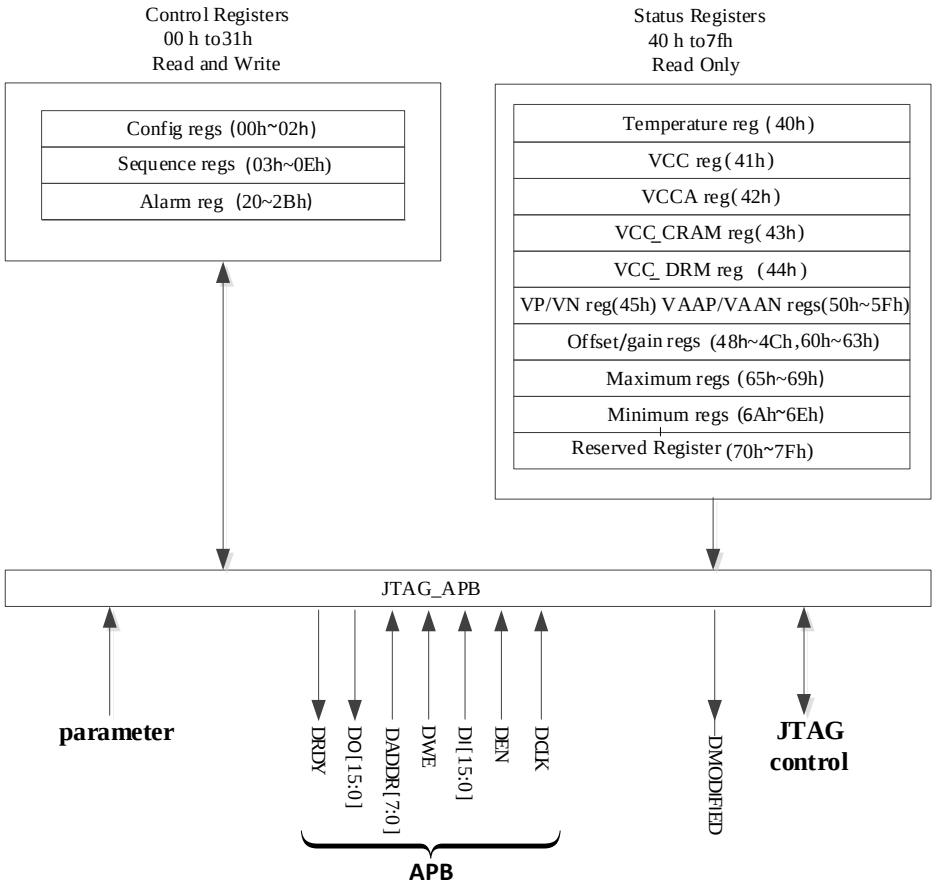

Figure 2-13 Register Interface

2.8.1 Control Registers

The ADC has 24 control registers. For address mapping, please refer to Table 2-5. These register configurations are used for specific operations of the ADC and can be read and written. All ADC functions are controlled through these registers. The control registers primarily have 3 functions:

1. Set the working mode of the Logos2 ADC, such as clock frequency, ADC_A/B status, and the alarm indicator switch.
2. Select the scanning channel, the corresponding bipolar or unipolar mode, and whether to enable averaging.
3. Set the maximum and minimum thresholds for voltage and on-chip temperature.

Table 2-5 Control Register Address Description

Address	**Description**
Configuration register	
00h	creg_00h[15:0]
01h	creg_01h[15:0]
02h	creg_02h[15:0]
Sequence Register	

Address	Description
03h	creg_03h[15:0]
04h	creg_04h[15:0]
05h	creg_05h[15:0]
06h	creg_06h[15:0]
07h	creg_07h[15:0]
08h	creg_08h[15:0]
10h	creg_0Ah[15:0]
12h	creg_0Ch[15:0]
14h	creg_0Eh[15:0]
Alarm Control Register	
20-2Bh	creg_20h~creg_2Bh[11:0]

2.8.1.1 Configuration Register

The configuration register (00h-02h) is used for specific configurations of some internal modules of the ADC. The value of the configuration register can be modified through APB or JTAG during the proper operation of the ADC. The specific definition of each bit is shown in Table 2-6.

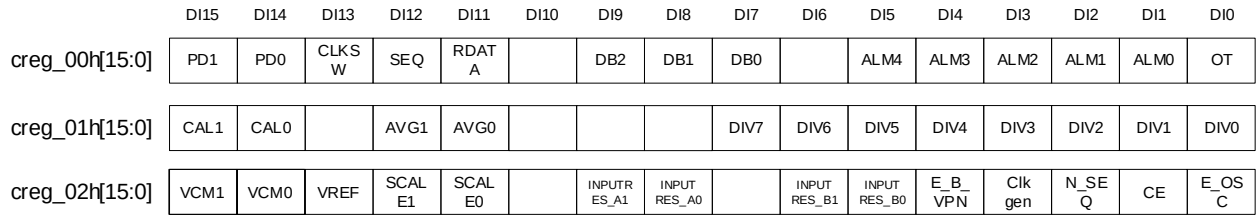

Figure 2-14 Configuration Register Bit Allocation

Table 2-6 Configuration Register List

Bit	Item	Read/ Write	Description
creg_00h			
DI15 to DI14	PD1 to PD0	R/W	Power-down control bit, ADC_PD [PD1: PD0] 00: Default, all modules powered up 01: Reserved 10: ADC B powered down 11: All modules powered down
DI13	CLKSW[1]	R/W	Clock source switch control bit: 1: The system selects the DCLK of the APB interface for clock division to generate ad_clk 0: The system selects clk_osc for clock division to generate ad_clk
DI12	SEQ	R/W	Scanning mode selection bit: 1: Sequential scan mode 0: Power-up mode
DI11	RDATA	R/W	Flag bit for bypassing error calibration process, meaning that data is stored directly in the status register. This function is not supported for

Bit	Item	Read/ Write	Description
			temperature and power voltage detection. 1: Valid, error calibration bypassed 0: Invalid
DI9 to DI7	DB2 to DB0	R/W	Set the debounce counter value for the over_temp signal. For details, please refer to Table 2-7 OT Signal Debounce Counter
DI5	ALM4	R/W	VCC_DRM voltage alarm output enable control bit: 1: Enable alarm 0: Disable alarm
DI4	ALM3	R/W	VCC_CRAM voltage alarm output enable control bit: 1: Enable alarm 0: Disable alarm
DI3	ALM2	R/W	VCCA voltage alarm output enable control bit: 1: Enable alarm 0: Disable alarm
DI2	ALM1	R/W	VCC voltage alarm output enable control bit: 1: Enable alarm 0: Disable alarm
DI1	ALM0	R/W	Temperature alarm output enable control bit: 1: Enable alarm 0: Disable alarm
DI0	OT	R/W	Over-temperature enable flag bit (active-high)
creg_01h			
DI15 to DI14	CAL1 to CAL0[2]	R/W	Calibration control configuration, [CAL1:CAL0] 00: Disable offset and Gain calibration 01: Enable offset calibration 10: Enable gain calibration; Only valid in debug mode, invalid for custom setting 11: Enable offset and Gain calibration
DI12 to DI11	AVG1 to AVG0[2]	R/W	ADC average control bit [AVG1:AVG0] 00: Non-averaging 01: Averaging over 16 samples 10: Averaging over 64 samples 11: Averaging over 256 samples Note that in 2-channel mode, the non-averaging setting ([AVG1:AVG0]=2'b00) is not supported when using division by 2.
DI9 to DI8	CD1 to CD0	R/W	Control the clock divider during the calibration sampling process [CD1:CD0] 00: Calibration clock division factor is 16 01: Calibration clock division factor is 16 10: Calibration clock division factor is 32 11: Calibration clock division factor is 64
DI7 to DI0	DIVA7 to DIVA0	R/W	Clock division signal for ADC. For details, please refer to Table 2-8 Clock Division Control
creg_02h			
DI15 to DI14	VCM1 to VCM0	R/W	Reserved, maintain the fixed value 00.
DI13	VREF[2]	R/W	Select reference source for ADC 0: Internal reference source 1: External reference source
DI12 to DI11	SCALE[1] to SCALE[0]	R/W	Reserved, maintain the fixed value 00.

Bit	Item	Read/ Write	Description
DI9 to DI8	INPUT_RESA[1] to INPUT_RESA[0]	R/W	Reserved, maintain the fixed value 00.
DI6 to DI5	INPUT_RESB[1] to INPUT_RESB[0]	R/W	Reserved, maintain the fixed value 00.
DI4	E_B_VPN	R/W	ADC_B enable signal for scanning dedicated channels: 0: creg_03h/05h/07h[14] controls ADC_A's scanning of dedicated channels; 1: creg_03h/05h/07h[14] controls ADC_B's scanning of dedicated channels.
DI3	CLKGEN	R/W	Clock generation enable signal
DI2	N_SEQ	R/W	Control bit used to generate the scan signal in event-driven sampling state.
DI1	CE	R/W	Continuous sampling mode and event-driven sampling mode selection bit 0: Continuous sampling 1: Event-driven sampling
DI0	E_OSC	R/W	Built-in clk_osc switch enable signal 0: Control the clk_osc switch according to the system's clkswitch and PD0 control bit; 1: clk_osc is always on, unaffected by other signals.

Notes:

1. When the user selects DCLK, the ADC configuration loading is triggered upon receiving the LOADSC_N signal at a low level. For detailed timing of the LOADSC_N signal, please refer to Figure 2-3; when the user selects clk_osc, the ADC configuration can be automatically loaded.
2. To meet the detection accuracy requirements for on-chip temperature and on-chip supply voltage with -40°C ≤ Tj ≤ 100°C, it is necessary to enable offset and gain calibration, average 64 samples or 256 samples, and simultaneously use an external high-precision VREF voltage. The external VREF should be maintained within the range of 1.255V ±0.2%.

Table 2-7 OT Signal Debounce Counter

CLKSW Configuration	DB2	DB1	DB0	Corresponding Source Clock Cycle	Corresponding Counter Size
1, DCLK	0	0	0	1000ns>DCLK cycle≥850ns	20'h 03000
1, DCLK	0	0	1	850ns>DCLK cycle≥650ns	20'h 04000
1, DCLK	0	1	0	650ns>DCLK cycle≥500ns	20'h 05000
1, DCLK	0	1	1	500ns>DCLK cycle≥300ns	20'h 09000
1, DCLK	1	0	0	300ns>DCLK cycle≥150ns	20'h 20000
1, DCLK	1	0	1	150ns>DCLK cycle≥50ns	20'h 40000
1, DCLK	1	1	0	50ns>DCLK cycle≥10ns	20'h F5000
1, DCLK	1	1	1	N/A	N/A
0, clk_osc	X	X	X	clk_osc cycle 20ns	20'h 80000

Note: To eliminate OT signal glitches, when the temperature exceeds the threshold of creg_2Ah, the ADC internal counter starts counting. The counter size is set through DB2~DB0 based on the source clock frequency. When the count value reaches its upper limit, the OT signal outputs high level.

Table 2-8 Clock Division Control

DIVA7	DIVA6	DIVA5	DIVA4	DIVA3	DIVA2	DIVA1	DIVA0	Division Ratio

DIVA7	DIVA6	DIVA5	DIVA4	DIVA3	DIVA2	DIVA1	DIVA0	Division Ratio
0	0	0	0	0	0	0	0	2
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	4
0	0	0	0	0	0	1	1	4
0	0	0	0	0	1	0	0	6
0	0	0	0	0	1	0	1	6
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	0	0	254
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	256
1	1	1	1	1	1	1	1	256

2.8.1.2 Sequence Register

Like the configuration register, the value of the sequence register can be modified through APB or JTAG at any time during the proper operation of the ADC. The definition of each bit is shown in Table 2-9.

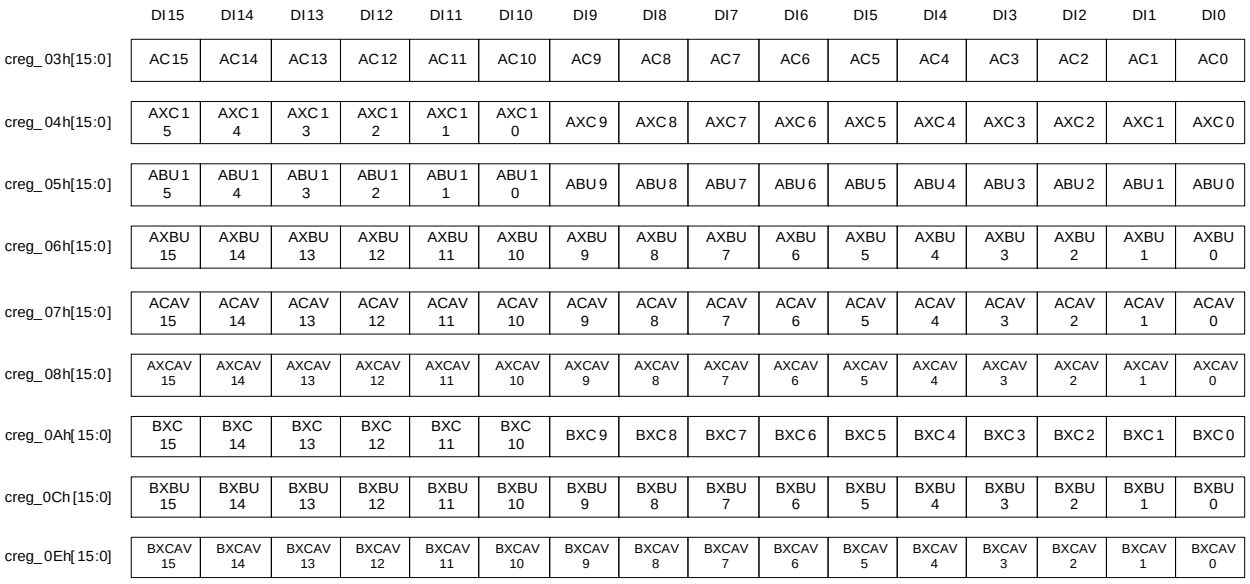

Figure 2-15 Sequence Register Bit Allocation

Table 2-9 Sequence Register List

Bit	Item	Read/ Write	Description
creg_03h			
DI0~DI15	AC0~AC15	R/W	ADC_A internal voltage, temperature and dedicated channel enable 1: Valid; 0: Invalid; For the correspondence between each bit and channel, please refer

Bit	Item	Read/ Write	Description
			to Table 2-10 Sequence Register Dedicated Channel Bit Mapping Relationship (ADC_B does not scan internal voltage, temperature)
creg_04h			
DI0~DI15	AXC0~AXC15	R/W	ADC_A external multiplex channel enable 1: Valid; 0: Invalid; DI0~15 correspond to multiplex channels 0~15
creg_05h			
DI0~DI15	ABU0~ABU15	R/W	ADC_A internal voltage, temperature and dedicated channel scan mode selection 1: Bipolar; 0: Unipolar; For the correspondence between each bit and channel please refer to Table 2-10 Sequence Register Dedicated Channel Bit Mapping Relationship
creg_06h			
DI0~DI15	AXBU0~AXBU15	R/W	ADC_A external multiplex channel scan mode selection 1: Bipolar; 0: Unipolar; DI0~15 correspond to multiplex channels 0~15
creg_07h			
DI0~DI15	ACAV0~ACAV15	R/W	ADC_A internal voltage, temperature and dedicated channel averaging mode selection 1: Valid; 0: Invalid; For the correspondence between each bit and channel please refer to Table 2-10 Sequence Register Dedicated Channel Bit Mapping Relationship
creg_08h			
DI0~DI15	AXCAV0~ AXCAV15	R/W	ADC_A external multiplex channel averaging mode selection 1: Valid; 0: Invalid; DI0~15 correspond to multiplex channels 0~15
creg_0Ah			
DI0~DI15	BXC0~BXC15	R/W	ADC_B external multiplex channel enable 1: Valid; 0: Invalid; DI0~15 correspond to multiplex channels 0~15
creg_0Ch			
DI0~DI15	BXBU0~BXBU15	R/W	ADC_B external multiplex channel scan mode selection 1: Bipolar; 0: Unipolar; DI0~15 correspond to multiplex channels 0~15
creg_0Eh			
DI0~DI15	BXCAV0~ BXCAV15	R/W	ADC_B external multiplex channel averaging mode selection 1: Valid; 0: Invalid; DI0~15 correspond to multiplex channels 0~15

Notes:

1. The channel modes and averaging control bits only take effect when the corresponding channel selection enables for creg_03/04/0Ah.

2. PG2L100H, currently does not support switching Unipolar/Bipolar mode during multi-channel switching; ADC_A or ADC_B channels only support being fully configured as Unipolar or Bipolar mode.

Table 2-10 Sequence Register Dedicated Channel Bit Mapping Relationship

Bit	**Corresponding Channel**	**Scan Mode**
0~1	For internal calibration use, not open	N/A
2	Temperature	Unipolar
3	VCC	Unipolar
4	VCCA	Unipolar
5	VCC_CRAM	Unipolar
6	VCC_DRM	Unipolar
7~8	For internal calibration use, not open	N/A
9~13	Not used	N/A
14	Dedicated channel	Unipolar/Bipolar
15	Not used	N/A

2.8.1.3 Alarm Registers

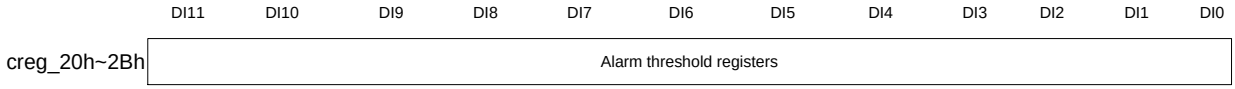

Figure 2-16 Alarm Register Bit Allocation

Table 2-11 Alarm Register List

Alarm Control	**Read/Write**	**Description**	**Corresponding Control Bit**
creg_20h	R/W	Temperature record alarm threshold upper limit setting	creg_00h ALM0 enable
creg_21h	R/W	Temperature record alarm threshold lower limit setting	
creg_22h	R/W	VCC record alarm threshold upper limit setting	creg_00h ALM1 enable
creg_23h	R/W	VCC record alarm threshold lower limit setting	
creg_24h	R/W	VCCA record alarm threshold upper limit setting	creg_00h ALM2 enable
creg_25h	R/W	VCCA record alarm threshold lower limit setting	
creg_26h	R/W	VCC_CRAM record alarm threshold upper limit setting	creg_00h ALM3 enable
creg_27h	R/W	VCC_CRAM record alarm threshold lower limit setting	
creg_28h	R/W	VCC_DRM record alarm threshold upper limit setting	creg_00h ALM4 enable
creg_29h	R/W	VCC_DRM record alarm threshold lower limit setting	
creg_2Ah	R/W	Over-temperature alarm reporting upper limit setting	creg_00h OT enable
creg_2Bh	R/W	Over-temperature alarm clearing lower limit setting	

Note: The corresponding threshold settings take effect only after the corresponding control bits in creg_00h are enabled.

2.8.2 Status Registers

Status registers (40h to 6Eh) store the conversion results for each channel as well as the offset and gain error values for calibration. All status registers can only be read by the user and cannot be written to.

The following is the definition of each address bit in the status register:

Table 2-12 Status Register List

Address	Defaults	Read/Write	Description
40h	16'h 0000	RO	Converted temperature
41h	16'h 0000	RO	Converted VCC
42h	16'h 0000	RO	Converted VCCA
43h	16'h 0000	RO	Converted VCC_CRAM
44h	16'h 0000	RO	Converted VCC_DRM
45h	16'h 0000	RO	Converted dedicated channel VAADC_P/VAADC_N
46h	16'h 0000	RO	Converted calibration code0
47h	16'h 0000	RO	Converted calibration code1
48h	16'h 0000	RO	Converted ADC_A Offset (Unipolar)
49h	16'h 0000	RO	Converted ADC_A Offset (Bipolar)
4Ah	16'h 0000	RO	Converted ADC_A Gain (Unipolar)
4Bh	16'h 0000	RO	Converted ADC_A Gain (Bipolar)
4Ch	16'h 0000	RO	Converted ADC_A supply sensor Offset (Unipolar)
50-5Fh	16'h 0000	RO	Converted VAA[0:15]P/VAA[0:15] N——Multiplexed channel 0-15
60h	16'h 0000	RO	Converted ADC_B Offset (Unipolar)
61h	16'h 0000	RO	Converted ADC_B Offset (Bipolar)
62h	16'h 0000	RO	Converted ADC_B Gain (Unipolar)
63h	16'h 0000	RO	Converted ADC_B Gain (Bipolar)
65h	16'h 0000	RO	Temperature after the maximum conversion since the last power-up or reset
66h	16'h 0000	RO	VCC after the maximum conversion since the last power-up or reset
67h	16'h 0000	RO	VCCA after the maximum conversion since the last power-up or reset
68h	16'h 0000	RO	VCC_CRAM after the maximum conversion since the last power-up or reset
69h	16'h 0000	RO	VCC_DRM after the maximum conversion since the last power-up or reset
6Ah	16'h FFF0	RO	Temperature after the minimum conversion since the last power-up or reset
6Bh	16'h FFF0	RO	VCC after the minimum conversion since the last power-up or reset
6Ch	16'h FFF0	RO	VCCA after the minimum conversion since the last power-up or reset
6Dh	16'h FFF0	RO	VCC_CRAM after the minimum conversion since the last power-up or reset
6Eh	16'h FFF0	RO	VCC_DRM after the minimum conversion since the last power-up or reset

The following diagram explains the data format for each address bit in the status register:

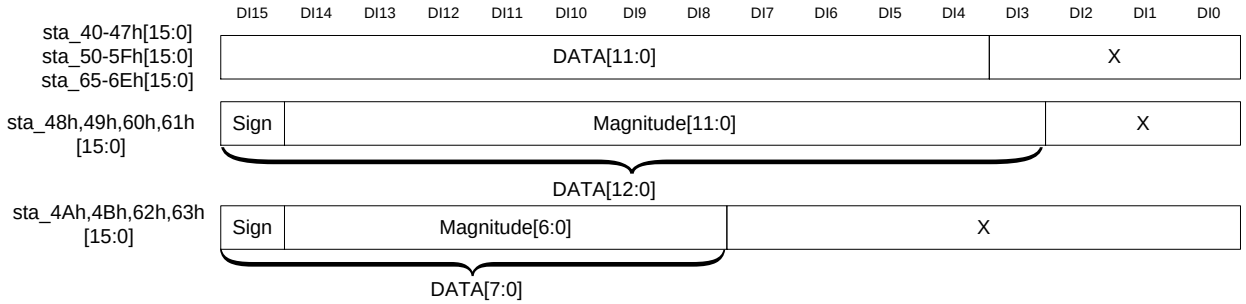

Figure 2-17 Status Register Data Structure Diagram

After each reset and power-up, the register storing the minimum value will be reset to FFFFh, and the register storing the maximum value will be reset to 0000h. Each signal detected must be compared with the set threshold values. If the detected value exceeds the upper limit, it will be stored in the corresponding maximum value register within the status registers. Similarly, if the detected value is below the lower limit, it will be stored in the corresponding minimum value register within the status registers.

For the value of the offset register, the upper 13 bits represent the significant digits, with the highest bit being the sign bit. If the ADC offset is -10 LSBs (10*-0.244mV=-2.44mV), the value stored in the offset register is -10 LSBs, i.e., FF6h, and the value recorded in the status register is 1111_1111_1011_0xxxb.

For the value of the gain register, the upper 8 bits represent the significant digits, with the highest bit being the sign bit. If the ADC gain is +1%, the gain register stores the value +1%, with the LSB being 0.1%. Thus 1% = 10*0.1%, and the register value is 0000_1010_xxxx_xxxxb. The maximum value recorded by the register is ±0.1%*63=±6.3%.

2.9 ADC Operating Modes

Logos2 ADC supports two working modes:

- Power-up mode, which detects on-chip voltages and temperature;
- Scan sequence mode, which scans selected channels based on the control register settings.

After power-up, glogen=0 (glogen is the system build indicator, glogen=0 means no build has been performed), the system automatically performs calibration and enters Power-Up Mode. When glogen=1 (after the system build), the system performs the corresponding mode or channel scan according to the settings in the control register.

In addition to power-up reset and active reset, a soft reset signal is generated when creg_00h and creg_01h are rewritten. When this reset occurs, the Logos2 ADC restarts to execute the newly

written modes. The values in the status register are not affected by this reset.

When both ADC_A and ADC_B are set to off in the control register, the ad_clk in the system will also be turned off to save power. When both ADC_A and ADC_B are set to off in the control register, the internal state process of the Logos2 ADC will be in a waiting state, and the values in the status register will remain unchanged. When ADC_A or ADC_B is turned on again, the internal state process of the Logos2 ADC will be reset and will start a new process according to the settings in the control register.

ADC_A can detect temperature and supply voltage, and scan external channels, while ADC_B can only scan external channels. When both ADC_A and ADC_B select the same external channel, the final result will be based on the scan result of ADC_A.

The Logos2 ADC is implemented independently using JTAG and APB. The read/write operations of the control register settings and data readout of the status register are all done via JTAG and APB.

When ADC_A/B is operating, the following points should be noted:

- Below is the timing diagram of the ADC converting analog signals into sampling data.

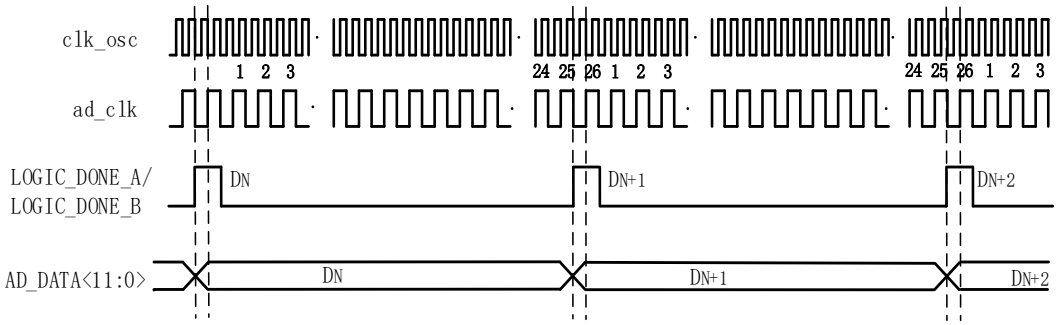

Figure 2-18 ADC Analog-to-Digital Conversion Timing Diagram

As shown in the above diagram, ad_clk is the ADC sampling clock, with the division factor controlled by DIVA7 to DIVA0 (configuration register, 01h). The LOGIC_DONE_A or LOGIC_DONE_B signal being pulled high indicates the completion of a conversion. A complete conversion cycle requires at least 26 ad_clk cycles. AD_DATA is a 12-bit internal conversion result stored in the corresponding status register for reading.

- When ADC_A/B transitions from the closed state to working mode, the ADC analogue requires time to stabilize the bias circuit. Therefore, from a timing perspective, the ADC enables the ADC_RSTN signal to wait for a period before entering the periodic reset release loop, or filter out initial data after ADC sampling. After ADC_A/B resumes operation, the bias circuit requires a stabilization time of 4096 ADC_CLK cycles. The timing requirements for ADC_A/B after power-down are shown in the following diagram:

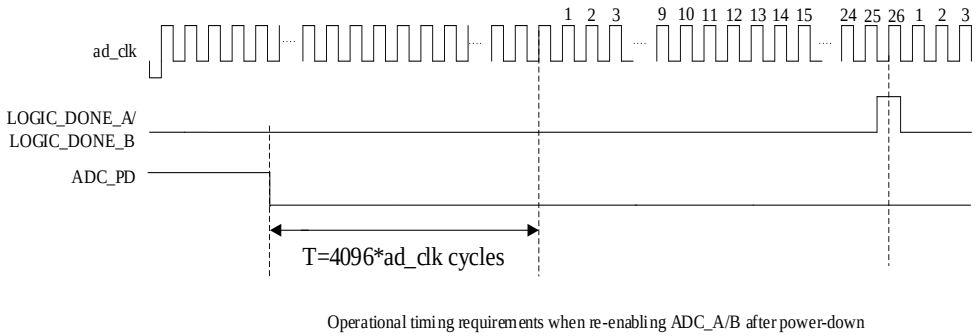

Figure 2-19 Timing Diagram for ADC_A/B Power-down then Power-up

After the ADC is powered down, ADC_A/B requires 4096 ad_clk cycles to stabilize. ADC_PD is the power-down control bit. For details, please refer to Table 2-6 Configuration Register List.

2.9.1 Power-up Mode

The main function of the power-up mode is to use on-chip detectors to detect internal voltage signals and temperature.

The ADC enters power-up mode in two cases. The first case is when the ADC is not configured, upon system power-up, the ADC automatically performs calibration and cycles without any regulation from the register. In this mode, the clock division is fixed to division by 32, data averaging occurs after 16 samples, and the internal reference voltage is used. At this time, an over-temperature indication signal (OT signal) is output, and no other alarm signals can be output. The other case is when the ADC is configured, it can enter power-up mode by setting the SEQ bit (creg_00h, DI12) in the configuration register to 1'b0. At this time the alarm signal can be output according to the control register settings.

The power-up mode has the following features:

- **Scan mode setting: Fixed to Unipolar mode**
- **Data averaging setting: Fixed to average = 16 times**
- **Event-driven mode disabled**
- **Scan order is Temperature->VCC->VCCA->VCC_CRAM->VCC_DRM**

2.9.2 Sequential Scanning Mode

The main function of the sequential scanning mode is to perform the configured scan on the selected channel, executing either a single scan or a cyclic scan.

The trigger, sampling frequency, corresponding scan channel, and scanning mode settings of the sequential scanning mode are all controlled by the control register. Whether calibration is performed

before executing the sequential scanning mode is also controlled by the control register. According to the configuration, it is possible to only scan ADC_A, or scan both ADC_A and ADC_A/B, or power down ADC_A/B simultaneously. ADC_A can scan on-chip temperature, voltage, dedicated channels, and multiplexed channels. ADC_B can only scan dedicated channels and multiplexed channels.

In sequential scanning mode, the alarm signal and OT signal can be enabled to detect if the internal temperature and voltage are within the threshold range.

When event-driven mode is configured in the control register, ADC_A/B enters a waiting state after completing the first scan, waiting for an event-driven signal to generate a pulse before executing another scan.

The following are several scan settings in sequential scanning mode:

- Single ADC_A scan; ADC_A performs the corresponding scan according to the control register settings. It is possible to scan a single channel or scan multiple channels at once.
- ADC_A and ADC_B scan different multiplexed channels in pairs (i.e., ADC_A scans channel 0, ADC_B scans channel 8), and both ADCs select the same number of multiplexed channels. At this time, ADC_A can still choose to scan internal temperature and voltage channels. When ADC_A scans temperature and voltage, ADC_B remains idle.
- ADC_A executes the power-up mode, and ADC_B selects multiplexed or dedicated channels. They perform scans independently. When using ADC_B to scan dedicated channels, the E_B_VPN control bit (creg_02h[DI4]) must be set to 1.

Example of the 1M sampling function:

- When using an external clock, set DCLK to 52MHz and clock division to 2. When the system scans only one channel with average_time=1 (no averaging), one sample is completed every 26 clock cycles, achieving a 1M sampling rate for the system.

Event-driven Mode Description:

When the event-driven mode is set in the control register, the Logos2 ADC will enter a waiting state after completing a scan. A new scan will only be executed after an external event_drv signal generates a pulse. In event driven mode, either an external or internal clock can be used. During sampling in event driven mode, the maximum sampling rate is 1/6M. If the trigger frequency is less than 1/6M, the sampling rate equals the trigger frequency; if the trigger frequency is greater than 1/6M, the sampling rate is 1/6M.

In non-event driven mode, the system scans the channel once every 26 clock cycles. In the event-driven mode, when event_drv is a periodic external pulse signal, its main function is to change the system's 1M scan to other frequencies.

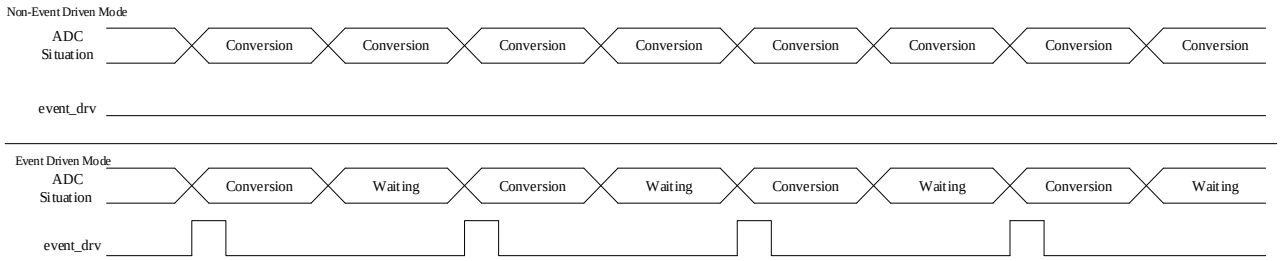

Figure 2-20 Function of the event_drv Signal in Event-driven Mode

If event_drv is not generated periodically and is triggered during the scan process, the trigger will be recorded. That is, after completing the current scan, the system will continue to perform another scan. Multiple triggers are considered as a single trigger. If the sequence register (seq_reg) changes before event_drv is triggered, the scan after the trigger will be based on the settings of the changed sequence register.

When the system is in the waiting state of event-driven mode, a new sequence register is written. When the N_SEQ (creg_02h[DI2]) control bit in the register is set to 1, the system will scan the newly written channel. After completing one scan, the system will return to the waiting state.

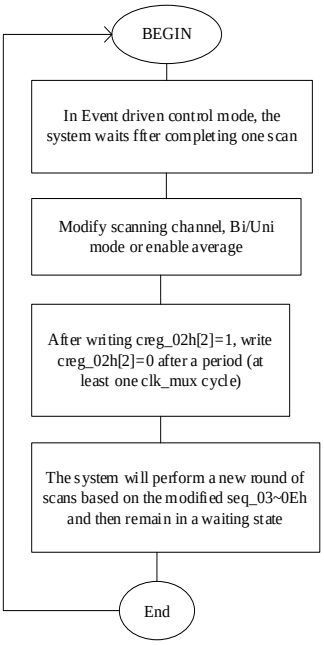

Figure 2-21 Flowchart for Modifying Sequence Register Functions in Event-driven Mode

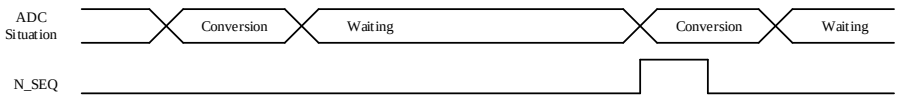

Figure 2-22 N_SEQ Function Implementation Flow and Waveform Diagram

If N_SEQ is triggered during the scan process, the trigger will be recorded. That is, after completing the current scan, the system will continue to perform another scan. Multiple triggers are considered as a single trigger. If the sequence register changes before N_SEQ is triggered, the scan after the trigger will be based on the settings of the changed sequence register.

2.10 JTAG and APB Interfaces of the ADC

Users can read and write the registers of the Logos2 ADC through the JTAG and APB interfaces. Since JTAG and APB are in parallel, there will be contention conflicts when writing simultaneously. Only either JTAG or APB is allowed to operate on the ADC at a time.

2.10.1 ADC JTAG Read/Write Timing

JTAG consists of two working modes: read and write. The data address bits during the read process and the address bits and data during the write process are determined by the input TDI. During the read process, the registers that can be read includes control registers and status registers. During the write process, the registers that can be written includes control registers.

The JTAG operation instructions are as follows:

Table 2-13 JTAG Operation Instructions

Bit	**Bit Definition**
[31:30]	Reserved
[29:26]	Op Code 0000: No operation 0101: Write operation 1010: Read operation Others: Undefined
[25:24]	Reserved
[23:16]	Address Addresses of the ADC's control and status registers
[15:0]	Data In write operations, data is written to the ADC's control registers In read operations, the data from the ADC's control and status registers is output

The JTAG command is a 32-bit word. When the state machine is in the data shift state, the data is serially shifted in from low to high bits by TDI. When the TAPC state machine is in the data update state, the data is latched to the parallel output of the APB register on the falling edge of TCK.

The diagram below describes the timing of JTAG Dynamic Reconfiguration Port (DRP) instructions:

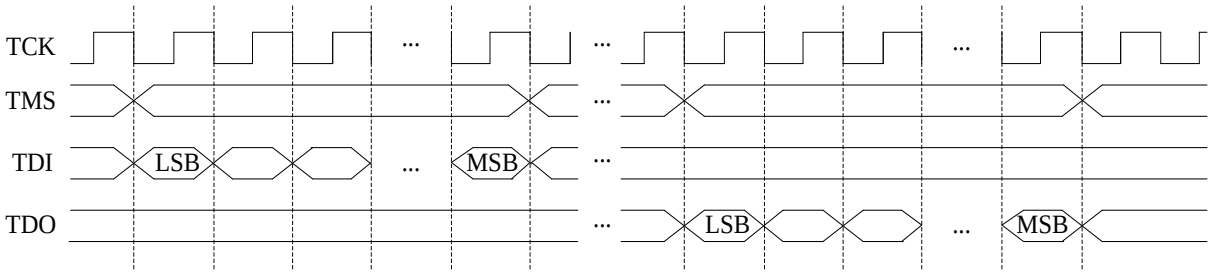

Figure 2-23 JTAG DRP Timing Diagram

2.10.2 ADC APB Read/Write Timing

Users can read and write the status registers and control registers through APB. DWE is an indicator signal for user write operations. When DWE is at a low level, logical write operations are prohibited. It should also be noted that the SECEN signal needs to be pulled low within one clock cycle after DRDY is pulled high, and the DEN signal should be pulled high at least 2 DCLK cycles before the SECEN signal. The read/write timing diagram is as follows:

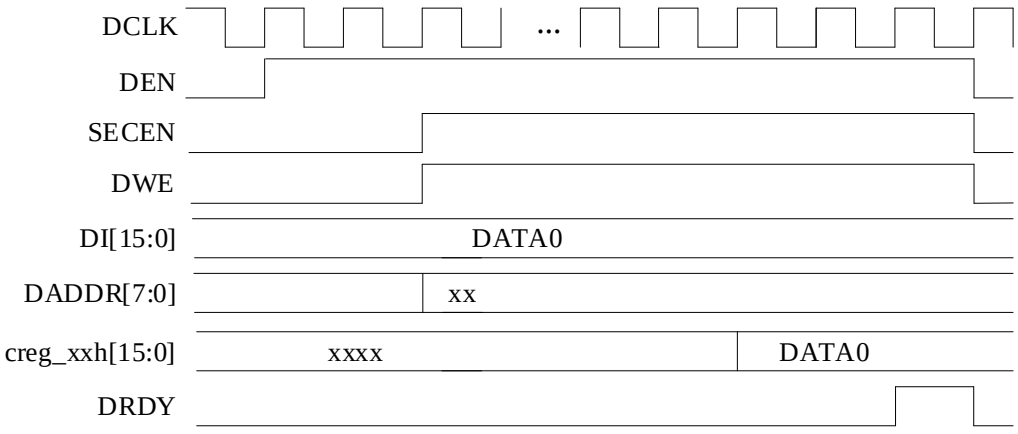

Figure 2-24 APB Write Register Timing Diagram

The diagram above shows the timing of the APB write process. After DRDY is pulled high, it indicates that the data has been written into the control register at the corresponding address.

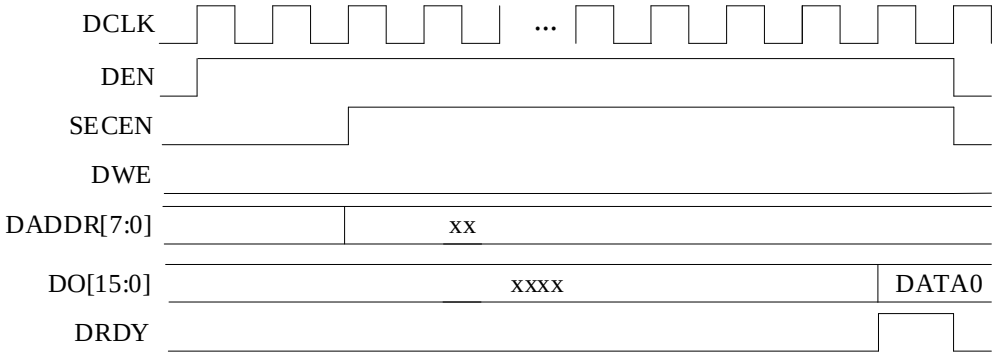

Figure 2-25 APB Read Register Timing Diagram

The above diagram is the timing diagram of the APB read process. After the DRDY signal is pulled high, the updated value of the register at the corresponding address can be read.

2.10.3 Description of Sampling and APB Read Tme in User Mode

The following explains the calculation for a single-channel 1M sampling.

Completing an APB read requires at least 7 DCLK cycles and 4 clk_mux cycles (clk_mux can be DCLK or clk_osc, decided by the user) to extract data from the status register.

During 1M sampling for a single channel, the clock division factor is 2. After LOGIC_DONE_A or LOGIC_DONE_B is pulled high, there are 7 ad_clk cycles (i.e., 14 clk_mux cycles) until the next scan ends and the first channel is overridden.

When the extreme condition 7*DCLK + 4*clk_mux < 14*clk_mux is met, the data can be read with 1M sampling between two LOGIC_DONE_A or LOGIC_DONE_B signals.

- When clk_mux = DCLK:

  The read time is 11 clk_mux cycles, and the minimum time to override the status register is 14 clk_mux cycles. At this time, the user can complete the extraction of system sampling data before the status register is overridden.

- When clk_mux = clk_osc,

$$7 * \mathrm{DCLK} + 4 * \mathrm{clk_{mux}} < 14 * \mathrm{clk_{mux}}$$

  The calculation result is:

$$\mathrm{F_{DCLK}} > 7 * \mathrm{F_{osc}}/10$$

According to the above calculation results, when the frequency of DCLK is greater than seven-tenths of the clk_osc frequency (i.e., greater than 36.4MHz), the user can complete the extraction of system sampling data before the status register is overridden.

Table 2-14 Clock Division and DCLK Frequency That Meet Data Sampling Requirements

Division Ratio	**Time Cycle from LOGIC_DONE_A or LOGIC_DONE_B Being Pulled High to the Status Register Being Overridden**	**DCLK Frequency to Complete Reading Before the Status Register is Overridden**
2	7 ad_clk, i.e., 14 clk_mux	FDCLK > 36.4MHz
4	15 ad_clk, i.e., 60 clk_mux	FDCLK > 6.5MHz
6	17 ad_clk, i.e., 102 clk_mux	FDCLK > 3.7MHz
8	18 ad_clk, i.e., 144 clk_mux	FDCLK > 2.6MHz
10	19 ad_clk, i.e., 190 clk_mux	FDCLK > 2MHz
12	20 ad_clk, i.e., 240 clk_mux	FDCLK > 1.6MHz
14	20 ad_clk, i.e., 280 clk_mux	FDCLK > 1.3MHz
16	20 ad_clk, i.e., 320 clk_mux	FDCLK > 1.2MHz
18	20 ad_clk, i.e., 360 clk_mux	FDCLK > 1MHz
20~256	20 ad_clk, i.e., 400~512 clk_mux	FDCLK≥1MHz

Description of changes in the number of channel scans:

Currently 11 channels are scanned, and then the user changes the number of scanned channels from 11 to 1. At this time, the time between the end of scanning 11 channels with LOGIC_DONE_A and LOGIC_DONE_B signals being pulled high and the end of scanning 1 channel with LOGIC_DONE_A or LOGIC_DONE_B signals being pulled high is not enough for the user to read out the data of all 11 channels. However, due to the reduction in the number of scans, the status registers corresponding to the channels that are not rescanned still maintain the original data. The user should be aware of this risk when changing the number of channel scans; one read before changing the control register is invalid, and the scan and read order should be consistent during sampling.

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