PK03028_PGC4KLS_SBG81

(V1.0)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	21.08.2020	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

The PGC4KLS_SBG81 device is packaged with a Wire Bond BGA. Its package size is 5x5mm, with 81 solder balls, a pitch of 0.5mm between the balls and a maximum package thickness of 0.86mm.

The PGC4KLS_SBG81 device internally encapsulates two pieces of PSRAM, powered by the dedicated power pin VCCIO1, with a supply voltage of 1.8V.

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Data

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	0.66	0.76	0.86	c	0.10	0.13	0.16
A1	0.08	0.13	0.18	e	-	0.5	-
A2	0.58	0.63	0.68	b	0.15	0.20	0.25
D	4.9	5.0	5.1	aaa	-	-	0.10
E	4.9	5.0	5.1	bbb	-	-	0.10
D1	-	4.0	-	ddd	-	-	0.08
E1	-	4.0	-	eee	-	-	0.15

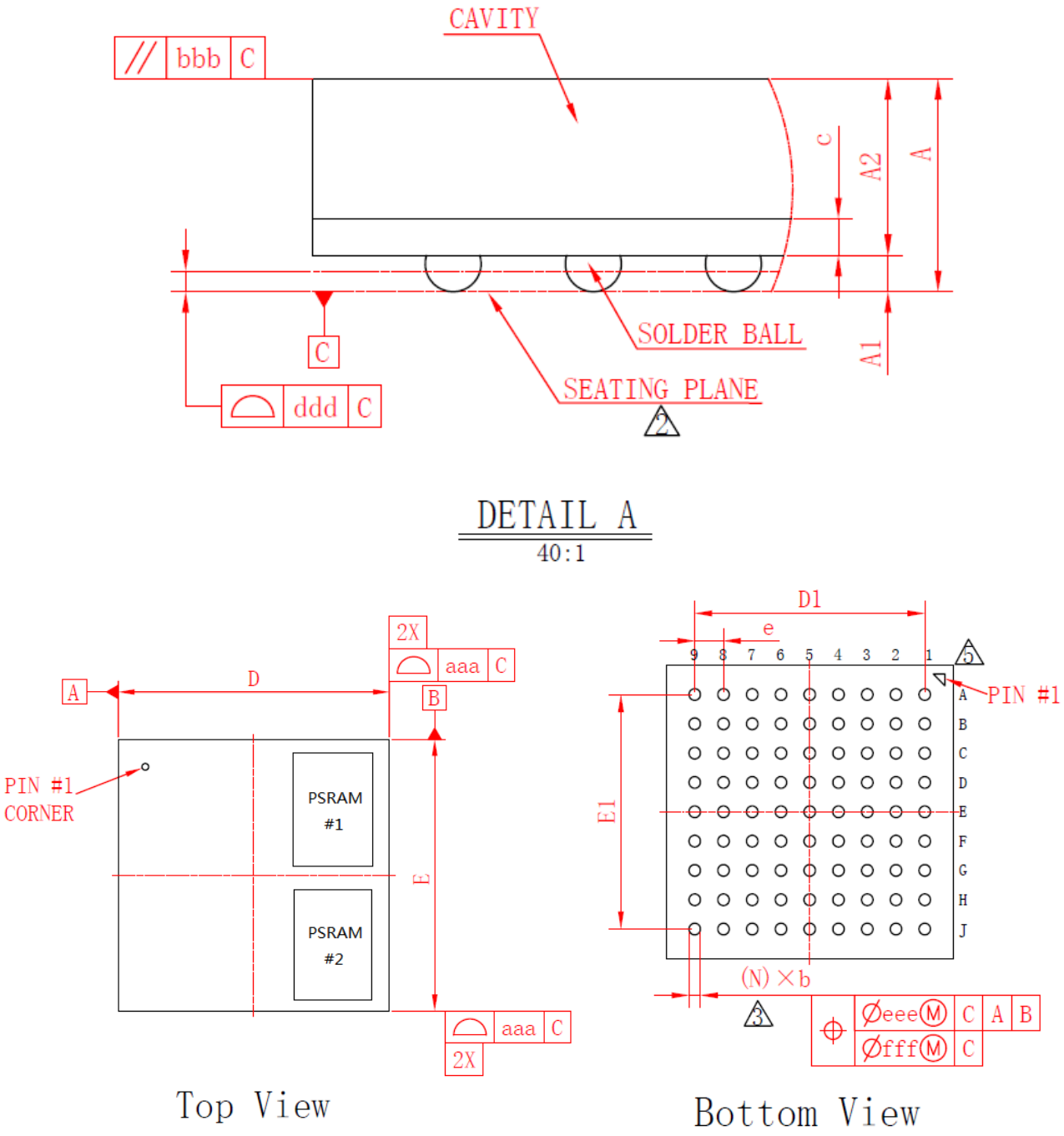

Figure 2-1 Package Outline Drawing (POD)

2.2 Pin Description

The PGC4KLS_SBG81 device has 55 user IOs.

Table 2-2 Device Pin Definitions

Pin Name	Pin Type	Direction	Pin Description
User I/O Pin			
DIFF[I,IO]_XX_NN[P,N]	User pin	Input/Output	User I/O. (1) DIFFI indicates support for differential signal input

Pin Name	Pin Type	Direction	Pin Description
			and pseudo-differential output; DIFFIO indicates support for differential signal input and true differential output, which can be used for transmitting and receiving LVDS signals; (2) “XX” denotes the Bank number, with possible values being B0, B1, B2, B3, B4, and B5; (3) “NN” denotes the sequence number of the programmable I/O group within the Bank, starting from 0 and increasing incrementally; (4) [P,N]: “P” denotes the positive side of the differential pair, and “N” denotes the negative side; During power-up, the user I/O is at a low voltage; After power-up is complete but before configuration, the general user I/O is at pull-down status; During configuration, the user I/O is at pull-down status;
Configuration[1]			
INIT_FLAG_N	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When used as a configuration pin: During power-up, it is at a low voltage; After power-up is complete before configuration, it is open-drain at weak pull-up status; During configuration, it is open-drain at weak pull-up status; During initialization, the pin can be driven to a low voltage by an external input to indicate an error or to delay configuration. During configuration, the pin serves as an indicator output for configuration errors, where a low voltage indicates an error has occurred;
CFG_DONE	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When it is used as configuration pin, it serves as an indicator output for configuration completion, where a high voltage indicates configuration is complete; Before or during configuration, the pin is driven to a low voltage; after configuration is complete, the pin can continue to be driven to a low voltage by an external source. If the internal start-up timing detects CFG_DONE at a low voltage, the internal start-up circuitry maintains its state until CFG_DONE goes high to continue the start-up process;
RSTN	Multi-function pin	Input	Configurable multiplexed reset pin, with an internal weak pull-up resistor. When it is used as a reset pin, it serves to restart the configuration process, active low. At this situation, it must be pulled up with an external resistor (internal weak pull-up resistor typically has a value of over 20kOhms, with a relatively weak pull-up strength); when the pin is at a low voltage, the CPLD enters reset state, with all I/Os in a weak pull-down status;
CFG_CLK	Multi-function pin	Input/Output	Configurable multiplexed clock pin, with an internal weak pull-up resistor. When it is used as a configuration pin: In slave SPI configuration mode, the pin serves as a clock input to acquire configuration data from an external source; In master SPI configuration mode, the pin serves as a clock output to acquire configuration data from an

Pin Name	Pin Type	Direction	Pin Description
			external source; in this mode, a 1kOhms pull-up resistor is needed; Master SPI mode and slave SPI mode are allowed to be enabled simultaneously, but using them at the same time is not permitted;
TCK	Multi-function pin	Input	Multiplexed JTAG test clock input pin; requires an external 4.7kOhms pull-down resistor;
TMS	Multi-function pin	Input	Multiplexed JTAG test mode select input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDI	Multi-function pin	Input	Multiplexed JTAG test data input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDO	Multi-function pin	Output	Multiplexed JTAG test data output pin; with an internal weak pull-up resistor, pulled up to VCCIO0.
JTAGEN	Multi-function pin	Input	Optional JTAG port behaviour control pin, usually used in user mode, when JTAG pins are configured as configuration I/Os, this pin is user I/O, with the state controlled by the user; when JTAG pins serve as user I/Os, JTAGEN serves as a dedicated input used to control the availability of JTAG pins; the default state is weak pull-down; when JTAGEN is configured as a dedicated I/O: (1) When at a low voltage, the JTAG pins function as user I/Os; (2) When at a high voltage, the JTAG pins function as JTAG configuration port.
FCS_N	Multi-function pin	Output	Configurable multiplexed pin, used for master SPI configuration mode, (1) In master SPI mode, outputs an active-low chip select signal to an external Flash; (2) After configuration is completed, it can be used as a user I/O.
MISO_SO	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MISO, serial data input in master SPI mode; (2) SO, serial data output in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
MOSI_SI	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MOSI, serial data output in master SPI mode; (2) SI, serial data input in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
FCSI_N	Multi-function pin	Input	Configurable multiplexed pin, with an internal weak pull-up resistor; In slave SPI mode, active-low chip select input.
SCL	Multi-function pin	Input (Open-drain)	Configurable multiplexed pin, clock input in slave I2C mode; requires an external weak pull-up resistor.
SDA	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, data input/output in I2C mode; requires an external weak pull-up resistor.
SPAL_CLK	Multi-function pin	Input	Clock input in slave parallel X16 configuration mode.

Pin Name	Pin Type	Direction	Pin Description
SPAL_CS_N	Multi-function pin	Input	Chip select input in slave parallel X16 configuration mode. Active-low
SPAL_RDWR_N	Multi-function pin	Input	Read/write control input in slave parallel X16 configuration mode; 1: read; 0: write.
SPAL_BUSY	Multi-function pin	Output	Busy indicator in slave parallel X16 configuration mode; During readback, if the data is not ready, SPAL_BUSY changes to high voltage.
SPAL_D15~SPAL_D0	Multi-function pin	Input/Output	Data bus in slave parallel X16 configuration mode.
Clock, PLL			
CLK[0,1,2][P,N]_[B0,B1,…,B5]	Multi-function pin	Input	Global clock input pin; can also be used as user I/O; (1) [0,1,2]: clock pin numbers; (2) [P,N]: positive and negative sides of the differential clock pins; (3) [B0,B1,…,B5]: bank numbers.
PLL[0,1]_CLKIN_[P,N]	Multi-function pin	Input	PLL input. PLL can choose to directly input a clock from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
PLL[0,1]_CLKFB_[P,N]	Multi-function pin	Input	Optional PLL feedback clock input. PLL can select to feedback clock externally from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
Power			
VCC		Power	External power supply of 1.2V, providing power to the core logic.
VCCIO[0,1,2,3,5]		Power	I/O Bank power.
VSS		Ground	Ground associated with VCC;
MIPI_CTRL	Dedicated		MIPI high-performance application control pin; when connected to 2.5V or 3.3V, the device supports high-performance MIPI transmission functions; when connected to VSS or left floating, the device does not support the high-performance MIPI transmission capabilities.

Note:

1. When the configured multi-function pin is used as a user I/O, its status is the same as the user I/O pin.

2.2.1 Pin Name list

Table 2-3 Pin Name List

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFI_B0_0N/CFG_DONE	B9	IO_1_N	22.3806
B0	DIFFI_B0_0P/INIT_FLAG_N	C9	IO_1_P	28.8754

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFIO_B0_1N/SPAL_CLK	D9	IO_2_N	31.9288
B0	DIFFIO_B0_1P/SPAL_CS_N	E9	IO_2_P	37.6232
B0	DIFFIO_B0_3N/SPAL_RDWR_N	F9	IO_4_N	48.1099
B0	DIFFIO_B0_3P/SPAL_BUSY	G9	IO_4_P	52.5409
B0	DIFFIO_B0_5N/SPAL_D15	D8	IO_6_N	33.7697
B0	DIFFIO_B0_5P/SPAL_D14	C8	IO_6_P	29.5766
B0	DIFFIO_B0_7N/SPAL_D13	A8	IO_8_N	19.3661
B0	DIFFIO_B0_7P/SPAL_D12	B7	IO_8_P	21.5661
B0	DIFFIO_B0_9N/SPAL_D9	A7	IO_10_N	17.1126
B0	DIFFIO_B0_9P/SPAL_D8	B6	IO_10_P	21.8601
B0	DIFFI_B0_10N/RSTN	C7	IO_11_N	28.9862
B0	DIFFI_B0_10P/JTAGEN	C6	IO_11_P	28.6193
B0	DIFFI_B0_16N/SDA/CLK0N_B0	G5	IO_17_N	46.4639
B0	DIFFI_B0_16P/SCL/CLK0P_B0	G4	IO_17_P	47.8518
B0	DIFFIO_B0_21N/CLK1N_B0	A5	IO_22_N	20.271
B0	DIFFIO_B0_21P/CLK1P_B0	A6	IO_22_P	28.4093
B0	DIFFI_B0_22N/TMS	C5	IO_23_N	29.7518
B0	DIFFI_B0_22P/TCK	C4	IO_23_P	27.1799
B0	DIFFI_B0_26N/TDI	A4	IO_27_N	20.5613
B0	DIFFI_B0_26P/TDO	B4	IO_27_P	23.2158
B0	DIFFIO_B0_31N	A3	IO_32_N	16.4978
B0	DIFFIO_B0_31P	B3	IO_32_P	21.6368
B0	DIFFIO_B0_33N	C3	IO_34_N	26.704
B0	DIFFIO_B0_33P	C2	IO_34_P	24.4344
B2	DIFFI_B2_1N/MOSI_SI	H9	IO_86_N	23.6993
B2	DIFFI_B2_1P/FCSI_N	J8	IO_86_P	16.1817
B2	DIFFI_B2_3N	F8	IO_88_N	33.3958
B2	DIFFI_B2_3P	F7	IO_88_P	33.3915
B2	DIFFI_B2_5N	G8	IO_90_N	27.607
B2	DIFFI_B2_5P	G7	IO_90_P	24.9444
B2	DIFFI_B2_7N	J7	IO_92_N	21.0655
B2	DIFFI_B2_7P	J6	IO_92_P	17.3524
B2	DIFFI_B2_15N/CLK1N_B2	H6	IO_100_N	21.1261
B2	DIFFI_B2_15P/CLK1P_B2	H7	IO_100_P	32.9557
B2	DIFFI_B2_21N/CLK0N_B2	J5	IO_106_N	20.3042
B2	DIFFI_B2_21P/CLK0P_B2	H4	IO_106_P	21.9502
B2	DIFFI_B2_27N/MISO_SO	J4	IO_112_N	21.11
B2	DIFFI_B2_27P/CFG_CLK	J3	IO_112_P	19.905

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B2	DIFFI_B2_33P/FCS_N	J2	IO_118_P	16.3417
B3	DIFFI_B3_2P	G1	IO_129_P	22.1107
B3	DIFFI_B3_2N	F1	IO_129_N	17.767
B3	DIFFI_B3_3P	F2	IO_130_P	24.0616
B3	DIFFI_B3_4P/CLK0P_B3	G3	IO_131_P	25.7532
B3	DIFFI_B3_4N/CLK0N_B3	H3	IO_131_N	28.8419
B3	DIFFI_B3_7P	G2	IO_134_P	23.648
B3	DIFFI_B3_7N	H1	IO_134_N	19.6729
B5	DIFFI_B5_2P/PLL0_CLKFB_P	B1	IO_155_P	16.2184
B5	DIFFI_B5_2N/PLL0_CLKFB_N	C1	IO_155_N	15.8411
B5	DIFFI_B5_4P/PLL0_CLKIN_P	E3	IO_157_P	32.5365
B5	DIFFI_B5_4N/PLL0_CLKIN_N	E2	IO_157_N	31.3541
B5	DIFFI_B5_5P	D2	IO_158_P	22.2933
B5	DIFFI_B5_8P/CLK0P_B5	D1	IO_161_P	16.6385
B5	DIFFI_B5_8N/CLK0N_B5	E1	IO_161_N	22.1586
	MIPI_CTRL	A2		19.5062
	VCC	D5		
	VCC	E4		
	VCC	E6		
	VCC	F5		
	VCCIO0	B5		
	VCCIO0	B8		
	VCCIO0	D7		
	VCCIO1	E8		
	VCCIO1	H8		
	VCCIO2	G6		
	VCCIO2	H5		
	VCCIO3	F3		
	VCCIO3	H2		
	VCCIO5	B2		
	VCCIO5	D3		
	VSS	A1		
	VSS	A9		
	VSS	D4		
	VSS	D6		
	VSS	E5		
	VSS	E7		
	VSS	F4		

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
	VSS	F6		
	VSS	J1		
	VSS	J9		

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