PG2L50H_MBG324

(PK04006, V1.1)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.1	30.06.2022	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

PG2L50H_MBG324 uses a Wire-Bond BGA type of packaging. Package size: 15x15mm; Number of balls: 324; Ball pitch: 0.8mm; Maximum package thickness: 1.41mm.

Chapter 2 Package Dimension and Pin Definitions

2.1 Package Dimension

Table 2-1 Dimensional Values

Unit: millimeter

Dimension Symbol	Value			Dimension Symbol	Value		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	1.21	1.31	1.41	e	-	0.8	-
A1	0.30	0.35	0.40	b	0.4	0.45	0.5
A2	0.91	0.96	1.01	aaa	-	0.15	-
c	0.22	0.26	0.30	bbb	-	0.2	-
D	14.9	15.0	15.1	ddd	-	0.2	-
E	14.9	15.0	15.1	eee	-	0.15	-
D1	-	13.6	-	fff	-	0.08	-
E1	-	13.6	-	Ball Diam	-	0.45	-

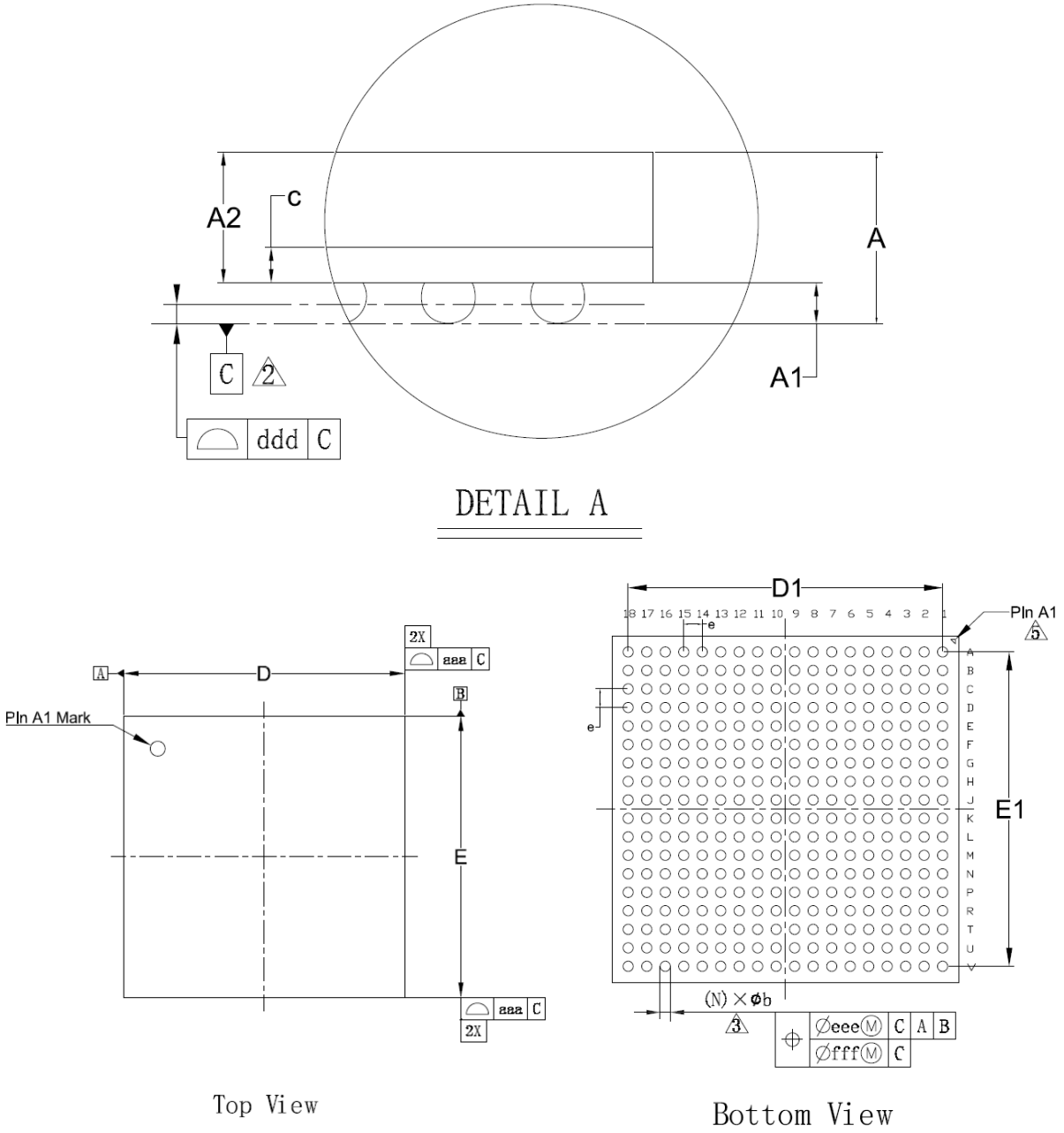

Figure 2-1 Package Outline Dimension (POD)

2.2 Pin Definitions

PG2L50H_ MBG324 has 210 user IOs.

Table 2-2 Product Pin Definitions

PIN Name	PIN Type	PIN Direction	PIN Description
General PIN			
DIFFIO_XX_GY _NN[P,N]	General	Input/Output	General pin； (1) "DIFFIO" indicates the pin supports differential input/output and can be used for transmitting and receiving LVDS signals; (2) " XX " indicates bank numbers, which can be L3, L4, L5, R4, R5； (3) " G " indicates belonging to a memory group； (4) " Y " indicates the group number in a bank, each of which contains four groups； (5) "NN" indicates the sequence number of programmable IO pairs in a bank, increasing from 0, a bank contains 24 difference pairs; (6) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end; During initialization (clear configuration memory), all general pins remain in Tri-state, when IO_STATUS_C=0, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri-state except those need to be used for the multiplexed configuration IOs, when IO_STATUS_C=0, enable internal weak pull-up resistors.
SIO_XX_NN	General	Input/Output	General pin； (1) " SIO " indicates the pin only supports single ended input/output; (2) " XX " indicates bank numbers, which can be L3, L4, L5, R4, R5； (3) "NN" indicates the sequence number of programmable IO in a bank, increasing from 0, a bank contains 2 single ended pins; During initialization (clear configuration memory), all general pins remain in Tri-state, when IO_STATUS_C=0, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri-state except those need to be used for the multiplexed configuration IOs, when IO_STATUS_C=0, enable internal weak pull-up resistors.
Configuration PIN			
INIT_FLAG_N	Dedicated	Bidirectional (open-drain)	Initialization and configuration status dedicated pin: When it is low, it indicates that the FPGA is being initialized (clear configuration memory) or a configuration error has occurred.

PIN Name	PIN Type	PIN Direction	PIN Description
			The pin has an internal weak pull-up resistor that is enabled during configuration; When the FPGA powers up completion, the pin is driven to low level. Once the FPGA completes initialization, the pin is released. During the power up and initialization process, this pin can accept an external low-level input to delay the configuration process. When the FPGA detects high level input on this pin after initialization, the FPGA starts the configuration process.During configuration, this pin serves as an output for the configuration error indication state, low level indicates that an error occurred. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. After the configuration is complete, user can configure weak pull-up or float state for this pin.
CFG_DONE	Dedicated	Bidirectional (open-drain)	Dedicated configuration status pin, built in weak pull-up resistor about 10K. Output as the configuration completion indicator, high level indicates that the configuration is complete. This pin is an open-drain output. When the FPGA powers up completion, the pin is driven to low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released. After the configuration is complete, the pin can be driven externally to low level, Once the internal start-up timing finds that the external DONE pin is low, the internal start-up circuit stops until the external pin is high. After the configuration is complete, user can configure weak pull-up or float state for this pin.
RSTN	Dedicated	Input	Dedicated configuration reset pin, built in weak pull-up resistor and always effective. For restarting configuration logic and configuration memory, active-low. When this pin is low, the FPGA configuration memory is emptied and a new configuration process begins. The configuration logic reset begins with the falling edge of the pin, and the configuration process begins with the rising edge of the pin. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. Keeping this pin low during power up does not put the FPGA configuration logic in a reset state. After the configuration is complete, user can configure weak pull-up or float state for this

PIN Name	PIN Type	PIN Direction	PIN Description
			pin.
CFG_CLK	Dedicated	Input/Output	Configuration clock pin. Except for the JTAG configuration mode, the configuration process of the FPGA is synchronize by this clock in other modes。 In the slave SPI, slave serial and slave parallel configuration modes, the pin serves as a clock input to obtain configuration data from external sources. In the master SPI configuration mode, the pin serves as a clock output to obtain configuration data from external sources and an external pull-up resistor of 1K is required. When the clock is not needed (such as in the JTAG mode), this pin is in the High-Z state. After the configuration is complete, user can configure weak pull-up or float state for this pin.
TCK	Dedicated	Input	Test clock input pin compliant with IEEE STD 1149.1 and provides a clock for the JTAG chain of the FPGA. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TMS	Dedicated	Input	Dedicated JTAG test mode selection input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDI	Dedicated	Input	Dedicated JTAG test data input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDO	Dedicated	Iutput	Dedicated JTAG test data output pin Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
MODE_2	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_1	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_0	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
SCBV	Dedicated	Input	The pin is always effective on BANKCFG, but only on BANK which the multiplexing configuration pins is located during

PIN Name	PIN Type	PIN Direction	PIN Description
			configuration. When the voltage of VCCIOCFG is 2.5V or 3.3V, the pin must be connected to high level and can be connected directly to the VCCIOCFG. When the voltage of VCCIOCFG is 1.8V or lower, the pin must be connected to low level and can be connected directly to the ground. Note: The pin must be used in conjunction with the software, and the SCBV selection in the bitstream setting must be consistent with the hardware setting. For details about the SCBV pin pull-up/pull-down level corresponds to the configured BANK power, see "UG040012_Logos2 Family Hardware Design Guide".
FCS_N	Multiplexed	Output	Multi-function configuration pin, used for the Master SPI configuration mode. (1) In the Master SPI X1, X2 and X4 modes, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
MOSI_D0	Multiplexed	Input/Output	Multi-function configuration data pin. (1) "MOSI", in the master SPI X1 mode; this pin used for serial data output and connects to the data input pin of the external SPI flash (such as DQ0, D, SI, IO0, etc). After the command and address are sent to the external SPI flash, the pin output high-Z or weak pull-up, depending on the state of the IO_STATUS_C pin. (2) In the master SPI X2, X4 and X8 modes, the pin is bidirectional data port, as command and address output to the external SPI flash. Receive the lowest bit data from the external SPI flash. The pin connects to the bidirectional data pin of the external SPI flash (such as DQ0, D, SI, IO0, etc). (3) " D0" , in the slave parallel mode, this pin serves as the D[0] bit of the data bus. (4) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (5) After the configuration is complete, the pin serves as a general pin.
MISO_D1_DI	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X1 mode, " MISO" serves as data input and connects to the data output pin of the external SPI flash (such as DQ1, Q, SO, IO1, etc).

PIN Name	PIN Type	PIN Direction	PIN Description
			(2) In the master SPI X2, X4 and X8 modes, “D1” connects to the second serial data output pin of the external SPI flash (such as DQ1, Q, SO, IO1, etc). (3) In the slave parallel mode, this pin serves as the D[1] bit of the data bus. (4) In the slave serial mode, “D1” serves as data input pin. (5) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. In the other configuration modes(such as JTAG), the state on the pin is ignored (6) After the configuration is complete, the pin serves as a general pin.
D[2，3]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X4 and X8 modes, serve as data input and connects to the data output pin of the external SPI flash. “D2” connects to the third bit data output pin of the external SPI flash (such as DQ2, W#, WP#, IO2, etc). “D3” connects to the fourth bit data output pin of the external SPI flash (such as DQ3, HOLD#, IO3, etc). These pins should be connected to VCCIO via an external weak pull-up resistor of 4.7K. (2) In the slave parallel mode, these pins serve as the D[3:2] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[4，5，6，7]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X8 mode, connect to the second flash in the same way as D[3:0]. (2) In the slave parallel mode, these pins serve as the D[7:4] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[8,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1)In the slave parallel X16 and X32 modes, serve as the D[15:8] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
D[16,…,31]_A[0,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the slave parallel X32 mode, serve as the D[31:16] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these

PIN Name	PIN Type	PIN Direction	PIN Description
			pins serve as general pins.
A[16,…,28]	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (2) After the configuration is complete, these pins serve as general pins.
CS_N	Multiplexed	Input	Multi-function configuration pin. For chip select input. Active low. (1) When it is low level, this pin enables the slave parallel mode configuration interface. In the slave parallel configuration mode, the external controller can select the slave parallel bus of the FPGA by controlling this pin. Or this pin connected to the previous FPGA CSO_DOUT pin in the slave parallel configuration chain. (2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
RWSEL	Multiplexed	Input	Multi-function configuration pin. For selecting the read/write input in the slave parallel configuration mode (high for read and low for write). (1) When it is high level, the slave parallel configuration mode reads data from the data bus. (2) When it is low level, the slave parallel configuration mode writes data to the data bus. (3) Read and write can be switched only when CS_N is high level. (4) After the configuration is complete, the pin serves as a general pin. (5) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state.
CSO_DOUT	Multiplexed	Output(OD）、Output	Multi-function configuration pin. Needed for cascade. (1) In the master SPI X1 mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2) In the slave serial configuration mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (3) In the slave parallel cascade configuration mode, this pin serves as a chip select signal open-drain output, connects to downstream chip CS_N pin and should be connected to VCCIO via an external pull-up resistor of 330Ω. (4) In the other configuration modes or in initialization process, the pin acts as a general

PIN Name	PIN Type	PIN Direction	PIN Description
			pin in a high-Z or weak pull-up state.
VS[0、1]	Multiplexed	Output	Multi-function configuration pin. After the configuration is complete, these pins serve as general pins.
IO_STATUS_C	Multiplexed	Input	Multi-function configuration pin, used for controlling whether the weak pull-up resistors for all general pins are enabled during the configuration process. (1) When it is set to "0", the internal pull-up resistors for all general pins are enabled. (2) When it is set to "1", the internal pull-up resistors for all general pins are disabled. (3)It is recommended that the pin connects to VCCIO via an external weak pull-up resistor. (4)The pin can connect to VCCIO or VSS, either directly or via an external resistor of no more than 1K. (5) This pin must not be left floating before or during configuration.
ECCLKIN	Multiplexed	Input	The external clock input for the Master configuration mode, which is an optional external clock input to the configuration logic. (1) In the master SPI mode, the FPGA can select this clock input as the configuration clock for the configuration logic. This clock can be divided (Depends on the settings in the bitstream) and output from the CFG_CLK pin. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.
BFOE_N	Multiplexed	Output	Multi-function configuration pin. After the configuration is complete, the pin serves as a. general pin.
BFWE_FCS2_N	Multiplexed	Output	Multi-function configuration pin used for the master SPI X8 configuration modes. (1) In the Master SPI X8 mode, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin as a general pin.
BADRVO_N	Multiplexed	Output	Multi-function configuration pin. After the configuration is complete, the pin serves as a. general pin.
Clock PIN			
GMCLK	Multiplexed	Input	Multiplexing global multi-regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL, PPLL, and also drive the multi-regional clock buffer. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end

PIN Name	PIN Type	PIN Direction	PIN Description
			of the differential pair needs to be connected. When these pins serve as single regional clock sources, they are able to drive all the IO clock buffers and regional clock buffers of the BANK.
GSCLK	Multiplexed	Input	Multiplexing global single regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL and PPLL. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. They are able to drive all the IO clock buffers and regional clock buffers of the BANK.
Memory Interface PIN			
DQS	Multiplexed	N/A	DDR DQS PIN, each memory group contains two pins.
Reference PIN			
VREF	Multiplexed	N/A	Input reference voltage pins. When not used as external reference voltage pins, these pins serve as general pins,
Power/ Ground PIN			
VCC	Dedicated	Power	Core logic power, 1.0V. Power supply for core logic
VCC_DRM	Dedicated	Power	DRM power, 1.0V. Dedicated power supply for DRM. If the voltage is the same as VCC, it can be connected to VCC at the board.
VCCA	Dedicated	Power	Analog power, 1.8V. Power supply for internal analog circuit.
VCCIO[L3、L4、L5、R4、R5、CFG]	Dedicated	Power	IO BANK power.
VCCB	Dedicated	Power	Key memory backup battery power supply voltage, 1.0V~1.9V. When the key function is not used, the pin needs to be connected to the VCCA or ground.
VSS	Dedicated	Ground	Ground
ADC PIN			
VCCADC	Dedicated	Power	ADC analog power, 1.8V. Power supply for ADC analog circuit.
VSSADC	Dedicated	Ground	GND relative to VCCADC
VAADC_P	Dedicated	Input	ADC dedicated analog differential input (Positive).
VAADC_N	Dedicated	Input	ADC dedicated analog differential input (Negative).
VREFADC_P	Dedicated	N/A	1.255V ADC reference voltage pin.
VREFADC_N	Dedicated	N/A	ADC reference voltage ground.
VAA[0,..,15]P,VAA[0,..,15]N	Multiplexed	Input	ADC differential analog input signals.
TSDP	Dedicated	N/A	Positive pin of the temperature sensor diode. When not used temperature diode, the pin needs to be connected to the VSS. When temperature sensor diode is to be used, then appropriate

PIN Name	PIN Type	PIN Direction	PIN Description
			external temperature monitoring chip is required.
TSDN	Dedicated	N/A	Negative pin of the temperature sensor diode.

2.2.1 Pin Name List

Table 2-3 Pin Name List

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L3	DIFFIO_L3_G0_05N_VREF	D9		65.9987	L3_G0
L3	DIFFIO_L3_G1_10P_GSCLK	C9	IO_1_P	56.9244	L3_G1
L3	DIFFIO_L3_G1_10N_GSCLK	B9	IO_1_N	56.7721	L3_G1
L3	DIFFIO_L3_G1_11P_GMCLK	B8	IO_2_P	68.2198	L3_G1
L3	DIFFIO_L3_G1_11N_GMCLK	A8	IO_2_N	67.7198	L3_G1
L3	DIFFIO_L3_G2_12P_GMCLK	C11	IO_3_P	73.4012	L3_G2
L3	DIFFIO_L3_G2_12N_GMCLK	C10	IO_3_N	73.8220	L3_G2
L3	DIFFIO_L3_G2_13P_GSCLK	A10	IO_4_P	65.5902	L3_G2
L3	DIFFIO_L3_G2_13N_GSCLK	A9	IO_4_N	66.0033	L3_G2
L3	DIFFIO_L3_G3_18N_VREF	D10		85.8326	L3_G3
L4	SIO_L4_00	G13		32.7999	
L4	DIFFIO_L4_G0_00P_VAA1P	D14	IO_5_P	50.7718	L4_G0
L4	DIFFIO_L4_G0_00N_VAA1N	C14	IO_5_N	50.7108	L4_G0
L4	DIFFIO_L4_G0_01P_VAA2P	B13	IO_6_P	51.4650	L4_G0
L4	DIFFIO_L4_G0_01N_VAA2N	B14	IO_6_N	50.9035	L4_G0
L4	DIFFIO_L4_G0_02P_DQS_VAA3P	C12	IO_7_P	73.5188	L4_G0_DQS
L4	DIFFIO_L4_G0_02N_DQS_VAA3N	B12	IO_7_N	73.6795	L4_G0_DQS
L4	DIFFIO_L4_G0_03P	B11	IO_8_P	62.1108	L4_G0
L4	DIFFIO_L4_G0_03N	A11	IO_8_N	62.4369	L4_G0
L4	DIFFIO_L4_G0_04P_VAA5P	F13	IO_9_P	50.7332	L4_G0
L4	DIFFIO_L4_G0_04N_VAA5N	F14	IO_9_N	51.1819	L4_G0
L4	DIFFIO_L4_G0_05P	D12	IO_10_P	55.2901	L4_G0
L4	DIFFIO_L4_G0_05N_VREF	D13	IO_10_N	54.7226	L4_G0
L4	DIFFIO_L4_G1_06P_VAA7P	B16	IO_11_P	46.4721	L4_G1
L4	DIFFIO_L4_G1_06N_VAA7N	B17	IO_11_N	46.9495	L4_G1
L4	DIFFIO_L4_G1_07P_VAA8P	A15	IO_12_P	59.5230	L4_G1
L4	DIFFIO_L4_G1_07N_VAA8N	A16	IO_12_N	60.0692	L4_G1
L4	DIFFIO_L4_G1_08P_DQS_VAA9P	A13	IO_13_P	73.0844	L4_G1_DQS
L4	DIFFIO_L4_G1_08N_DQS_VAA9N	A14	IO_13_N	73.6562	L4_G1_DQS
L4	DIFFIO_L4_G1_09P_VAA10P	B18	IO_14_P	56.5859	L4_G1
L4	DIFFIO_L4_G1_09N_VAA10N	A18	IO_14_N	57.1242	L4_G1
L4	DIFFIO_L4_G1_10P_GSCLK	E15	IO_15_P	46.2280	L4_G1
L4	DIFFIO_L4_G1_10N_GSCLK	E16	IO_15_N	45.9428	L4_G1
L4	DIFFIO_L4_G1_11P_GMCLK	D15	IO_16_P	48.5744	L4_G1
L4	DIFFIO_L4_G1_11N_GMCLK	C15	IO_16_N	48.6287	L4_G1

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L4	DIFFIO_L4_G2_12P_GMCLK	H16	IO_17_P	35.6121	L4_G2
L4	DIFFIO_L4_G2_12N_GMCLK	G16	IO_17_N	35.9540	L4_G2
L4	DIFFIO_L4_G2_13P_GSCLK	F15	IO_18_P	35.8427	L4_G2
L4	DIFFIO_L4_G2_13N_GSCLK	F16	IO_18_N	36.3030	L4_G2
L4	DIFFIO_L4_G2_14P_DQS	H14	IO_19_P	42.7324	L4_G2_DQS
L4	DIFFIO_L4_G2_14N_DQS_BADRVO_N	G14	IO_19_N	42.7571	L4_G2_DQS
L4	DIFFIO_L4_G2_15P_A28	E17	IO_20_P	46.5911	L4_G2
L4	DIFFIO_L4_G2_15N_A27	D17	IO_20_N	47.1273	L4_G2
L4	DIFFIO_L4_G2_16P_A26	K13	IO_21_P	42.4466	L4_G2
L4	DIFFIO_L4_G2_16N_A25	J13	IO_21_N	41.9908	L4_G2
L4	DIFFIO_L4_G2_17P_A24	H17	IO_22_P	35.5344	L4_G2
L4	DIFFIO_L4_G2_17N_A23	G17	IO_22_N	35.5267	L4_G2
L4	DIFFIO_L4_G3_18P_A22	J14	IO_23_P	44.4456	L4_G3
L4	DIFFIO_L4_G3_18N_VREF_A21	H15	IO_23_N	43.9085	L4_G3
L4	DIFFIO_L4_G3_19P_A20	C16	IO_24_P	64.2496	L4_G3
L4	DIFFIO_L4_G3_19N_A19	C17	IO_24_N	64.5466	L4_G3
L4	DIFFIO_L4_G3_20P_DQS	E18	IO_25_P	54.5052	L4_G3_DQS
L4	DIFFIO_L4_G3_20N_DQS_A18	D18	IO_25_N	55.0550	L4_G3_DQS
L4	DIFFIO_L4_G3_21P_A17	G18	IO_26_P	43.1575	L4_G3
L4	DIFFIO_L4_G3_21N_A16	F18	IO_26_N	43.6984	L4_G3
L4	DIFFIO_L4_G3_22P_BFOE_N	J17	IO_27_P	43.9735	L4_G3
L4	DIFFIO_L4_G3_22N_BFWE_FCS2_N	J18	IO_27_N	44.0770	L4_G3
L4	DIFFIO_L4_G3_23P_VS1	K15	IO_28_P	44.2364	L4_G3
L4	DIFFIO_L4_G3_23N_VS0	J15	IO_28_N	44.5738	L4_G3
L4	SIO_L4_01	K16		20.9616	
L5	SIO_L5_00	R11		46.3796	
L5	DIFFIO_L5_G0_00P_MOSI_D0	K17	IO_29_P	34.8850	L5_G0
L5	DIFFIO_L5_G0_00N_MISO_D1_DI	K18	IO_29_N	35.3414	L5_G0
L5	DIFFIO_L5_G0_01P_D2	L14	IO_30_P	31.4001	L5_G0
L5	DIFFIO_L5_G0_01N_D3	M14	IO_30_N	31.6810	L5_G0
L5	DIFFIO_L5_G0_02P_DQS_IO_STATUS_C	L15	IO_31_P	34.7576	L5_G0_DQS
L5	DIFFIO_L5_G0_02N_DQS_ECCLKIN	L16	IO_31_N	34.2078	L5_G0_DQS
L5	DIFFIO_L5_G0_03P_D4	L18	IO_32_P	25.9521	L5_G0
L5	DIFFIO_L5_G0_03N_D5	M18	IO_32_N	26.3915	L5_G0
L5	DIFFIO_L5_G0_04P_D6	R12	IO_33_P	50.4023	L5_G0
L5	DIFFIO_L5_G0_04N_D7	R13	IO_33_N	50.3686	L5_G0

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L5	DIFFIO_L5_G0_05P_FCS_N	L13	IO_34_P	30.2414	L5_G0
L5	DIFFIO_L5_G0_05N_VREF_D8	M13	IO_34_N	29.8446	L5_G0
L5	DIFFIO_L5_G1_06P_D9	R18	IO_35_P	44.5690	L5_G1
L5	DIFFIO_L5_G1_06N_D10	T18	IO_35_N	44.9567	L5_G1
L5	DIFFIO_L5_G1_07P_D11	N14	IO_36_P	34.0764	L5_G1
L5	DIFFIO_L5_G1_07N_D12	P14	IO_36_N	34.2186	L5_G1
L5	DIFFIO_L5_G1_08P_DQS_N	N17	IO_37_P	36.4160	L5_G1_DQS
L5	DIFFIO_L5_G1_08N_DQS_D13	P18	IO_37_N	36.4057	L5_G1_DQS
L5	DIFFIO_L5_G1_09P_D14	M16	IO_38_P	33.6178	L5_G1
L5	DIFFIO_L5_G1_09N_D15	M17	IO_38_N	33.2350	L5_G1
L5	DIFFIO_L5_G1_10P_GSCLK	N15	IO_39_P	36.2275	L5_G1
L5	DIFFIO_L5_G1_10N_GSCLK	N16	IO_39_N	36.4576	L5_G1
L5	DIFFIO_L5_G1_11P_GMCLK	P17	IO_40_P	33.6614	L5_G1
L5	DIFFIO_L5_G1_11N_GMCLK	R17	IO_40_N	33.4928	L5_G1
L5	DIFFIO_L5_G2_12P_GMCLK	P15	IO_41_P	30.3446	L5_G2
L5	DIFFIO_L5_G2_12N_GMCLK	R15	IO_41_N	30.0718	L5_G2
L5	DIFFIO_L5_G2_13P_GSCLK	T14	IO_42_P	32.8956	L5_G2
L5	DIFFIO_L5_G2_13N_GSCLK	T15	IO_42_N	33.4251	L5_G2
L5	DIFFIO_L5_G2_14P_DQS_RWSEL	R16	IO_43_P	39.0965	L5_G2_DQS
L5	DIFFIO_L5_G2_14N_DQS_CSO_DOUT	T16	IO_43_N	38.9586	L5_G2_DQS
L5	DIFFIO_L5_G2_15P_CS_N	V15	IO_44_P	36.9308	L5_G2
L5	DIFFIO_L5_G2_15N_D31_A15	V16	IO_44_N	36.4907	L5_G2
L5	DIFFIO_L5_G2_16P_D30_A14	U17	IO_45_P	37.4198	L5_G2
L5	DIFFIO_L5_G2_16N_D29_A13	U18	IO_45_N	37.7592	L5_G2
L5	DIFFIO_L5_G2_17P_D28_A12	U16	IO_46_P	35.8602	L5_G2
L5	DIFFIO_L5_G2_17N_D27_A11	V17	IO_46_N	36.0111	L5_G2
L5	DIFFIO_L5_G3_18P_D26_A10	T11	IO_47_P	63.3953	L5_G3
L5	DIFFIO_L5_G3_18N_VREF_D25_A9	U11	IO_47_N	63.2311	L5_G3
L5	DIFFIO_L5_G3_19P_D24_A8	U12	IO_48_P	47.1777	L5_G3
L5	DIFFIO_L5_G3_19N_D23_A7	V12	IO_48_N	46.8742	L5_G3
L5	DIFFIO_L5_G3_20P_DQS	V10	IO_49_P	59.4160	L5_G3_DQS
L5	DIFFIO_L5_G3_20N_DQS_D22_A6	V11	IO_49_N	59.0613	L5_G3_DQS
L5	DIFFIO_L5_G3_21P_D21_A5	U14	IO_50_P	48.4487	L5_G3
L5	DIFFIO_L5_G3_21N_D20_A4	V14	IO_50_N	48.1448	L5_G3
L5	DIFFIO_L5_G3_22P_D19_A3	T13	IO_51_P	48.7398	L5_G3
L5	DIFFIO_L5_G3_22N_D18_A2	U13	IO_51_N	48.1993	L5_G3

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L5	DIFFIO_L5_G3_23P_D17_A1	T9	IO_52_P	48.2792	L5_G3
L5	DIFFIO_L5_G3_23N_D16_A0	T10	IO_52_N	47.8910	L5_G3
L5	SIO_L5_01	R10		32.1741	
R4	SIO_R4_00	F5		16.9112	
R4	DIFFIO_R4_G0_00P_VAA4P	C6	IO_53_P	47.5370	R4_G0
R4	DIFFIO_R4_G0_00N_VAA4N	C5	IO_53_N	46.9979	R4_G0
R4	DIFFIO_R4_G0_01P_VAA6P	B7	IO_54_P	52.0253	R4_G0
R4	DIFFIO_R4_G0_01N_VAA6N	B6	IO_54_N	51.8072	R4_G0
R4	DIFFIO_R4_G0_02P_DQS_VAA11P	A6	IO_55_P	55.6416	R4_G0_DQS
R4	DIFFIO_R4_G0_02N_DQS_VAA11N	A5	IO_55_N	56.1889	R4_G0_DQS
R4	DIFFIO_R4_G0_03P	D8	IO_56_P	56.9045	R4_G0
R4	DIFFIO_R4_G0_03N	C7	IO_56_N	56.7738	R4_G0
R4	DIFFIO_R4_G0_04P_VAA12P	E6	IO_57_P	44.9749	R4_G0
R4	DIFFIO_R4_G0_04N_VAA12N	E5	IO_57_N	44.7101	R4_G0
R4	DIFFIO_R4_G0_05P	E7	IO_58_P	49.5687	R4_G0
R4	DIFFIO_R4_G0_05N_VREF	D7	IO_58_N	50.0759	R4_G0
R4	DIFFIO_R4_G1_06P_VAA13P	C4	IO_59_P	51.7550	R4_G1
R4	DIFFIO_R4_G1_06N_VAA13N	B4	IO_59_N	51.4750	R4_G1
R4	DIFFIO_R4_G1_07P_VAA14P	A4	IO_60_P	57.7595	R4_G1
R4	DIFFIO_R4_G1_07N_VAA14N	A3	IO_60_N	57.4702	R4_G1
R4	DIFFIO_R4_G1_08P_DQS_VAA15P	B1	IO_61_P	57.0068	R4_G1_DQS
R4	DIFFIO_R4_G1_08N_DQS_VAA15N	A1	IO_61_N	56.9323	R4_G1_DQS
R4	DIFFIO_R4_G1_09P_VAA0P	B3	IO_62_P	46.3876	R4_G1
R4	DIFFIO_R4_G1_09N_VAA0N	B2	IO_62_N	46.5543	R4_G1
R4	DIFFIO_R4_G1_10P_GSCLK	D5	IO_63_P	66.9603	R4_G1
R4	DIFFIO_R4_G1_10N_GSCLK	D4	IO_63_N	66.6335	R4_G1
R4	DIFFIO_R4_G1_11P_GMCLK	E3	IO_64_P	45.8678	R4_G1
R4	DIFFIO_R4_G1_11N_GMCLK	D3	IO_64_N	45.8207	R4_G1
R4	DIFFIO_R4_G2_12P_GMCLK	F4	IO_65_P	47.5353	R4_G2
R4	DIFFIO_R4_G2_12N_GMCLK	F3	IO_65_N	47.0398	R4_G2
R4	DIFFIO_R4_G2_13P_GSCLK	E2	IO_66_P	46.4400	R4_G2
R4	DIFFIO_R4_G2_13N_GSCLK	D2	IO_66_N	46.7300	R4_G2
R4	DIFFIO_R4_G2_14P_DQS	H2	IO_67_P	40.4448	R4_G2_DQS
R4	DIFFIO_R4_G2_14N_DQS	G2	IO_67_N	39.9136	R4_G2_DQS
R4	DIFFIO_R4_G2_15P	C2	IO_68_P	57.5672	R4_G2
R4	DIFFIO_R4_G2_15N	C1	IO_68_N	57.9575	R4_G2

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R4	DIFFIO_R4_G2_16P	H1	IO_69_P	43.7214	R4_G2
R4	DIFFIO_R4_G2_16N	G1	IO_69_N	44.2548	R4_G2
R4	DIFFIO_R4_G2_17P	F1	IO_70_P	51.2452	R4_G2
R4	DIFFIO_R4_G2_17N	E1	IO_70_N	51.0769	R4_G2
R4	DIFFIO_R4_G3_18P	G6	IO_71_P	51.8211	R4_G3
R4	DIFFIO_R4_G3_18N_VREF	F6	IO_71_N	51.4772	R4_G3
R4	DIFFIO_R4_G3_19P	G4	IO_72_P	35.0265	R4_G3
R4	DIFFIO_R4_G3_19N	G3	IO_72_N	35.4794	R4_G3
R4	DIFFIO_R4_G3_20P_DQS	J4	IO_73_P	46.6967	R4_G3_DQS
R4	DIFFIO_R4_G3_20N_DQS	H4	IO_73_N	46.3049	R4_G3_DQS
R4	DIFFIO_R4_G3_21P	J3	IO_74_P	30.0269	R4_G3
R4	DIFFIO_R4_G3_21N	J2	IO_74_N	30.0035	R4_G3
R4	DIFFIO_R4_G3_22P	K2	IO_75_P	39.1040	R4_G3
R4	DIFFIO_R4_G3_22N	K1	IO_75_N	38.5161	R4_G3
R4	DIFFIO_R4_G3_23P	H6	IO_76_P	40.7885	R4_G3
R4	DIFFIO_R4_G3_23N	H5	IO_76_N	40.2846	R4_G3
R4	SIO_R4_01	J5		28.6774	
R5	SIO_R5_00	K6		31.3328	
R5	DIFFIO_R5_G0_00P	L1	IO_77_P	31.9806	R5_G0
R5	DIFFIO_R5_G0_00N	M1	IO_77_N	31.9956	R5_G0
R5	DIFFIO_R5_G0_01P	K3	IO_78_P	34.2440	R5_G0
R5	DIFFIO_R5_G0_01N	L3	IO_78_N	34.3755	R5_G0
R5	DIFFIO_R5_G0_02P_DQS	N2	IO_79_P	38.4447	R5_G0_DQS
R5	DIFFIO_R5_G0_02N_DQS	N1	IO_79_N	37.8614	R5_G0_DQS
R5	DIFFIO_R5_G0_03P	M3	IO_80_P	30.4389	R5_G0
R5	DIFFIO_R5_G0_03N	M2	IO_80_N	30.8214	R5_G0
R5	DIFFIO_R5_G0_04P	K5	IO_81_P	42.7881	R5_G0
R5	DIFFIO_R5_G0_04N	L4	IO_81_N	42.8939	R5_G0
R5	DIFFIO_R5_G0_05P	L6	IO_82_P	32.5996	R5_G0
R5	DIFFIO_R5_G0_05N_VREF	L5	IO_82_N	32.9033	R5_G0
R5	DIFFIO_R5_G1_06P	U1	IO_83_P	53.9521	R5_G1
R5	DIFFIO_R5_G1_06N	V1	IO_83_N	53.7570	R5_G1
R5	DIFFIO_R5_G1_07P	U4	IO_84_P	64.9694	R5_G1
R5	DIFFIO_R5_G1_07N	U3	IO_84_N	64.3928	R5_G1
R5	DIFFIO_R5_G1_08P_DQS	U2	IO_85_P	51.1804	R5_G1_DQS
R5	DIFFIO_R5_G1_08N_DQS	V2	IO_85_N	50.6320	R5_G1_DQS

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R5	DIFFIO_R5_G1_09P	V5	IO_86_P	56.4018	R5_G1
R5	DIFFIO_R5_G1_09N	V4	IO_86_N	55.9497	R5_G1
R5	DIFFIO_R5_G1_10P_GSCLK	R3	IO_87_P	42.1272	R5_G1
R5	DIFFIO_R5_G1_10N_GSCLK	T3	IO_87_N	42.2501	R5_G1
R5	DIFFIO_R5_G1_11P_GMCLK	T5	IO_88_P	42.5596	R5_G1
R5	DIFFIO_R5_G1_11N_GMCLK	T4	IO_88_N	43.0457	R5_G1
R5	DIFFIO_R5_G2_12P_GMCLK	N5	IO_89_P	38.1234	R5_G2
R5	DIFFIO_R5_G2_12N_GMCLK	P5	IO_89_N	37.7499	R5_G2
R5	DIFFIO_R5_G2_13P_GSCLK	P4	IO_90_P	24.6844	R5_G2
R5	DIFFIO_R5_G2_13N_GSCLK	P3	IO_90_N	24.2210	R5_G2
R5	DIFFIO_R5_G2_14P_DQS	P2	IO_91_P	26.8134	R5_G2_DQS
R5	DIFFIO_R5_G2_14N_DQS	R2	IO_91_N	26.7699	R5_G2_DQS
R5	DIFFIO_R5_G2_15P	M4	IO_92_P	27.5815	R5_G2
R5	DIFFIO_R5_G2_15N	N4	IO_92_N	27.9000	R5_G2
R5	DIFFIO_R5_G2_16P	R1	IO_93_P	28.9638	R5_G2
R5	DIFFIO_R5_G2_16N	T1	IO_93_N	28.7234	R5_G2
R5	DIFFIO_R5_G2_17P	M6	IO_94_P	37.5574	R5_G2
R5	DIFFIO_R5_G2_17N	N6	IO_94_N	37.6571	R5_G2
R5	DIFFIO_R5_G3_18P	R6	IO_95_P	51.6924	R5_G3
R5	DIFFIO_R5_G3_18N_VREF	R5	IO_95_N	51.2293	R5_G3
R5	DIFFIO_R5_G3_19P	V7	IO_96_P	55.3256	R5_G3
R5	DIFFIO_R5_G3_19N	V6	IO_96_N	55.1986	R5_G3
R5	DIFFIO_R5_G3_20P_DQS	U9	IO_97_P	63.1291	R5_G3_DQS
R5	DIFFIO_R5_G3_20N_DQS	V9	IO_97_N	62.8387	R5_G3_DQS
R5	DIFFIO_R5_G3_21P	U7	IO_98_P	51.5790	R5_G3
R5	DIFFIO_R5_G3_21N	U6	IO_98_N	51.1918	R5_G3
R5	DIFFIO_R5_G3_22P	R7	IO_99_P	48.6439	R5_G3
R5	DIFFIO_R5_G3_22N	T6	IO_99_N	48.2486	R5_G3
R5	DIFFIO_R5_G3_23P	R8	IO_100_P	49.9707	R5_G3
R5	DIFFIO_R5_G3_23N	T8	IO_100_N	50.4491	R5_G3
R5	SIO_R5_01	U8		24.5684	
	CFG_CLK	E9		9.8778	
	CFG_DONE	P10		10.6829	
	INIT_FLAG_N	P7		21.4249	
	MODE_0	P12		13.5635	
	MODE_1	P13		20.4505	
	MODE_2	P11		12.3471	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	RSTN	P9		12.9090	
	SCBV	P8		21.2166	
	TCK	E10		16.3386	
	TDI	E11		11.0039	
	TDO	E13		25.4248	
	TMS	E12		12.6247	
	TSDN	L9	IO_101_N	51.2899	
	TSDP	L10	IO_101_P	50.8256	
	VAADC_N	K9	IO_102_N	39.1204	
	VAADC_P	J10	IO_102_P	37.7971	
	VREFADC_N	J9	IO_103_N	45.0451	
	VREFADC_P	K10	IO_103_P	45.3006	
	VCCIOR4	A7			
	VCCIOL4	A17			
	VCCIOL3	B10			
	VCCIOR4	C3			
	VCCIOL4	C13			
	VCCIOR4	D6			
	VCCIOL4	D16			
	VCCB	E8			
	VCCIOR4	F2			
	VCC	F8			
	VCC_DRM	F10			
	VCCA	F12			
	VCCIOR4	G5			
	VCC	G7			
	VCC	G9			
	VCC_DRM	G11			
	VCCIOL4	G15			
	VCC	H8			
	VCCADC	H10			
	VCCA	H12			
	VCCIOL4	H18			
	VCCIOR4	J1			
	VCC	J7			
	VCC	J11			
	VCCIOR5	K4			
	VCC	K8			
	VCCA	K12			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCCIOL4	K14			
	VCC	L7			
	VCC	L11			
	VCCIOL5	L17			
	VCC	M8			
	VCC	M10			
	VCCA	M12			
	VCCIOR5	N3			
	VCC	N7			
	VCC	N9			
	VCC	N11			
	VCCIOL5	N13			
	VCCIOR5	P6			
	VCCIOL5	P16			
	VCCIOCFG	R9			
	VCCIOR5	T2			
	VCCIOL5	T12			
	VCCIOR5	U5			
	VCCIOL5	U15			
	VCCIOR5	V8			
	VCCIOL5	V18			
	VSS	A2			
	VSS	A12			
	VSS	B5			
	VSS	B15			
	VSS	C8			
	VSS	C18			
	VSS	D1			
	VSS	D11			
	VSS	E4			
	VSS	E14			
	VSS	F7			
	VSS	F9			
	VSS	F11			
	VSS	F17			
	VSS	G8			
	VSS	G10			
	VSS	G12			
	VSS	H3			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	H7			
	VSSADC	H9			
	VSS	H11			
	VSS	H13			
	VSS	J6			
	VSS	J8			
	VSS	J12			
	VSS	J16			
	VSS	K7			
	VSS	K11			
	VSS	L2			
	VSS	L8			
	VSS	L12			
	VSS	M5			
	VSS	M7			
	VSS	M9			
	VSS	M11			
	VSS	M15			
	VSS	N8			
	VSS	N10			
	VSS	N12			
	VSS	N18			
	VSS	P1			
	VSS	R4			
	VSS	R14			
	VSS	T7			
	VSS	T17			
	VSS	U10			
	VSS	V3			
	VSS	V13			

Chapter 3 Thermal Resistance

Table 3-1 Thermal Resistance

θ_{JA}(℃/W) (Flow: 0m/s)	**θ_{JB}(℃/W)**	**θ_{JC}(℃/W)**	**θ_{JA}(℃/W) (Flow: 1m/s)**	**θ_{JA}(℃/W) (Flow: 2m/s)**
19.1	6.7	4.8	16.1	14.4

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