PK02002_PGL22G_MBG324

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.6	30.06.2020	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing

Table of Contents

Tables

Figures

Chapter 1 Introduction to Packaging

PGL22G_MBG324 uses a wire- bond Ball Grid Array (BGA) type of packaging. Its package size is 15mmx15mm, with 324 solder balls, a pitch of 0.8mm and a maximum package thickness of 1.36mm.

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Values

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
D	14.9	15.0	15.1	A	1.16	1.26	1.36
D1	n/a	13.6	n/a	A1	0.25	0.30	0.35
E	14.9	15.0	15.1	A2	0.91	0.96	1.01
E1	n/a	13.6	n/a	c	0.22	0.26	0.3
b	0.35	0.4	0.45	e	n/a	0.8	n/a
DDD (Die-to-Die Alignment)	0.2						

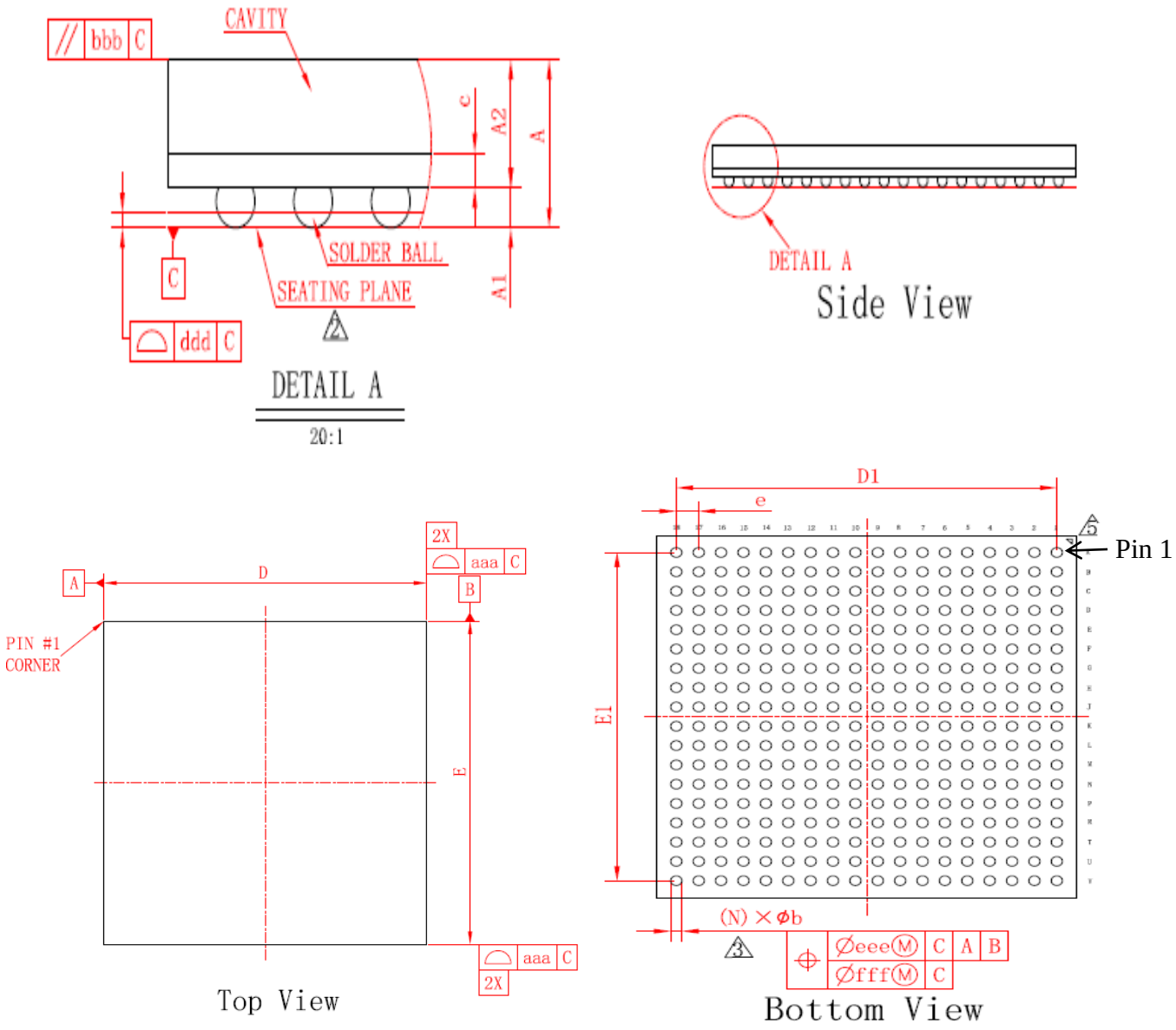

Figure 2-1 Package Outline Dimension (POD)

Note: PIN #1 indicates the position of the first pin

2.2 Pin Description

Table 2-2 Product Pin Definitions

PIN name	PIN type	PIN description
General PIN		
DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]	input/output	All general IOs are marked as DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]. DIFFIO: indicates that all general IOs support differential input/output, such as LVDS; [L0, L1, L2, R0, R1, R2]: indicates BANK names [0…n]: indicates the unique differential pair number in the BANK; [N, P]: N indicates the negative end of the

PIN name	PIN type	PIN description
		differential pair and P represents the positive end.
Multiplexed Pin		
DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]/XXX		Multiplexed pins are marked as DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]/XXX, where XXX indicates one or more of the functions described below. When the multiplexed pin is not used for special applications, it can serve as a general IO
--Configuration Pin		
MODE_2, MODE_1, MODE_0	input	They are used for configuration mode selection during configuration, as follows: 000: JTAG 001: Master SPI (X1, X2, X4, X8) 010: Master BPI (X8, X16) 011: Slave Serial (X1) 100: Slave Parallel (X8, X16, X32) 101: Slave SPI (X1) 111: Internal Master SPI (X1, X2, X4)
INIT_FLAG_N	Bidirectional (open-drain)	When the FPGA powers up completion during configuration, the pin is driven to a low level. Once the FPGA completes initialization, the pin is released. During configuration, this pin serves as an output for the configuration error indication state. During the configuration or initialization process, this pin can also accept an external low-level input to indicate an error or delay the configuration.
CFG_CLK	input/output	Configuration Clock Pin. In the slave mode, the pin serves as a clock input to obtain configuration data from external sources; In the master mode, the pin serves as a clock output to obtain configuration data from external sources;
D[31, 30…1, 0]	input/output	32-bit configuration data bus input/output pins: (1) In the Master SPI X1 configuration mode, pin D[0], as command output, is connected to the data input of the SPI flash, and pin D[1], as data input, is connected to the data output of the SPI flash. (2) In the Master SPI X2 configuration mode, pins D[1:0] serve as the data bus. (3) In the Master SPI X4 configuration mode, pins D[3:0] serve as the data bus. (4) In the Master SPI X8 configuration mode, pins D[3:0] serve as the data bus for the first SPI FLASH, and pins D[7:4] serve as the data bus for the second SPI FLASH. (5) In the Slave Serial configuration mode, pin D[1] serves as the data bus.

PIN name	PIN type	PIN description
		(6) In the Slave SPI configuration mode, pin D[0] is for the master device output and slave device input, pin D[1] is for the master device input and slave device output, and pin D[3] is for chip hold. (7) In the Master BPI configuration X8 asynchronous mode, pins D[7:0] serve as an 8-bit data bus. (8) In the Master BPI configuration X16 asynchronous/synchronous mode, pins D[15:0] serve as a 16-bit data bus. (9) In the Slave Parallel X8 configuration mode, pins D[7:0] are an 8-bit data bus. (10) In the Slave Parallel X16 configuration mode, pins D[15:0] are a 16-bit data bus. (11) In the Slave Parallel X32 configuration mode, pins D[31:0] are a 32-bit data bus.
CS_N	input	Multi-function Configuration Pin. for chip select input. Active low. (1) When it is low level, this pin enables the Slave Parallel mode configuration interface. (2) In other configuration modes, this pin is high-z. (3) To make this pin continue playing its configuration function after configuration is complete, users need to set the configuration register to preserve its configuration function.
RWSEL	input	Multi-function Configuration Pin. For selecting the read/write input in the Slave Parallel configuration mode (high for read and low for write). (1) When it is high level, the Slave Parallel configuration mode reads data from the data bus; (2) When it is low level, the Slave Parallel configuration mode writes data to the data bus; (3) Read and write can be switched only when CS_N is high level. (4) To make this pin continue playing its configuration function after configuration is complete, users need to set the configuration register to preserve its configuration function. (5) In other configuration modes, this pin is high-z.
BUSY	output	Multi-function Configuration Pin. (1) During readback in the Slave Parallel mode, a high level output indicates that the data read from the bus is invalid. (2)To make this pin continue playing its configuration function in the user mode, users need to set the configuration register to preserve its configuration function. (3) In other configuration modes, this pin is in the high-z state.

PIN name	PIN type	PIN description
CSO_DOUT	output	Multi-function Configuration Pin. Needed for cascade. (1) In the Master SPI X1 mode, this pin serves as cascaded data output; (2) In the Slave Serial configuration mode, this pin serves as cascaded data output; (3) In the Slave Parallel configuration mode, this pin serves as a chip select signal output;
FCS_N	output	Multi-function configuration pin, used for the external Master SPI configuration mode. (1) In the Master SPI mode, this pin outputs a chip select signal to external flash, active-low;
VS1, VS0	input	Multi-function configuration pins, used in the Master SPI or internal Master SPI mode. (1) It is used for selecting the bitstream version: 00 for the first set of bitstreams, 01 for the second set, 10 for the third set, 11 for the fourth set; (2) Enable the internal pull-down resistors during configuration.
IO_STATUS_C	input	Multi-function pin, used for inputting signals and controlling the state of all general IOs during the configuration process. (1) "1" keeps all general IOs in a pull-up state during configuration. (2) "0" keeps all general IOs in a tri-state during configuration.
ADR[25:0]	output	Multi-function configuration pins, used for outputting addresses in the BPI configuration mode.
BFOE_N	output	Multi-function configuration pin, used for providing a low-level output enable control signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, this pin should be connected to the flash's output enable input and to VCCIO via a 4.7K resistor.
BADRVO_N	output	Multi-function configuration pin, used for providing a low-level address valid control signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, if the external FLASH supports address valid signal input, then this pin should be connected to the FLASH's address valid input pin and to VCCIO via a 4.7K resistor. If the external flash does not support address valid signal input, then there is no need to connect this pin.
BFWE_N	output	Multi-function configuration pin, used for providing a low-level write enable signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, this pin should be connected to the flash's write enable input and to VCCIO via a 4.7K resistor;
BFCE_N	output	Multi-function configuration pin, used for providing a low-level chip select control signal for parallel NOR FLASH in the BPI configuration

PIN name	PIN type	PIN description
		mode; (1) In the BPI configuration mode, this pin should be connected to the flash's chip select input and to VCCIO via a 4.7K resistor.
FCS2_N	output	Multi-function configuration pin, used for the external Master SPI X8 configuration mode. (1) In the Master SPI X8 mode, this pin outputs a chip select signal to the external flash, active-low. The pin should be connected to VCCIO via an external pull-up resistor not more than 4.7K.
ECCLKIN	input	Multi-function configuration pin, used for inputting signals and serves as clock input for the internal Master configuration mode.
-- Clock, PLL, Crystal Oscillator Multi-function Pin		
CLK[0,1,2,3]_[L0,L1,L2,R0,R1,R2]	input	Dedicated global clock input pins, 4 pins for each bank
DIFFCLK[0,1]_[L0,L1,L2,R0,R1,R2]_[N,P]	input	Dedicated global differential clock input pins, 2 pairs for each bank
PLL[0,1,2,…10]_CLKOUT_[P,N]	output	Direct selection of PLL[0, 1, …, 19] output to these pins are possible
PLL[0,1,2,…10]_CLKIN[0,1,2,3]	input	Optional PLL input, PLL can select directly the input clock from these pins
PLL[0,1,2,…10]_CLKFB_[P,N]	input	Optional PLL feedback clock input, PLL can input external feedback clock from these pins
XTALA_[L0,L1,L2,R0,R1,R2]	input	Dedicated external crystal input at port A. Input for the on-die inverter, 1 pin for each bank
XTALB_[L0,L1,L2,R0,R1,R2]	output	Dedicated external crystal output at port B. Output for the on-die inverter, 1 pin for each bank
-- External Memory Interface Pin		
DQS[0,1,2][#]_[L0,L1,L2,R0,R1,R2]	input/output	Used to connect to the DQS/DQS# signal pins of external memory
DQ[0,1,2]_[L0,L1,L2,R0,R1,R2]	input/output	Can connect to the DQ signal pins of external memory
--HMEMC Memory Interface Pin		
[R,L]_A[0,..,15]	output	DDR memory address
[R,L]_CS_N	output	DDR memory chip selection signal, active-low, depends on whether the memory is in use.
[R,L]_RAS_N	output	RAS, active-low
[R,L]_CAS_N	output	CAS, active-low
[R,L]_WE_N	output	Write enable, active-low
[R,L]_BA[0,1,2]	output	DDR BANK address
[R,L]_ODT	output	ODT, on-die terminal
[R,L]_CK_P	output	Clock P side of DDR memory
[R,L]_CK_N	output	Clock N side of DDR memory
[R,L]_CKE	output	DDR memory clock enable signal, active-high
[R,L]_RESET_N	output	DDR memory reset, active-low
[R,L]_DML	output	Write data mask signals of DQ0-DQ7
[R,L]_DQSL	input/output	DQS signals related to DQ0-DQ7
[R,L]_DQSL_N		DQS# signals related to DQ0-DQ7

PIN name	PIN type	PIN description
	input/output	
[R,L]_DQ[0,…,15]	input/output	Memory data bus
[R,L]_DMU	output	Write data mask signals of DQ8-DQ15
[R,L]_DQSU	input/output	DQS signals related to DQ8-DQ15
[R,L]_DQSU_N	input/output	DQS# signals related to DQ8-DQ15
[R,L]_DQSL_GATE_IN	input	DQS gate window signal feedback (low bit) after compensating for read command path delay
[R,L]_DQSL_GATE_OUT	output	DQS gate window signal output (low bit) after compensating for read command path delay
[R,L]_DQSU_GATE_IN	input	DQS gate window signal feedback (high bit) after compensating for read command path delay
[R,L]_DQSU_GATE_OUT	output	DQS gate window signal output (high bit) after compensating for read command path delay
--Reference Pin		
RRP_[L0,L1,L2,R0,R1,R2]	input	External reference resistor pins, one for each bank. Provides a reference resistor to the power supply for on-die terminal resistor adjustment.
RRN_[L0,L1,L2,R0,R1,R2]	input	External reference resistor pins, one for each bank. Provides a reference resistor to the ground for on-die terminal resistor adjustment.
VREF_[L0,L1,L2,R0,R1,R2]	input	External reference voltage pins, one for each bank. Provides reference voltage input for each BANK
--ADC Pin		
VAUX[9,8,7,..0]	input	Input analog signals
Dedicated Pin		
--Configuration Pin, JTAG Pin		
CFG_DONE	Bidirectional (open-drain)	Dedicated pin for configuration state. Serves as a status output, this pin is driven to low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.
RST_N	input	Dedicated configuration input pin, internally weak pull-up, for restarting the configuration process, active-low. It is recommended that users externally pull up the RST_N with a resistor when using this pin. When this pin is low level, the FPGA enters a reset state, and all IOs are in the high-z state.
TCK	input	Dedicated JTAG test clock input pin
TMS	input	Dedicated JTAG test mode selection input pin
TDI	input	Dedicated JTAG test data input pin.
TDO	output	Dedicated JTAG test data output pin.
--Reference Pin		
REXT	input	Dedicated external high-precision resistor pin, with a resistance of 10k and an accuracy of 1%. Provides resistance for the bandgap.
--ADC Pin		

PIN name	PIN type	PIN description
VA[1,0]	input	Dedicated analog input signals
VREF_EXT	input	Dedicated external reference 2.5V voltage.
Power Pin, Ground Pin		
VCC	POWER	Core power, 1.1V. Power supply for core logic
VCCAUX	POWER	3.3V auxiliary power supply for IOB, LDO, and other modules
VCCIO[L0,L1,L2,R0,R1,R2]	POWER	IO BANK power, the banks on the left are BANKL0, BANKL1, BANKL2, and so on from top to down; the banks on the right side are BANKR0, BANKR1, BANKR2, and so on from top to down
VCCAUX_A	POWER	Power supply for ADC, BANDGAP, and POR
VSS	GROUND	GND relative to VCC&VCCAUX
VSSA	GROUND	GND relative to VCCAUX_A
VCCEFUSE	POWER	Efuse programming voltage
VCCIOCFG	POWER	BANKCFG power supply

Note: PGL22G_MBG324 has 240 user IOs.

2.2.1 Pinout Diagram

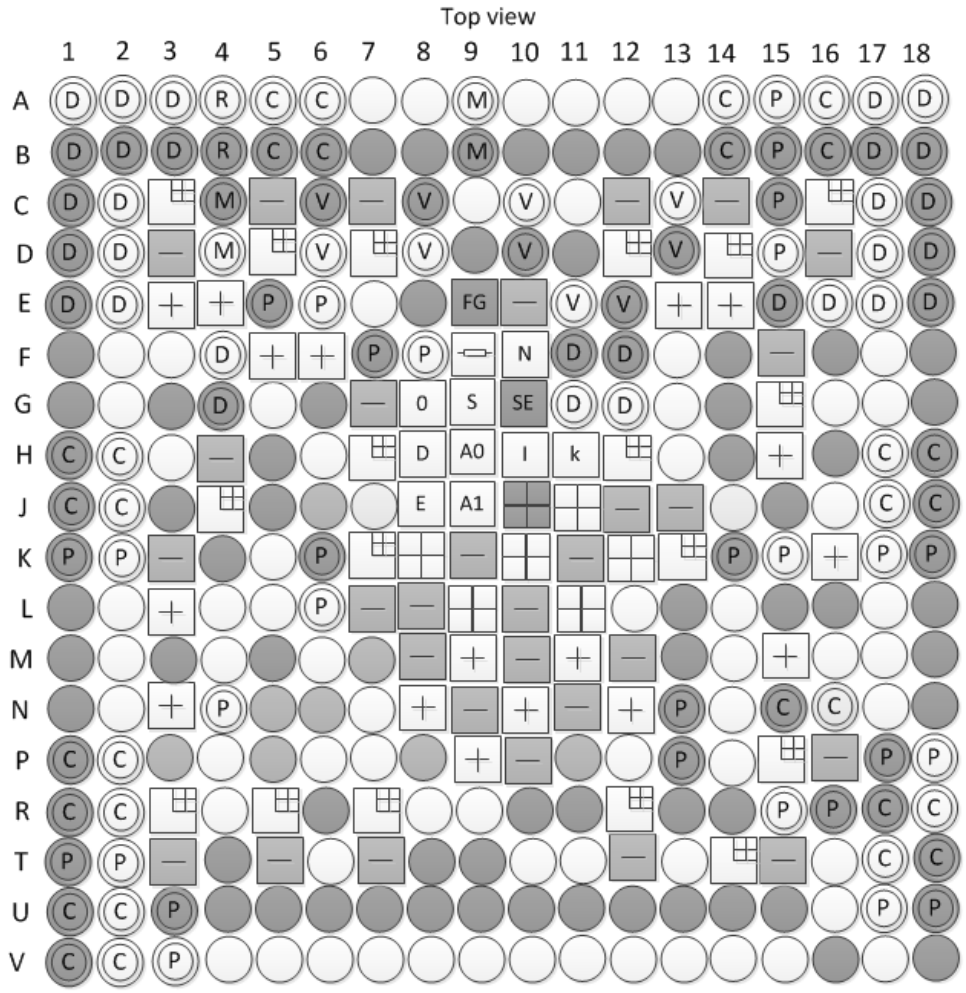

Figure 2-2 Pinout Diagram

Note: The Pinout symbols have the following meanings:

General IO	DIFFIO*	COMP(N) TRUE(P)	Dedicated IO		Other IO	
			REST_N	N	VSS	—
Multiplex IO	DIFFIO*/D0~D31	D D	CFG_DONE	D	VCC	+
	DIFFIO*/MODE*	M M	VREF_EXT	E	VCCAUX	
	DIFFIO*/BUSY	B B	VA1	A1	VDDIO*	
	DIFFIO*/CS_N	C C	VA0	A0	VSSA	A
	DIFFIO*/FCS_N	FC FC	REXT		VDDEFUSE	SE
	DIFFIO*/VREF	V V	TMS	S	VCCAUX_A	
	DIFFIO*/CLK*	C C	TCK	K	VDDIOCFG	FG
	DIFFIO*/PLL*	P P	TDI	I		
	DIFFIO*/RR*	R R	TDO	O		

2.2.2 IO Banks

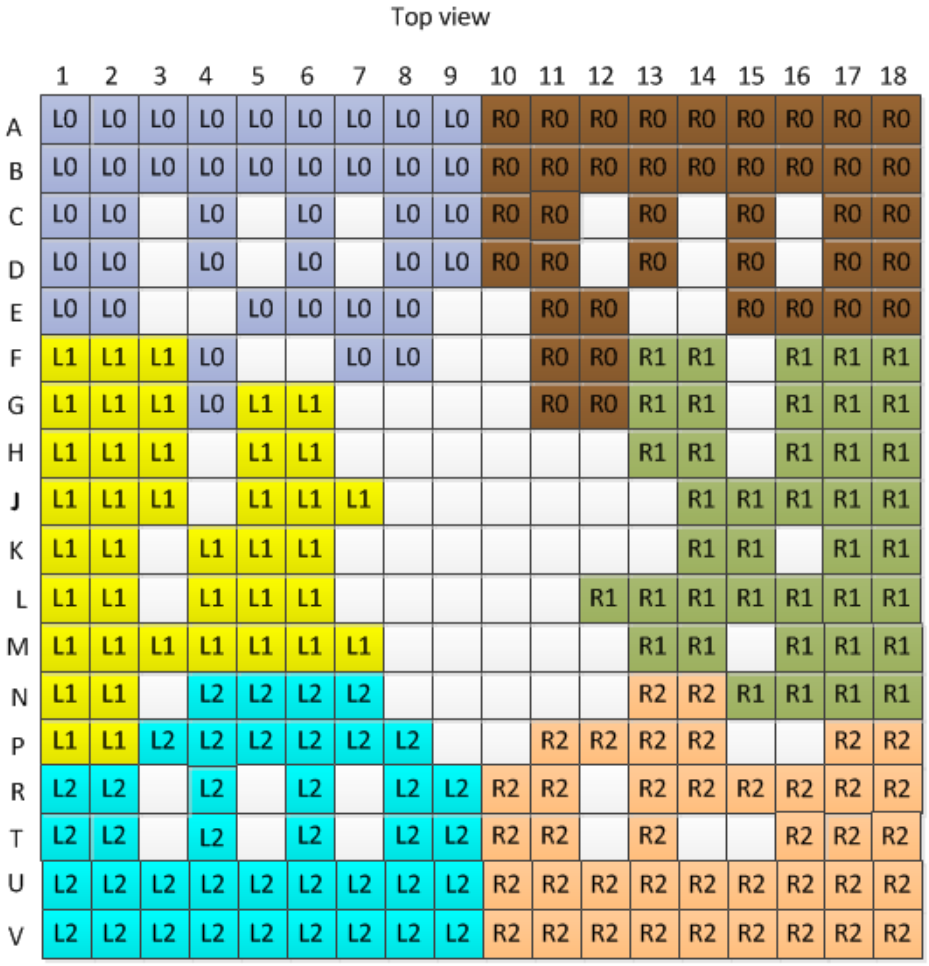

Figure 2-3 IO Banks

2.2.3 Memory Grouping

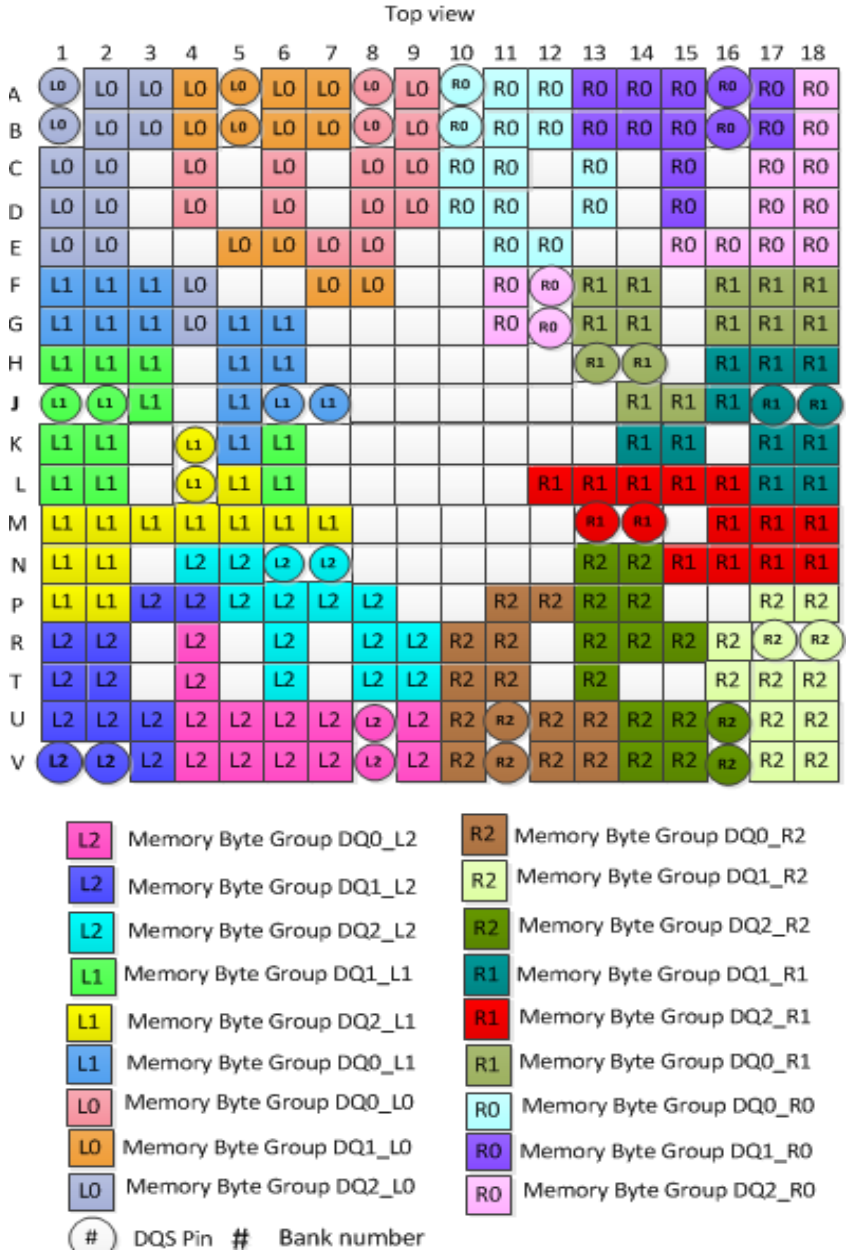

Figure 2-4 Memory Grouping

2.2.4 Power and GND Placement

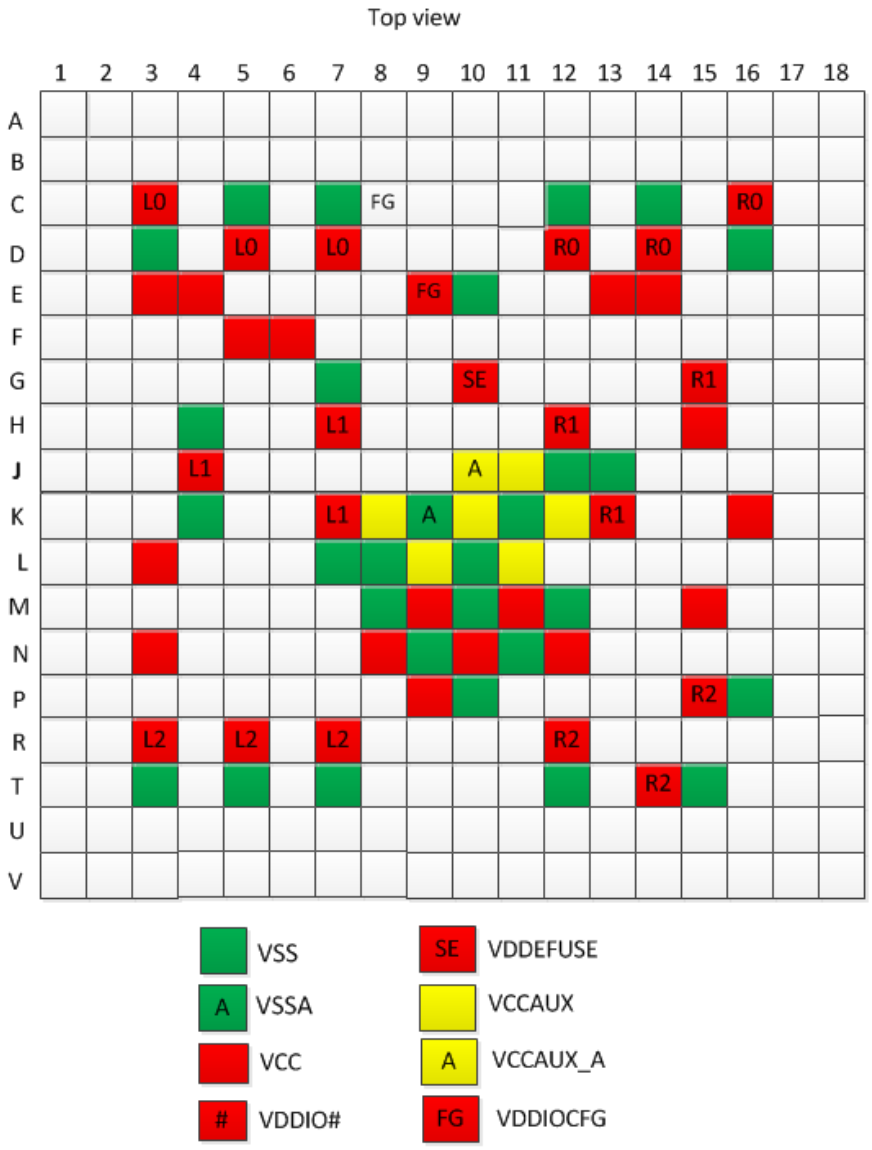

Figure 2-5 Power and GND Placement

2.2.5 Ball Name List

Table 2-1 Ball Name List

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK CFG	RST_N	F10			
BANK CFG	CFG_DONE	H8			
BANK CFG	TCK	H11			
BANK CFG	TMS	G9			

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK CFG	TDI	H10			
BANK CFG	TDO	G8			
BANK CFG	VREF_EXT	J8			
BANK CFG	VA0	H9			
BANK CFG	VA1	J9			
BANK CFG	REXT	F9			
BANK L0	DIFFIO_L0_0_P/BUSY	E8	DQ0_L0		49.55
BANK L0	DIFFIO_L0_0_N	E7	DQ0_L0		51.57
BANK L0	DIFFIO_L0_1_P/VAUX9	C8	DQ0_L0		87.22
BANK L0	DIFFIO_L0_1_N/VAUX8	D8	DQ0_L0		88.99
BANK L0	DIFFIO_L0_2_P/VAUX7	C6	DQ0_L0		49.46
BANK L0	DIFFIO_L0_2_N/VAUX6	D6	DQ0_L0		49.16
BANK L0	DIFFIO_L0_3_P/IO_STATUS_C	D9	DQ0_L0		101.29
BANK L0	DIFFIO_L0_3_N/CFG_CLK	C9	DQ0_L0		98.05
BANK L0	DIFFIO_L0_4_P/FCS_N	B8	DQS0_L0		90.75
BANK L0	DIFFIO_L0_4_N/CS_N	A8	DQS0#_L0		92.98
BANK L0	DIFFIO_L0_5_P/MODE_0	B9	DQ0_L0		95.14
BANK L0	DIFFIO_L0_5_N/MODE_1	A9	DQ0_L0		100.41
BANK L0	DIFFIO_L0_6_P/MODE_2	C4	DQ0_L0		46.71
BANK L0	DIFFIO_L0_6_N/VREF_L0/CSO_DOUT	D4	DQ0_L0		46.98
BANK L0	DIFFIO_L0_7_P/RWSEL	B7	DQ1_L0		95.25
BANK L0	DIFFIO_L0_7_N/INIT_FLAG_N	A7	DQ1_L0		88.91
BANK L0	DIFFIO_L0_8_P/PLL0_CLKOUT_P	E5	DQ1_L0		36.79
BANK L0	DIFFIO_L0_8_N/PLL0_CLKOUT_N	E6	DQ1_L0		37.03
BANK L0	DIFFIO_L0_9_P/CLK0_L0/DIFFCLK0_L0_P/PLL0_CLKFB_P/XTALA_L0	B6	DQ1_L0		97.47
BANK L0	DIFFIO_L0_9_N/CLK1_L0/DIFFCLK0_L0_N/PLL0_CLKFB_N/XTALB_L0	A6	DQ1_L0		103.79
BANK L0	DIFFIO_L0_10_P/CLK2_L0/DIFFCLK1_L0_P/PLL1_CLKIN0	B5	DQS1_L0		93.83

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK L0	DIFFIO_L0_10_N/CLK3_L0/DIFFCLK1_L0_N/PLL1_CLKIN1	A5	DQS1#_L0		96.36
BANK L0	DIFFIO_L0_11_P/PLL1_CLKIN2	F7	DQ1_L0		55.63
BANK L0	DIFFIO_L0_11_N/PLL1_CLKIN3	F8	DQ1_L0		54.88
BANK L0	DIFFIO_L0_12_P/D0	B4	DQ1_L0		99.11
BANK L0	DIFFIO_L0_12_N/RRN_L0/D1	A4	DQ1_L0		102.31
BANK L0	DIFFIO_L0_13_P/RRP_L0/D2	B3	DQ2_L0		83.60
BANK L0	DIFFIO_L0_13_N/D3	A3	DQ2_L0		81.39
BANK L0	DIFFIO_L0_14_P/D4	B2	DQ2_L0		83.63
BANK L0	DIFFIO_L0_14_N/D5	A2	DQ2_L0		88.71
BANK L0	DIFFIO_L0_15_P/D6	B1	DQS2_L0		83.95
BANK L0	DIFFIO_L0_15_N/D7	A1	DQS2#_L0		88.80
BANK L0	DIFFIO_L0_16_P/D8	C1	DQ2_L0		83.45
BANK L0	DIFFIO_L0_16_N/D9	C2	DQ2_L0		79.90
BANK L0	DIFFIO_L0_17_P/D10	G4	DQ2_L0		42.29
BANK L0	DIFFIO_L0_17_N/D11	F4	DQ2_L0		43.04
BANK L0	DIFFIO_L0_18_P/D12	D1	DQ2_L0		73.38
BANK L0	DIFFIO_L0_18_N/D13	D2	DQ2_L0		76.81
BANK L0	DIFFIO_L0_19_P/D14	E1	DQ2_L0		70.58
BANK L0	DIFFIO_L0_19_N/D15	E2	DQ2_L0		71.15
BANK L1	DIFFIO_L1_0_P	G6	DQ0_L1		49.37
BANK L1	DIFFIO_L1_0_N	G5	DQ0_L1		42.54
BANK L1	DIFFIO_L1_1_P	F1	DQ0_L1		64.49
BANK L1	DIFFIO_L1_1_N	F2	DQ0_L1		64.08
BANK L1	DIFFIO_L1_2_P	H5	DQ0_L1		32.27
BANK L1	DIFFIO_L1_2_N	H6	DQ0_L1		41.62
BANK L1	DIFFIO_L1_3_P	G3	DQ0_L1		60.50
BANK L1	DIFFIO_L1_3_N	F3	DQ0_L1		60.57

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK L1	DIFFIO_L1_4_P	J6	DQS0_L1		53.89
BANK L1	DIFFIO_L1_4_N	J7	DQS0#_L1		53.47
BANK L1	DIFFIO_L1_5_P	G1	DQ0_L1		64.63
BANK L1	DIFFIO_L1_5_N	G2	DQ0_L1		64.36
BANK L1	DIFFIO_L1_6_P	J5	DQ0_L1		36.90
BANK L1	DIFFIO_L1_6_N/VREF_L1	K5	DQ0_L1		36.55
BANK L1	DIFFIO_L1_7_P	J3	DQ1_L1		58.00
BANK L1	DIFFIO_L1_7_N	H3	DQ1_L1		60.35
BANK L1	DIFFIO_L1_8_P/PLL2_CLKOUT_P	K6	DQ1_L1		45.99
BANK L1	DIFFIO_L1_8_N/PLL2_CLKOUT_N	L6	DQ1_L1		46.81
BANK L1	DIFFIO_L1_9_P/CLK0_L1/DIFFCLK0_L1_P/PLL2_CLKFB_P/XTALA_L1	H1	DQ1_L1		66.22
BANK L1	DIFFIO_L1_9_N/CLK1_L1/DIFFCLK0_L1_N/PLL2_CLKFB_N/XTALB_L1	H2	DQ1_L1		69.37
BANK L1	DIFFIO_L1_10_P/CLK2_L1/DIFFCLK1_L1_P/PLL3_CLKIN0	J1	DQS1_L1	L_A15	61.37
BANK L1	DIFFIO_L1_10_N/CLK3_L1/DIFFCLK1_L1_N/PLL3_CLKIN1	J2	DQS1#_L1	L_A14	60.51
BANK L1	DIFFIO_L1_11_P/PLL3_CLKIN2	K1	DQ1_L1	L_A13	45.08
BANK L1	DIFFIO_L1_11_N/PLL3_CLKIN3	K2	DQ1_L1	L_A12	49.87
BANK L1	DIFFIO_L1_12_P	L1	DQ1_L1	L_A11	48.16
BANK L1	DIFFIO_L1_12_N/RRN_L1	L2	DQ1_L1		49.68
BANK L1	DIFFIO_L1_13_P/RRP_L1	M7	DQ2_L1		55.58
BANK L1	DIFFIO_L1_13_N	M6	DQ2_L1	L_A10	53.67
BANK L1	DIFFIO_L1_14_P	M1	DQ2_L1	L_A9	61.19
BANK L1	DIFFIO_L1_14_N	M2	DQ2_L1	L_RESET_N	58.29
BANK L1	DIFFIO_L1_15_P	K4	DQS2_L1	L_A8	35.53
BANK L1	DIFFIO_L1_15_N	L4	DQS2#_L1	L_CKE	33.66
BANK L1	DIFFIO_L1_16_P	N1	DQ2_L1	L_A7	73.04
BANK L1	DIFFIO_L1_16_N	N2	DQ2_L1	L_A6	70.84
BANK L1	DIFFIO_L1_17_P	M5	DQ2_L1	L_A5	40.70

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK L1	DIFFIO_L1_17_N	L5	DQ2_L1	L_A4	38.59
BANK L1	DIFFIO_L1_18_P	P1	DQ2_L1	L_A3	72.48
BANK L1	DIFFIO_L1_18_N	P2	DQ2_L1	L_A2	68.86
BANK L1	DIFFIO_L1_19_P	M3	DQ2_L1	L_A1	41.37
BANK L1	DIFFIO_L1_19_N	M4	DQ2_L1	L_A0	43.25
BANK L2	DIFFIO_L2_0_P	U4	DQ0_L2	L_DQSU_GATE_OUT	137.15
BANK L2	DIFFIO_L2_0_N	V4	DQ0_L2	L_DQSU_GATE_IN	140.03
BANK L2	DIFFIO_L2_1_P	U5	DQ0_L2	L_DMU	148.53
BANK L2	DIFFIO_L2_1_N	V5	DQ0_L2	L_DQ15	146.35
BANK L2	DIFFIO_L2_2_P	U6	DQ0_L2	L_DQ14	148.92
BANK L2	DIFFIO_L2_2_N	V6	DQ0_L2	L_DQ13	145.22
BANK L2	DIFFIO_L2_3_P	U7	DQ0_L2	L_DQ12	157.16
BANK L2	DIFFIO_L2_3_N	V7	DQ0_L2	L_DQ11	155.17
BANK L2	DIFFIO_L2_4_P	U8	DQS0_L2	L_DQSU	163.94
BANK L2	DIFFIO_L2_4_N	V8	DQS0#_L2	L_DQSU_N	160.88
BANK L2	DIFFIO_L2_5_P	U9	DQ0_L2	L_DQ10	159.30
BANK L2	DIFFIO_L2_5_N	V9	DQ0_L2	L_DQ9	157.55
BANK L2	DIFFIO_L2_6_P	T4	DQ0_L2	L_DQ8	66.24
BANK L2	DIFFIO_L2_6_N/VREF_L2	R4	DQ0_L2		68.40
BANK L2	DIFFIO_L2_7_P	R1	DQ1_L2	L_CS_N	55.95
BANK L2	DIFFIO_L2_7_N	R2	DQ1_L2	L_RAS_N	56.68
BANK L2	DIFFIO_L2_8_P/PLL4_CLKOUT_P	T1	DQ1_L2	L_CAS_N	61.04
BANK L2	DIFFIO_L2_8_N/PLL4_CLKOUT_N	T2	DQ1_L2	L_BA2	62.62
BANK L2	DIFFIO_L2_9_P/CLK0_L2/DIFFCLK0_L2_P/PLL4_CLKFB_P/XTALA_L2	U1	DQ1_L2	L_BA1	65.18
BANK L2	DIFFIO_L2_9_N/CLK1_L2/DIFFCLK0_L2_N/PLL4_CLKFB_N/XTALB_L2	U2	DQ1_L2	L_BA0	67.36
BANK L2	DIFFIO_L2_10_P/CLK2_L2/DIFFCLK1_L2_P/PLL5_CLKIN0	V1	DQS1_L2	L_WE_N	79.63
BANK L2	DIFFIO_L2_10_N/CLK3_L2/DIFFCLK1_L2_N/PLL5_CLKIN1	V2	DQS1#_L2	L_ODT	75.96

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK L2	DIFFIO_L2_11_P/PLL5_CLKIN2	U3	DQ1_L2	L_CK	57.56
BANK L2	DIFFIO_L2_11_N/PLL5_CLKIN3	V3	DQ1_L2	L_CK_N	66.04
BANK L2	DIFFIO_L2_12_P	P3	DQ1_L2		74.12
BANK L2	DIFFIO_L2_12_N/RRN_L2	P4	DQ1_L2		75.57
BANK L2	DIFFIO_L2_13_P/RRP_L2	P5	DQ2_L2		38.95
BANK L2	DIFFIO_L2_13_N	P6	DQ2_L2	L_DQ7	36.50
BANK L2	DIFFIO_L2_14_P	N5	DQ2_L2	L_DQ6	62.08
BANK L2	DIFFIO_L2_14_N	N4	DQ2_L2	L_DQ5	56.31
BANK L2	DIFFIO_L2_15_P	N6	DQS2_L2	L_DQSL	33.60
BANK L2	DIFFIO_L2_15_N	N7	DQS2#_L2	L_DQSL_N	34.50
BANK L2	DIFFIO_L2_16_P	T9	DQ2_L2	L_DQ4	84.20
BANK L2	DIFFIO_L2_16_N	R9	DQ2_L2	L_DQ3	90.49
BANK L2	DIFFIO_L2_17_P	R6	DQ2_L2	L_DQ2	34.79
BANK L2	DIFFIO_L2_17_N	T6	DQ2_L2	L_DQ1	35.63
BANK L2	DIFFIO_L2_18_P	T8	DQ2_L2	L_DQ0	74.54
BANK L2	DIFFIO_L2_18_N	R8	DQ2_L2	L_DML	68.55
BANK L2	DIFFIO_L2_19_P	P8	DQ2_L2	L_DQSL_GATE_OUT	45.08
BANK L2	DIFFIO_L2_19_N	P7	DQ2_L2	L_DQSL_GATE_IN	45.62
BANK R0	DIFFIO_R0_0_P/VAUX5	E12	DQ0_R0		37.26
BANK R0	DIFFIO_R0_0_N/VAUX4	E11	DQ0_R0		40.16
BANK R0	DIFFIO_R0_1_P/VAUX3	D10	DQ0_R0		81.34
BANK R0	DIFFIO_R0_1_N/VAUX2	C10	DQ0_R0		84.32
BANK R0	DIFFIO_R0_2_P/VAUX1	C13	DQ0_R0		52.52
BANK R0	DIFFIO_R0_2_N/VAUX0	D13	DQ0_R0		56.36
BANK R0	DIFFIO_R0_3_P	D11	DQ0_R0		78.66
BANK R0	DIFFIO_R0_3_N/ECCLKIN	C11	DQ0_R0		72.38
BANK R0	DIFFIO_R0_4_P/FCS2_N	B10	DQS0_R0		92.15

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK R0	DIFFIO_R0_4_N/BFCE_N	A10	DQS0#_R0		96.42
BANK R0	DIFFIO_R0_5_P/BFOE_N	B11	DQ0_R0		94.59
BANK R0	DIFFIO_R0_5_N/BADRVO_N	A11	DQ0_R0		95.35
BANK R0	DIFFIO_R0_6_P/BFWE_N	B12	DQ0_R0		90.66
BANK R0	DIFFIO_R0_6_N/VREF_R0	A12	DQ0_R0		87.30
BANK R0	DIFFIO_R0_7_P/VS1	B13	DQ1_R0		88.24
BANK R0	DIFFIO_R0_7_N/VS0	A13	DQ1_R0		91.22
BANK R0	DIFFIO_R0_8_P/PLL0_CLKIN0	B15	DQ1_R0		74.88
BANK R0	DIFFIO_R0_8_N/PLL0_CLKIN1	A15	DQ1_R0		69.46
BANK R0	DIFFIO_R0_9_P/CLK0_R0/DIFFCLK0_R0_P/PLL0_CLKIN2/XTALA_R0	B14	DQ1_R0		80.17
BANK R0	DIFFIO_R0_9_N/CLK1_R0/DIFFCLK0_R0_N/PLL0_CLKIN3/XTALB_R0	A14	DQ1_R0		83.24
BANK R0	DIFFIO_R0_10_P/CLK2_R0/DIFFCLK1_R0_P/PLL1_CLKFB_P	B16	DQS1_R0		71.68
BANK R0	DIFFIO_R0_10_N/CLK3_R0/DIFFCLK1_R0_N/PLL1_CLKFB_N	A16	DQS1#_R0		73.19
BANK R0	DIFFIO_R0_11_P/PLL1_CLKOUT_P	C15	DQ1_R0		75.80
BANK R0	DIFFIO_R0_11_N/PLL1_CLKOUT_N	D15	DQ1_R0		77.47
BANK R0	DIFFIO_R0_12_P/D16/ADR0	B17	DQ1_R0		82.56
BANK R0	DIFFIO_R0_12_N/RRN_R0/D17/ADR1	A17	DQ1_R0		83.98
BANK R0	DIFFIO_R0_13_P/RRP_R0/D18/ADR2	F11	DQ2_R0		69.35
BANK R0	DIFFIO_R0_13_N/D19/ADR3	G11	DQ2_R0		68.46
BANK R0	DIFFIO_R0_14_P/D20/ADR4	E15	DQ2_R0		60.71
BANK R0	DIFFIO_R0_14_N/D21/ADR5	E16	DQ2_R0		59.22
BANK R0	DIFFIO_R0_15_P/D22/ADR6	F12	DQS2_R0		56.27
BANK R0	DIFFIO_R0_15_N/D23/ADR7	G12	DQS2#_R0		56.58
BANK R0	DIFFIO_R0_16_P/D24/ADR8	B18	DQ2_R0		86.88
BANK R0	DIFFIO_R0_16_N/D25/ADR9	A18	DQ2_R0		86.98
BANK R0	DIFFIO_R0_17_P/D26/ADR10	C18	DQ2_R0		80.80
BANK R0	DIFFIO_R0_17_N/D27/ADR11	C17	DQ2_R0		83.55

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK R0	DIFFIO_R0_18_P/D28/ADR12	D18	DQ2_R0		76.57
BANK R0	DIFFIO_R0_18_N/D29/ADR13	D17	DQ2_R0		76.69
BANK R0	DIFFIO_R0_19_P/D30/ADR14	E18	DQ2_R0		68.61
BANK R0	DIFFIO_R0_19_N/D31/ADR15	E17	DQ2_R0		69.46
BANK R1	DIFFIO_R1_0_P/ADR16	F14	DQ0_R1		43.89
BANK R1	DIFFIO_R1_0_N	F13	DQ0_R1		44.90
BANK R1	DIFFIO_R1_1_P/ADR17	F18	DQ0_R1		62.93
BANK R1	DIFFIO_R1_1_N/ADR18	F17	DQ0_R1		65.09
BANK R1	DIFFIO_R1_2_P/ADR19	G14	DQ0_R1		40.38
BANK R1	DIFFIO_R1_2_N/ADR20	G13	DQ0_R1		43.49
BANK R1	DIFFIO_R1_3_P/ADR21	F16	DQ0_R1		58.29
BANK R1	DIFFIO_R1_3_N/ADR22	G16	DQ0_R1		61.66
BANK R1	DIFFIO_R1_4_P/ADR23	H14	DQS0_R1		33.64
BANK R1	DIFFIO_R1_4_N/ADR24	H13	DQS0#_R1		46.74
BANK R1	DIFFIO_R1_5_P/ADR25	G18	DQ0_R1		65.19
BANK R1	DIFFIO_R1_5_N	G17	DQ0_R1		65.35
BANK R1	DIFFIO_R1_6_P	J15	DQ0_R1		26.14
BANK R1	DIFFIO_R1_6_N/VREF_R1	J14	DQ0_R1		29.29
BANK R1	DIFFIO_R1_7_P	H16	DQ1_R1		51.36
BANK R1	DIFFIO_R1_7_N	J16	DQ1_R1		51.04
BANK R1	DIFFIO_R1_8_P/PLL2_CLKIN0	K14	DQ1_R1		38.36
BANK R1	DIFFIO_R1_8_N/PLL2_CLKIN1	K15	DQ1_R1		35.62
BANK R1	DIFFIO_R1_9_P/CLK0_R1/DIFFCLK0_R1_P/PLL2_CLKIN2/XTALA_R1	H18	DQ1_R1		64.52
BANK R1	DIFFIO_R1_9_N/CLK1_R1/DIFFCLK0_R1_N/PLL2_CLKIN3/XTALB_R1	H17	DQ1_R1		65.16
BANK R1	DIFFIO_R1_10_P/CLK2_R1/DIFFCLK1_R1_P/PLL3_CLKFB_P	J18	DQS1_R1	R_A15	62.95
BANK R1	DIFFIO_R1_10_N/CLK3_R1/DIFFCLK1_R1_N/PLL3_CLKFB_N	J17	DQS1#_R1	R_A14	63.54
BANK R1	DIFFIO_R1_11_P/PLL3_CLKOUT_P	K18	DQ1_R1	R_A13	65.52

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK R1	DIFFIO_R1_11_N/PLL3_CLKOUT_N	K17	DQ1_ R1	R_A12	70.14
BANK R1	DIFFIO_R1_12_P	L18	DQ1_ R1	R_A11	74.59
BANK R1	DIFFIO_R1_12_N/RRN_R1	L17	DQ1_ R1		72.46
BANK R1	DIFFIO_R1_13_P/RRP_R1	L13	DQ2_ R1		53.16
BANK R1	DIFFIO_R1_13_N	L12	DQ2_ R1	R_A10	55.55
BANK R1	DIFFIO_R1_14_P	L16	DQ2_ R1	R_A9	63.08
BANK R1	DIFFIO_R1_14_N	M16	DQ2_ R1	R_RESET_N	63.16
BANK R1	DIFFIO_R1_15_P	M13	DQS2_ R1	R_A8	51.87
BANK R1	DIFFIO_R1_15_N	M14	DQS2# _R1	R_CKE	45.00
BANK R1	DIFFIO_R1_16_P	M18	DQ2_ R1	R_A7	71.79
BANK R1	DIFFIO_R1_16_N	M17	DQ2_ R1	R_A6	73.08
BANK R1	DIFFIO_R1_17_P	N18	DQ2_ R1	R_A5	74.86
BANK R1	DIFFIO_R1_17_N	N17	DQ2_ R1	R_A4	76.01
BANK R1	DIFFIO_R1_18_P	N15	DQ2_ R1	R_A3	71.90
BANK R1	DIFFIO_R1_18_N	N16	DQ2_ R1	R_A2	68.71
BANK R1	DIFFIO_R1_19_P	L15	DQ2_ R1	R_A1	33.89
BANK R1	DIFFIO_R1_19_N	L14	DQ2_ R1	R_A0	35.07
BANK R2	DIFFIO_R2_0_P	R10	DQ0_ R2	R_DQSU_GA TE_OUT	92.05
BANK R2	DIFFIO_R2_0_N	T10	DQ0_ R2	R_DQSU_GA TE_IN	95.05
BANK R2	DIFFIO_R2_1_P	U10	DQ0_ R2	R_DMU	161.45
BANK R2	DIFFIO_R2_1_N	V10	DQ0_ R2	R_DQ15	168.07
BANK R2	DIFFIO_R2_2_P	U13	DQ0_ R2	R_DQ14	144.18
BANK R2	DIFFIO_R2_2_N	V13	DQ0_ R2	R_DQ13	142.82
BANK R2	DIFFIO_R2_3_P	U12	DQ0_ R2	R_DQ12	145.75
BANK R2	DIFFIO_R2_3_N	V12	DQ0_ R2	R_DQ11	141.88
BANK R2	DIFFIO_R2_4_P	U11	DQS0_ R2	R_DQSU	157.21
BANK R2	DIFFIO_R2_4_N	V11	DQS0# _R2	R_DQSU_N	164.40

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK R2	DIFFIO_R2_5_P	R11	DQ0_R2	R_DQ10	163.34
BANK R2	DIFFIO_R2_5_N	T11	DQ0_R2	R_DQ9	157.66
BANK R2	DIFFIO_R2_6_P	P11	DQ0_R2	R_DQ8	85.01
BANK R2	DIFFIO_R2_6_N/VREF_R2	P12	DQ0_R2		84.43
BANK R2	DIFFIO_R2_7_P	V18	DQ1_R2	R_CS_N	87.81
BANK R2	DIFFIO_R2_7_N	V17	DQ1_R2	R_RAS_N	88.57
BANK R2	DIFFIO_R2_8_P/PLL4_CLKIN0	U18	DQ1_R2	R_CAS_N	76.01
BANK R2	DIFFIO_R2_8_N/PLL4_CLKIN1	U17	DQ1_R2	R_BA2	73.36
BANK R2	DIFFIO_R2_9_P/CLK0_R2/DIFFCLK0_R2_P/PLL4_CLKIN2/XTALA_R2	T18	DQ1_R2	R_BA1	59.11
BANK R2	DIFFIO_R2_9_N/CLK1_R2/DIFFCLK0_R2_N/PLL4_CLKIN3/XTALB_R2	T17	DQ1_R2	R_BA0	62.10
BANK R2	DIFFIO_R2_10_P/CLK2_R2/DIFFCLK1_R2_P/PLL5_CLKFB_P	R17	DQS1_R2	R_WE_N	59.13
BANK R2	DIFFIO_R2_10_N/CLK3_R2/DIFFCLK1_R2_N/PLL5_CLKFB_N	R18	DQS1#_R2	R_ODT	58.01
BANK R2	DIFFIO_R2_11_P/PLL5_CLKOUT_P	P17	DQ1_R2	R_CK	61.41
BANK R2	DIFFIO_R2_11_N/PLL5_CLKOUT_N	P18	DQ1_R2	R_CK_N	62.03
BANK R2	DIFFIO_R2_12_P	R16	DQ1_R2		52.75
BANK R2	DIFFIO_R2_12_N/RRN_R2	T16	DQ1_R2		49.93
BANK R2	DIFFIO_R2_13_P/RRP_R2	U14	DQ2_R2		74.01
BANK R2	DIFFIO_R2_13_N	V14	DQ2_R2	R_DQ7	73.20
BANK R2	DIFFIO_R2_14_P	U15	DQ2_R2	R_DQ6	62.18
BANK R2	DIFFIO_R2_14_N	V15	DQ2_R2	R_DQ5	63.39
BANK R2	DIFFIO_R2_15_P	V16	DQS2_R2	R_DQSL	60.76
BANK R2	DIFFIO_R2_15_N	U16	DQS2#_R2	R_DQSL_N	60.32
BANK R2	DIFFIO_R2_16_P	R14	DQ2_R2	R_DQ4	51.55
BANK R2	DIFFIO_R2_16_N	R15	DQ2_R2	R_DQ3	53.46
BANK R2	DIFFIO_R2_17_P	R13	DQ2_R2	R_DQ2	47.78
BANK R2	DIFFIO_R2_17_N	T13	DQ2_R2	R_DQ1	47.13
BANK R2	DIFFIO_R2_18_P	P13	DQ2_R2	R_DQ0	82.10

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK R2	DIFFIO_R2_18_N	P14	DQ2_ R2	R_DML	75.91
BANK R2	DIFFIO_R2_19_P	N13	DQ2_ R2	R_DQSL_GA TE_OUT	45.87
BANK R2	DIFFIO_R2_19_N	N14	DQ2_ R2	R_DQSL_GA TE_IN	43.24
	VCC	E3			
	VCC	E4			
	VCC	E13			
	VCC	E14			
	VCC	F5			
	VCC	F6			
	VCC	H15			
	VCC	K16			
	VCC	L3			
	VCC	M9			
	VCC	M11			
	VCC	M15			
	VCC	N3			
	VCC	N8			
	VCC	N10			
	VCC	N12			
	VCC	P9			
	VCCAUX	J11			
	VCCAUX	K8			
	VCCAUX	K10			
	VCCAUX	K12			
	VCCAUX	L9			
	VCCAUX	L11			
BANK CFG	VCCAUX_A	J10			
BANK CFG	VCCEFUSE	G10			
BANK CFG	VCCIOCFG	E9			
BANK L0	VCCIOL0	C3			
BANK L0	VCCIOL0	D5			
BANK L0	VCCIOL0	D7			
BANK L1	VCCIOL1	H7			
BANK L1	VCCIOL1	J4			

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
BANK L1	VCCIOL1	K7			
BANK L2	VCCIOL2	R3			
BANK L2	VCCIOL2	R5			
BANK L2	VCCIOL2	R7			
BANK R0	VCCIOR0	C16			
BANK R0	VCCIOR0	D12			
BANK R0	VCCIOR0	D14			
BANK R1	VCCIOR1	G15			
BANK R1	VCCIOR1	H12			
BANK R1	VCCIOR1	K13			
BANK R2	VCCIOR2	P15			
BANK R2	VCCIOR2	R12			
BANK R2	VCCIOR2	T14			
	VSS	C5			
	VSS	C7			
	VSS	C12			
	VSS	C14			
	VSS	D3			
	VSS	D16			
	VSS	E10			
	VSS	F15			
	VSS	G7			
	VSS	H4			
	VSS	J12			
	VSS	J13			
	VSS	K3			
	VSS	K11			
	VSS	L7			
	VSS	L8			
	VSS	L10			
	VSS	M8			
	VSS	M10			
	VSS	M12			

Bank Name	Ball Name (Function Name)	Ball Number	DQS Group	Memory Byte Group	Time Delay(PS)
	VSS	N9			
	VSS	N11			
	VSS	P10			
	VSS	P16			
	VSS	T3			
	VSS	T5			
	VSS	T7			
	VSS	T12			
	VSS	T15			
BANK CFG	VSSA	K9			

2.2.6 Thermal Resistance

Table 2-2 Thermal Resistance

θJA(℃/W) (Flow: 0m/s)	θJB (℃/W)	θJC (℃/W)	θJA(℃/W) (Flow: 1m/s)	θJA(℃/W) (Flow: 2m/s)
21.2	10.2	9.6	19.7	18.4

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