Logos2 Family FPGA Input/Output Interface (IO) User Guide

(UG040006, V1.2)

(14.07.2023)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	14.07.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
IOBSHR	IO Buffer Single Ended High Range
IOBDHR	IO Buffer Single Differential High Range
FDC	FPGA Design Constraint
UCE	User Constraint Editor
ISERDES	Input SERializer DESerializer
OSERDES	Output SERializer DESerializer
HS	High Speed
LP	Low Power

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Chapter 1 Overview of IO Unit

The parameters and specifications in the document are design objectives and may differ from the actual parameters.

The Logos2 Family programmable logic devices feature configurable high-performance IO drivers and receivers and support various standard interfaces.

The IO units of Logos2 Family products mainly consist of IO BUFFER and IO LOGIC, typically distributed in pairs, with the structural diagram as follows:

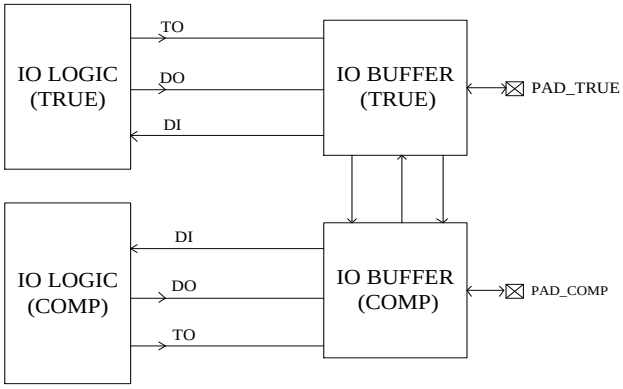


Figure 1-1 IO Structure Diagram

Each IO BUFFER is directly connected to an IO LOGIC, which includes data input and output, as well as the tri-state control signal of the IO BUFFER. IO LOGIC can be configured as either ISERDES or OSERDES.

The single-ended IO standards supported by the Logos2 Family products include LVCMOS, LVTTL33, SSTL, HSTL, HSUL, LPDDR and PCI33.

The true differential IO standards supported by the Logos2 family products include: LVDS, Mini-LVDS, RSDS, PPDS and TMDS, while pseudo-differential standards include: BLVDS, HSUL12D, SSTL135D_I, SSTL135D_II, HSTL15D_I, HSTL15D_II, HSTL18D_I, HSTL18D_II, LPDDRD, SSTL15D_I, SSTL15D_II, SSTL18D_I and SSTL18D_II.

The IO unit of Logos2 Family products features electrostatic discharge protection to prevent device pins from electrostatic damage.

Chapter 2 Detailed Introduction to IO Unit

2.1 Logos2 Family IO BANK

2.1.1 IO BANK Arrangement

The IO unit of Logos2 Family products is arranged according to the locations of BANKs. PG2L100H has 6 BANKs, arranged as shown in the following diagram.

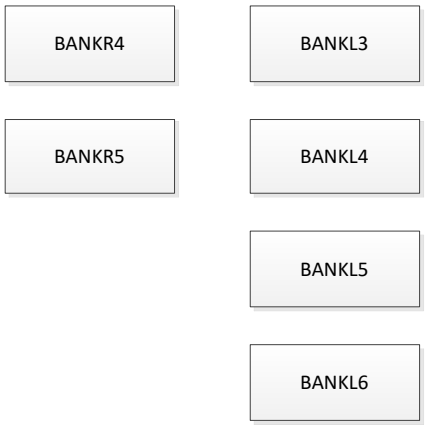


Figure 2-1 Top View of PG2L100H I/O BANK Arrangement

2.1.2 IO BANK Voltage

The Logos2 Family products limit the IO standards used within the BANK; the voltage of the output standards must match VCCIO. Logos2 products have built-in dedicated circuits that allow input standards to be compatible with different VCCIOs to a certain extent. For the input-output combination modes for mixed voltage LVCMOS level standard within the BANK, refer to the following table:

Table 2-1 Input-Output Combination Modes for Mixed-Voltage LVCMOS Level Standard Within BANK

VCCIO (V)	**Input (V)**					**Output (V)**				
	1.2	**1.5**	**1.8**	**2.5**	**3.3**	**1.2**	**1.5**	**1.8**	**2.5**	**3.3**
1.2	√					√				
1.5		√					√			
1.8			√					√		
2.5				√					√	
3.3					√					√

For any IO standard used within a BANK, its VCCIO level must adhere to limitations, which will be checked by the Pango Design Suite software.

If a BANK does not require VCCIO setup, connect VCCIO to a valid voltage.

2.2 IO BUFFER

Logos2 Family products all feature configurable high-performance I/O drivers and receivers and support a variety of IO standards. They allow programmatical setup of output drive current, slew rate, and on-chip termination resistance. Each bank has 50 pins, of which 2 pins can only be used for single-ended, while the other 48 pins can be used for either single-ended or differential.

2.2.1 IO BUFFER Structure

Each IO BUFFER includes input, output, and tri-state IO drivers. These drivers can be configured to various types of IO standards. The IO BUFFER has 2 golden models.

- IOBSHR (IOBS)

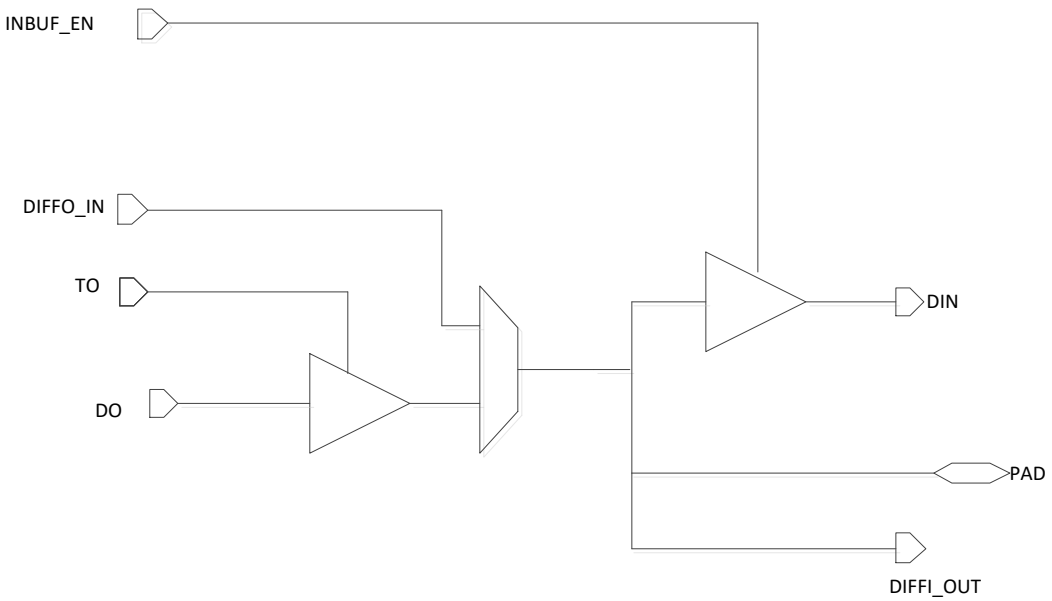


Figure 2-2 IO BUFFER Golden Model (IOBSHR)

- IOBDHR (IOBD)

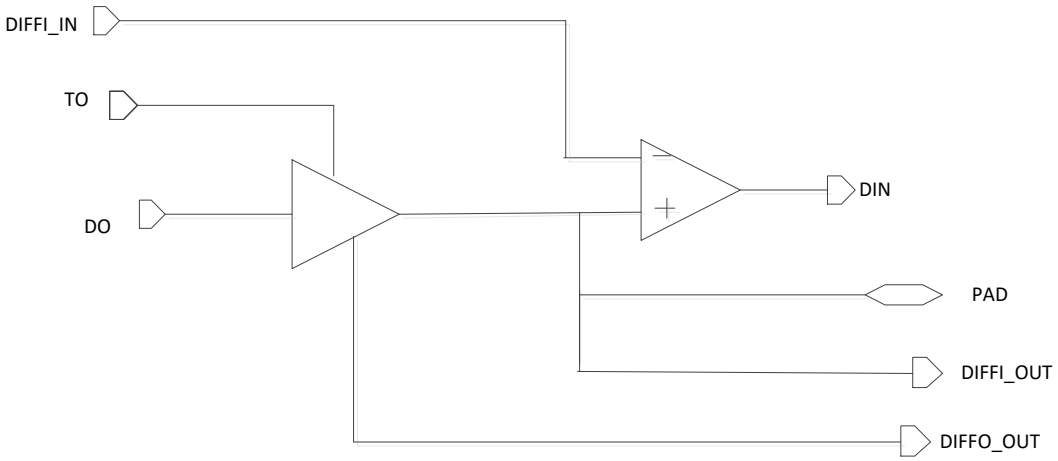


Figure 2-3 IO BUFFER Golden Model (IOBDHR)

2.2.2 Termination Matching Resistors

Termination matching resistors are commonly used to meet signal integrity requirements when using high-speed IO standards. Termination matching resistors should be placed as close to the receiver as possible to minimize interference with signal integrity.

For Logos2 Family FPGAs, termination resistors are provided for differential interfaces (such as LVDS) and single-ended interfaces (such as SSTL). If termination resistors are configured within the IO BUFFER, external termination resistors are not needed.

- Termination Matching of Differential Signal:

  Differential inputs use 100Ω parallel resistors. The following diagram shows the structure of external termination resistors.

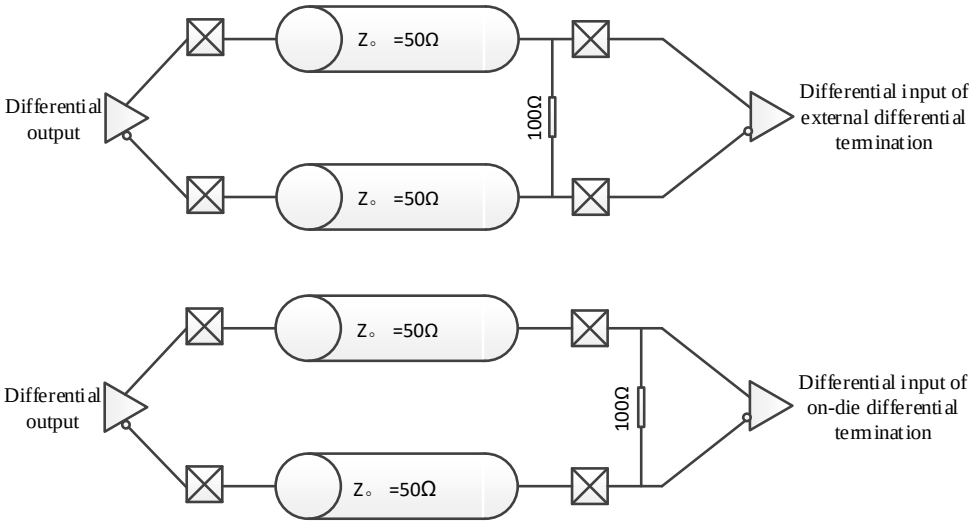
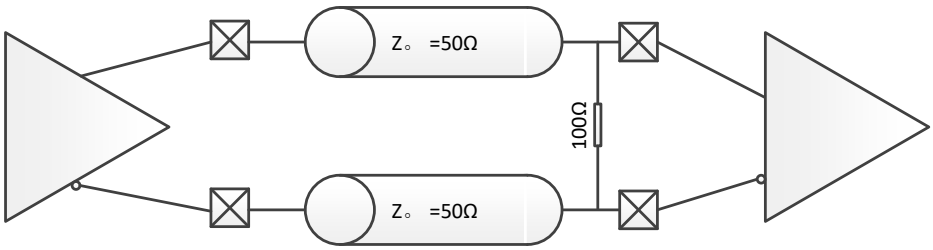


Figure 2-4 Termination Resistors for Differential Signals

Logos2 Family FPGAs offer optional on-chip differential terminations that can eliminate the need for 100Ω external termination resistors shown in the figure above. This type of on-chip differential termination resistor is fully compatible with LVDS level standards without any adjustment.

Optional on-chip differential terminations can be configured through IO constraints. The figure below presents different implementation methods using on-chip differential terminations or external termination resistors at the differential receiver end.

a. Use external termination resistors for differential pairs, with constraint DIFF_IN_TERM_MODE=OFF



b. Differential pairs with on-die differential terminals, with constraint DIFF_IN_TERM_MODE=ON

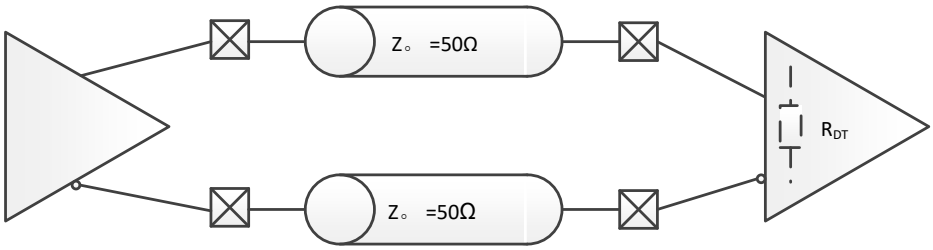


Figure 2-5 Termination Resistors Selection Method at the Differential Input End

When the attribute DIFF_IN_TERM_MODE of the IO pin is set to “ON”, the on-chip differential termination is enabled. Use the following command to set constraints in the FDC file:

define_attribute {p:*port_name*} {PAP_IO_DIFF_IN_TERM_MODE} {*ON*}

- Termination Matching of Single-Ended Signal:

  SSTL and HSTL interfaces support termination matching of single-ended signal. For high-speed single-ended signals, such as memory interfaces, Logos2 Family FPGAs offer optional on-chip termination features to eliminate the need for complex external on-board terminals.

The figure below shows how on-chip termination replaces external termination resistors.

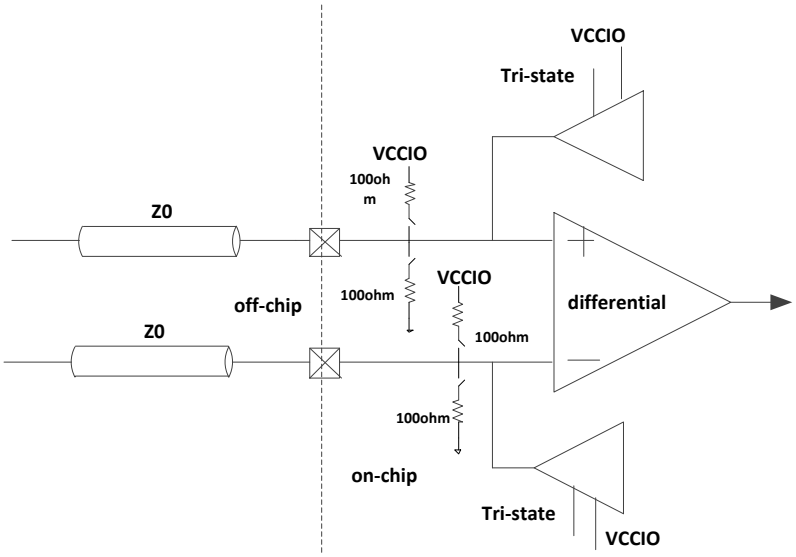


Figure 2-6 Termination Method of SSTL and HSTL Internal Resistors

In the FDC file, on-chip termination can be enabled through the IO constraint as follows:

define_attribute {p:*port_name*} {PAP_IO_DDR_TERM_MODE} {*ON*}

In which, to enable on-chip termination, select the parameter “ON”; otherwise, choose “OFF”.

2.2.3 Supported I/O Standards

The IO BUFFER of the Logos2 Family programmable logic devices supports a wide range of single-ended IO signal standards, and all IOs can be used to form differential pairs, which can support many differential signal standards. This flexibility allows users to select the most appropriate IO standard for each pin to meet the needs of interface and signal integrity. These IOs

are allocated in several independent BANKs, each with a common output voltage (VCCIO) and a common reference voltage (VREF).

The current trend in bus applications is usually led by the largest and most influential companies in the digital electronics industry. For every bus they launch, the corresponding IO standard will also be introduced. These bus IO standards provide detailed instructions for businesses that use them to design products. Each IO standard has its specific electrical characteristics: including current, voltage, IO Buffering, and termination technology. The Logos2 Family programmable logic devices are precisely in line with this trend, supporting an ever-expanding range of IO standards, and can adapt flexibly and rapidly to market demands. Configuring IO BUFFER drivers allows the IO to support multiple IO standards. The table below lists the single-ended IO standards supported by the Logos2 Family:

Table 2-2 Standards Supported by the Logos2 Family

Single-Ended IO Standard	SLEW RATE	VCCIO	IN/OUT	Supported by all BANKs
PCI33	FAST/SLOW	3.3	IN/OUT	Yes
LVTTL33	FAST/SLOW	3.3	IN/OUT/INOUT	Yes
LVCMOS33	FAST/SLOW	3.3	IN/OUT/INOUT	Yes
LVCMOS25	FAST/SLOW	2.5	IN/OUT/INOUT	Yes
LVCMOS18	FAST/SLOW	1.8	IN/OUT/INOUT	Yes
LVCMOS15	FAST/SLOW	1.5	IN/OUT/INOUT	Yes
LVCMOS12	FAST/SLOW	1.2	IN/OUT/INOUT	Yes
HSTL15_I	FAST/SLOW	1.5	IN/OUT	Yes
HSTL18_I	FAST/SLOW	1.8	IN/OUT	Yes
HSTL15_II	FAST/SLOW	1.5	IN/OUT/INOUT	Yes
HSTL18_II	FAST/SLOW	1.8	IN/OUT/INOUT	Yes
SSTL135_I	FAST/SLOW	1.35	IN/OUT/INOUT	Yes
SSTL135_II	FAST/SLOW	1.35	IN/OUT/INOUT	Yes
SSTL15_I	FAST/SLOW	1.5	IN/OUT/INOUT	Yes
SSTL15_II	FAST/SLOW	1.5	IN/OUT/INOUT	Yes
SSTL18_I	FAST/SLOW	1.8	IN/OUT	Yes
SSTL18_II	FAST/SLOW	1.8	IN/OUT/INOUT	Yes
HSUL12	FAST/SLOW	1.2	IN/OUT/INOUT	Yes
LPDDR	FAST/SLOW	1.8	IN/OUT/INOUT	Yes

LVTTL (Low-Voltage TTL): A 3.3V standard defined by JESD, requires a 3.3V VCCIO for output, without the need for reference voltage and termination voltage.

LVCMOS (Low-Voltage CMOS): A low-voltage CMOS standard, with an application voltage from 1.2V to 3.3V. No reference voltage or termination voltage required.

SSTL18 (Stub Series Terminated Logic for 1.8V): A 1.8V memory bus standard defined by JESD79-2C, requiring a 0.90V reference voltage, a 1.8V VCCIO, and a 0.90V termination voltage. SSTL18 is used for high-speed SDRAM interfaces.

SSTL15 (Stub Series Terminated Logic for 1.5V): A 1.5V memory bus standard defined by JESD79-3, requiring a 0.75V reference voltage, a 1.5V VCCIO, and a 0.75V termination voltage. SSTL15 is used for high-speed SDRAM interfaces.

SSTL135 (Stub Series Terminated Logic for 1.35V): A 1.35V memory bus standard defined by JESD79-3-1, requiring a 0.675V reference voltage, a 1.35V VCCIO, and a 0.675V termination voltage. SSTL135 is used for DDR3L SDRAM memory interfaces.

HSTL18 (High-Speed Transceiver Logic for 1.8V): A high-speed bus standard defined by IBM, requiring a 0.90V reference voltage, a 1.8V VCCIO, and a 0.90V termination voltage.

HSTL15 (High-Speed Transceiver Logic for 1.5V): A high-speed bus standard defined by IBM, requiring a 0.75V reference voltage, a 1.5V VCCIO, and a 0.75V termination voltage.

HSUL12 (High-Speed Unterminated Logic for 1.2V): A high-speed bus standard defined by JESD8-22B, requiring a 0.6V reference voltage, a 1.2V VCCIO, and a 0.6V termination voltage. HSUL12 is used to improve bus power consumption during high-speed data transmission.

Logos2 Family products feature two types of differential outputs: true differential and pseudo-differential:

True differential outputs offer higher performance through a dedicated circuit, including LVDS25, RSDS, MINI-LVDS, PPDS and TMDS. The differential pairs in the Logos2 Family products all support true differential outputs.

Pseudo-differential outputs are achieved with the help of external resistors based on the LVCMOS output standard, consisting of a single-end driven COMP PAD and TRUE PAD, that is, a complementary output mode. Pseudo-differential output mode is used to drive complementary SSTL, HSTL, HSUL standards and BLVDS.

The following table shows the differential IO standards supported by the Logos2 Family:

Table 2-3 Differential IO Standards Supported by the Logos2 Family

Differential IO Standard	**VCCIO**		**IN/OUT**	**Remarks**	**Supported by all BANKs**
	Output (V)	**Input (V)**			
LVDS25	2.5	2.5	IN/OUT	All BANKs support LVDS true differential outputs and have internal termination resistors.	Yes
RSDS	2.5	2.5	IN/OUT	With internal termination resistors	Yes
MINI-LVDS	2.5	2.5	IN/OUT	With internal termination resistors	Yes
PPDS	2.5	2.5	IN/OUT	With internal termination	Yes

Differential IO Standard	VCCIO		IN/OUT	Remarks	Supported by all BANKs
	Output (V)	Input (V)			
				resistors	
BLVDS	2.5	2.5	IN/OUT/INOUT	Bidirectional multi-point driven input and output differential signals. Outputs are supported by pseudo-differential mode with the help of peripheral resistors. Inputs are connected in differential mode	Yes
SSTL18D_I	1.8	1.8	IN/OUT	Outputs are implemented through pseudo-differential mode	Yes
SSTL18D_II	1.8	1.8	IN/OUT/INOUT	Outputs are implemented through pseudo-differential mode	Yes
SSTL15D_I	1.5	1.5	IN/OUT	Outputs are implemented through pseudo-differential mode	Yes
SSTL15D_II	1.5	1.5	IN/OUT/INOUT	Outputs are implemented through pseudo-differential mode	Yes
HSTL18D_I	1.8	1.8	IN/OUT	Outputs are implemented through pseudo-differential mode	Yes
HSTL18D_II	1.8	1.8	IN/OUT/INOUT	Outputs are implemented through pseudo-differential mode	Yes
HSTL15D_I	1.5	1.5	IN/OUT	Outputs are implemented through pseudo-differential mode	Yes
HSTL15D_II	1.5	1.5	IN/OUT/INOUT	Outputs are implemented through pseudo-differential mode	Yes
HSUL12D	1.2	1.2	IN/OUT/INOUT	Outputs are implemented through pseudo-differential mode	Yes

LVDS25 (Low Voltage Differential Signal): A differential standard where a data bit is transmitted through two signal lines, thus inherently immune to noise compared with single-ended IO standards. The voltage swing between the two signal lines is about 350mV. No reference voltage or termination voltage required. LVDS inputs require matching resistors, which can be discrete resistors on the PCB or enabled matching resistors on the chip through the DIFF_IN_TERM_MODE attribute. For PG2L100H devices, the differential pairs in each BANK support true differential LVDS25 output.

RSDS (Reduced Swing Differential Signaling): An intra-panel bus interface standard commonly used in the display sector. It defines the transmission/reception characteristics and protocol for interfaces between chips. RSDS inputs require parallel termination resistors, which can be discrete

resistors on the PCB or enabled matching resistors on the chip through the DIFF_IN_TERM_MODE attribute.

MINI-LVDS is developed based on the LVDS interface standard and is typically used in the flat panel display sector as an interface between the timing control module and the LCD. It has a smaller swing, generates very low electromagnetic interference, and can provide high bandwidth for display drivers.

PPDS (Point-to-Point Differential Signaling): The standard for internal display interfaces for next-generation LCD. PPDS inputs require parallel termination resistors, which can be discrete resistors on the PCB or enabled matching resistors on the chip through the DIFF_IN_TERM_MODE attribute.

TMDS (Transition Minimized Differential Signaling): An overmoduled differential signaling, also known as minimized transmission differential signaling, used for DVI and HDMI interfaces.

BLVDS (Bus Low Voltage Differential Signaling): An output standard similar to the MLVDS standard proposed by National Semiconductor, also used in situations requiring bidirectional multipoint driven differential signal input and output. The difference between them is that MLVDS is an industrial standard, and has a larger differential amplitude than BLVDS, requiring a higher current driving capability. The IO itself does not support BLVDS; it still requires the complementary output principle of LVCMOS and external chip resistors to implement this standard.

Differential outputs such as SSTL18D, SSTL15D, HSTL18D, HSTL15D and HSUL12D are implemented through pseudo-differential modes.

Different IO standards have different timings, which will be analysed by the Pango Design Suite software, with the result included in a timing analysis report.

IO Standards can be constrained through the following statement in the FDC file or operated on the PDS's UCE interface.

define_attribute {p:*port_name*} {PAP_IO_STANDARD} { *LVCMOS33* }

2.2.4 IO Supply Voltage Introduction

According to actual user designs, the IO BUFFER is powered by a mix of 3 main FPGA power sources: VCC, VCCA, and VCCIO.

Table 2-4 Supply Voltage Used in IO

Item	**Min.**	**Typ.**	**Max.**	**Unit**	**Description**
V_{CC}	0.95	1.0	1.05	V	Core Power Supply Voltage
V_{CCA}	1.71	1.8	1.89	V	Auxiliary power supply voltage
V_{CCIO}	1.14	--	3.465	V	Output driver power supply voltage

- VCC

  VCC is the core voltage of the FPGA chip, mainly used to power the control logic circuit of the IO BUFFER and the majority of IO LOGIC circuits. When outputting data from the core, through the IO LOGIC and IO BUFFER control logic, control signals convert the data signal power supply from VCC to higher supply voltage; when inputting data to the core, through the IO BUFFER control logic and IO LOGIC, control signals convert the data signal power supply from high supply voltage to VCC.

- VCCA

  VCCA is the auxiliary power voltage, primarily used to power differential output driving circuits, differential input circuits, and input circuits with reference voltages in SSTL and HSTL standards.

- VCCIO

  VCCIO voltage is independently supplied in each BANK, mainly for single-ended output driving circuits and ratio input circuits. Therefore, the characteristic values of IO standards powered by VCCIO will vary with VCCIO power voltage.

- GND

  Within the IO circuits, for layout planning and signal partitioning, different supply voltages correspond to different ground connections, such as VCCIO to VSSIO, VCCA to VSS, VCC to VSS, etc. However, at the chip's top level, all these IO grounds are connected to a common GND during the packaging process.

2.2.5 BUS KEEPER Feature

The main function of the BUS KEEPER circuit is to maintain the current IO data state before the next IO data becomes valid. Each IO has an independent BUS KEEPER function, typically with five programmable modes: PULLUP, PULLDW, KPR, UNUSED and NONE. NONE functions the same as UNUSED.

BUS KEEPER features can be edited through the following statement in the FDC file or operated in the PDS's UCE interface.

define_attribute {p:*port_name*} {PAP_IO_*UNUSED*} {TRUE}

2.2.6 Input Hysteresis Feature

LVCMOS33/LVTTL33/LVCMO25/LVCMOS18/ LVCMOS15/ LVCMOS12 input standards support the input hysteresis feature. The input hysteresis feature can be edited through the following statement in the FDC file or operated in the PDS's UCE interface.

define_attribute {p:*port_name*} {PAP_IO_HYS_DRIVE_MODE} {*NOHYS*}

2.2.7 IO Port State

During the power-up process, all IOs, including user IO and multiplexing IO output buffers are disabled.

After the power-up process, during initialization and programming, the multi-function IO pin IO_STATUS_C is used to control the state of all IO ports. When IO_STATUS_C input is at a low level, the internal weak pull-up of the IO is enabled. When IO_STATUS_C input is at a high level, the internal weak pull-up of the IO is disabled, and the IO output is in a high-impedance state.

After the programming process, it enters user mode, where the user logic controls the input and output modes and port states of the user IO. If persist = "on", the multi-function IO pin is still used for configuration; if persist = "off", the multi-function IO pin is used for user IO.

Note: For PG2L100H devices, after pin RSTN reset, JTAG port instruction reset, or warmboot in user mode (for details on JTAG port instruction reset and warmboot, refer to the "UG040005_Logos2 Family FPGA Configuration User Guide"), the IO may experience high pulses under the following conditions.

1. When there are IOs in BANKs L4 and L5 constrained to level standards of 1.8V and below, and VCCIOCFG is 2.5V and above, all IOs in the BANKs may experience high pulses after a device pin RSTN reset, JTAG port instruction reset, or warmboot;
2. When there are IOs constrained to level standards of 1.8V and below in BANKs other than BANKs L4 and L5 as well as the configuration-specific BANKCFG, all IOs in these BANKs may experience high pulses after a device pin RSTN reset, JTAG port instruction reset, or warmboot.

After the pin RSTN reset, JTAG port instruction reset, or warmboot, the timing sequence for IO high pulses is as follows:

For the diagram of IO high pulses upon Pin RSTN reset, refer to Figure 2-7. For T_{RSTN}, refer to "DS04001_Logos2 Family FPGA Device Data Sheet". The maximum time interval (T_R) from the pin RSTN reset signal pull-down to the emergence of IO high pulses is 500ns. The pulse width (T_W) depends on the IO link load, and users need to verify and evaluate it in hardware applications;

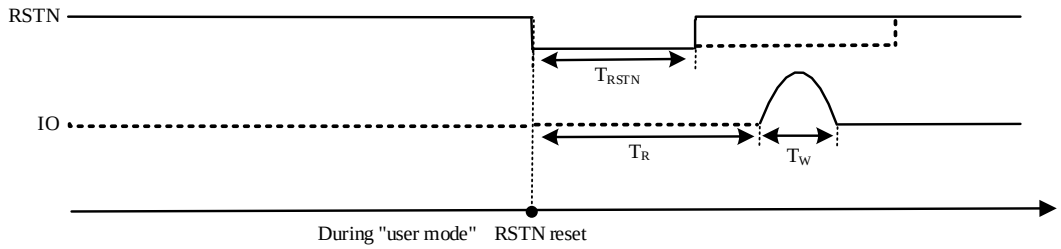


Figure 2-7 Diagram of IO High Pulses upon Pin RSTN Reset

For the diagram of IO high pulses upon JTAG port instruction reset, refer to Figure 2-8. After the JTAG instruction reset command is sent, it transitions through the Exit1_IR and Update_IR states to the Run_Test/IDLE state (for details on Exit1_IR, Update_IR, and Run_Test/IDLE states, refer to IEEE Std 1149.1). The maximum time interval (T_J) from the first TCK clock rising edge after entering the Run_Test/IDLE state to the emergence of IO high pulses is 50ns. The pulse width (T_W) depends on the IO link load, and users need to verify and evaluate it in hardware applications;

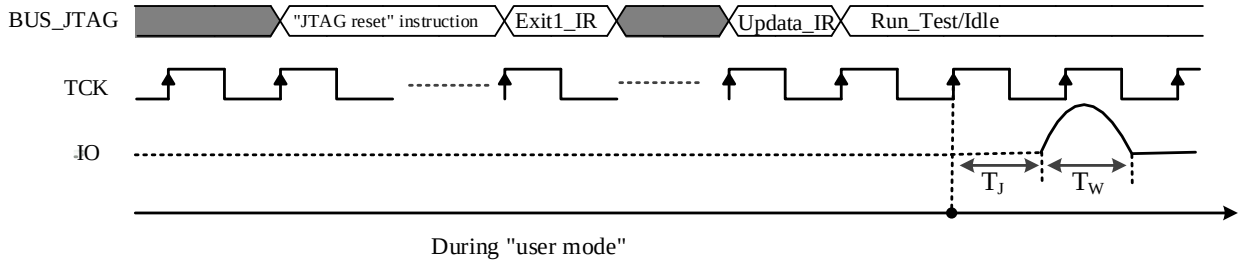


Figure 2-8 Diagram of IO High Pulses upon JTAG Port Command Reset

For the diagram of IO high pulses upon warmboot reset, refer to Figure 2-9. The maximum time interval (T_H) from the fourth CFG_CLK clock rising edge after the warmboot reset instruction is sent to the emergence of IO high pulses is 50ns. The pulse width (T_W) depends on the IO link load. and users need to verify and evaluate it in hardware applications.

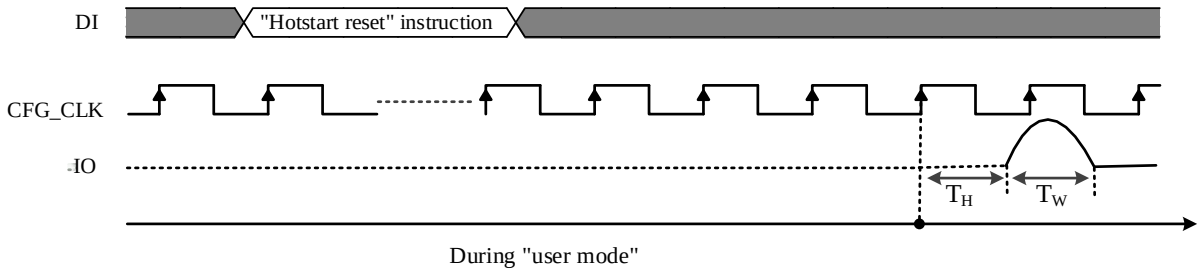


Figure 2-9 Diagram of IO High Pulses upon warmboot Reset

2.2.8 Input Buffer Types

Each input pin has two types of input buffers to meet the requirements of different input standards. The first type is the LVCMOS single-ended buffer with a power voltage of VCCIO; the second type is the input buffer with a power voltage of VCCA, which can implement input standards with reference voltage-determined thresholds and differential input standards.

Table 2-5 Input Buffer Types

		Power	Single-Ended	Dual Port	Supported Standard	Remarks
Input Buffer	**Single-Ended**	VCCIO	√		LVTTL33/LVCMOS	
	Differential	VCCA		√	SSTL/HSTL15/18, LVDS (input)	SSTL and HSTL standards require reference voltage and matching resistor support

2.2.9 Buffer Voltage Reference (VREF)

I/O standards with reference voltages, such as SSTL and HSTL, require a reference voltage to set thresholds. This reference voltage can be generated in two ways: One is to input an external reference voltage through the IO pin; the other is through an internal reference voltage generation circuit within the chip. In the first method, 2 dedicated IOs in each BANK are used as inputs for external VREFs, while in the second method, the reference voltage is provided to all IOs in the entire BANK through the chip's internal reference voltage generation circuit to support the I/O standards that require a reference voltage. Where each BANK will correspond to an internal reference voltage generation circuit, and the reference voltage output can be set through programming. Users need to set and select the method to generate the VREF reference voltage through programming as the dedicated IO for the VREF input, or as a general IO if not used as a VREF pin.

Use the following statement to set constraints in the FDC file, or operate in the PDS's UCE interface.

define_attribute {p:*port_name*} {PAP_IO_VREF_MODE_VALUE} {*0.5*}

2.2.10 Programmable Output Drive Capability

Table 2-6 Programmable Output Drive Capability

IO Standard	**Driver Strength**
PCI33	1.5mA
LVTTL33	4mA,8mA,12mA,16mA,24mA
LVCMOS33/25	4mA,8mA,12mA,16mA
LVCMOS18	4mA,8mA,12mA,16mA,24mA
LVCMOS15	4mA,8mA,12mA,16mA
LVCMOS12	4mA,8mA,12mA
HSLTL15_I	8mA
HSTL15D_I	8mA
HSTL18_I	8mA
HSTL18D_I	8mA
HSTL15_II	16mA
HSTL15D_II	16mA
HSLTL18_II	16mA
HSTL18D_II	16mA
SSTL135_I	8.9mA
SSTL135_II	13mA
SSTL15_I	8.9mA
SSTL15_II	13mA
SSTL15D_I	8.9mA
SSTL15D_II	13mA
SSTL18_I	8mA
SSTL18D_I	8mA
SSTL18_II	13.4mA
SSTL18D_II	13.4mA
HSUL12	0.1mA
HSUL12D	0.1mA
LPDDR	0.1mA
LVDS25	3mA,3.5mA,4mA,4.5mA
RSDS	
MINI-LVDS	4mA,4.5mA,5mA
PPDS	2mA,2.5mA,3mA,3.5mA,4mA
BLVDS	8mA,12mA,16mA

2.2.11 Open-Drain Control

Each IOB's single-ended output driving circuit can independently support the Open-Drain function. That is, during Open-Drain output, the output driving circuit only contains the sinking current but not the sourcing current.

Open-Drain control includes ON and OFF. Open-Drain control can be constrained using the following statement in the FDC file, or operated on the PDS's UCE interface.

define_attribute {p:port_name} {PAP_IO_OPEN_DRAIN} {OFF}

2.2.12 Tri-State Control Output

In the IO output path, each single-ended output driving circuit has an independent tri-state control circuit. Additionally, a multi-function IO pin generates a flag signal IO_STATUS for controlling the port state of all IOs during the configuration process. When IO_STATUS_C=1, it indicates that the IO is in a tri-state during configuration; when IO_STATUS_C=0, it indicates that the IO is in a pull-up state during configuration. The tri-state control of the differential driving circuit uses the tri-state control of the single-ended output driver of the TRUE pad.

2.2.13 Programmable Slew Rate

Based on the requirements to reduce output noise or enhance high-speed output performance, each IO output driver has a programmable slew rate control setting for controlling the speed of the output slew rate. The slew rate control for each IO is independent. The settable parameters are: "FAST" and "SLOW".

Programmable slew rate can be constrained using the following statement in the FDC file, or constrained in the PDS's UCE interface.

define_attribute {p:*port_name*} {PAP_IO_SLEW} {*FAST*}

2.2.14 Pseudo-Differential Output Implementation

LVDS differential structure is not used in the BLVDS output buffer. Instead, the BLVDS output interface level is achieved using two LVCMOS single-ended output buffers connected to external resistors.

- Pseudo-Differential Output - BLVDS

  BLVDS is an output standard similar to the MLVDS standard proposed by National Semiconductor, also used in situations requiring bidirectional multipoint driven differential

signal input and output. The difference between them is that MLVDS is an industrial standard, and has a larger differential amplitude than BLVDS, requiring a higher current driving capability. The IO itself does not support BLVDS; it still requires the complementary output principle of LVCMOS and external chip resistors to implement this standard. The figure below shows a typical application of BLVDS multi-point configuration. Where, the reference values of R0 and R1 should be provided based on circuit design and verification, to ensure the output levels meet the standard requirements, R1=80Ω, R1=40Ω~100Ω, with specific values determined according to the actual chip test results finally provided by the product engineers.

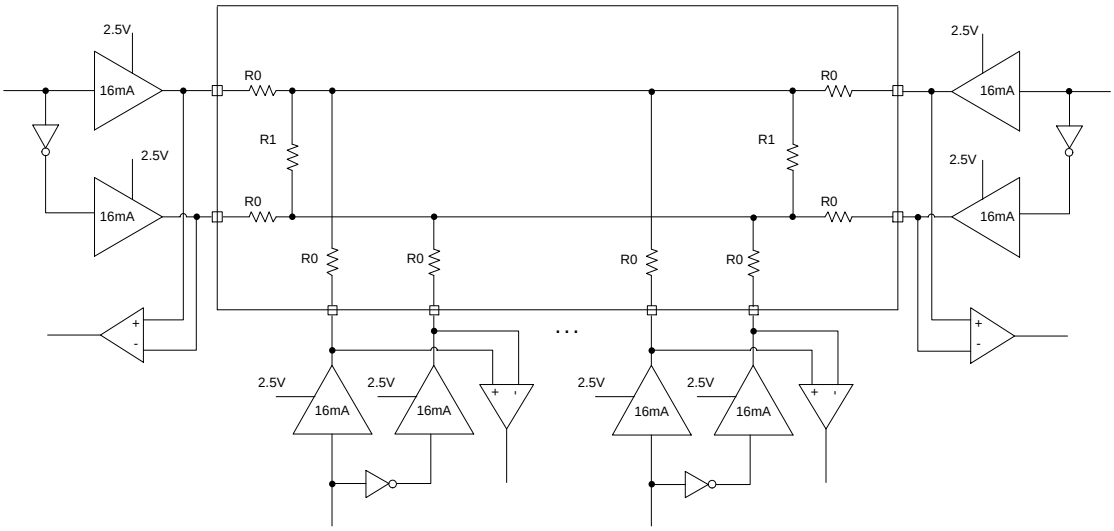
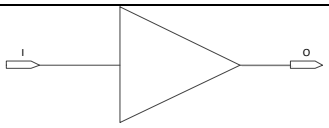
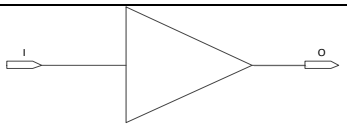
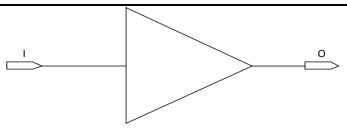


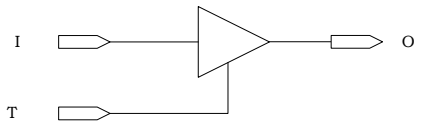
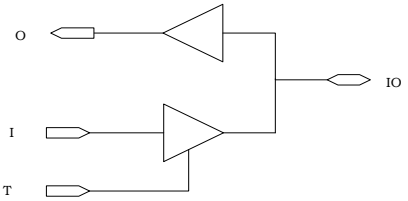
Figure 2-10 BLVDS Point-to-Point Output Example

2.2.15 Basic Prototype of GTP for IO BUFFER

The software library of Pango Design Suite includes related GTPs (General Technology Primitives) to support various I/O standards. The most common basic GTP prototypes in single-ended IO standards are listed as follows.

Table 2-7 GTPs for Single-Ended IOs

GTP Name	GTP Description	GTP Illustration
GTP_INBUF	Single-ended input signals must pass through INBUF, supporting IOBD and IOBS.	
GTP_INBUFG	INBUFG is identical to INBUF and is used for the clock input pin's input signal	
GTP_OUTBUF	Single-ended output signal	

GTP Name	GTP Description	GTP Illustration
GTP_OUTBUFT	Implement tri-state output	
GTP_IOBUF	Single-ended input/output function	

- GTP_INBUF

  Ports are described as follows:

Table 2-8 GTP_INBUF Port Description

Port	Direction	Function Description
I	IN	Single-ended signal input
O	OUT	Output from input buffer to the chip

Parameters are described as follows:

Table 2-9 GTP_INBUF Parameter Description

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	Refer to Table 2-10	LVCMOS33	Input IO standard
TERM_DDR	string	Refer to Table 2-10	ON	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs

The optional configuration attributes for the parameters are as follows:

Table 2-10 Parameter Configuration List

GTP_INBUF	
IOSTANDARD	**TERM_DDR**
LVTTL33	None
PCI33	
LVCMOS33	
LVCMOS25	
LVCMOS18	
LVCMOS15	
LVCMOS12	
SSTL18_I	OFF/ON
SSTL18_II	OFF/ON
SSTL15_I	OFF/ON

GTP_INBUF	
IOSTANDARD	**TERM_DDR**
SSTL15_II	OFF/ON
HSTL18_I	OFF/ON
HSTL18_II	OFF/ON
HSTL15_I	OFF/ON
SSTL15_I	OFF/ON
SSTL15_II	OFF/ON
HSTL15_I	OFF/ON

- GTP_INBUFG

  Ports are described as follows:

Table 2-11 GTP_INBUFG Port Description

Port	Direction	Function Description
I	IN	PAD signal input
O	OUT	Output from buffer to the chip

Parameters are described as follows:

Table 2-12 GTP_INBUFG Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	Refer to Table 2-13	LVCMOS33	Input IO standard
TERM_DDR	string	Refer to Table 2-13	ON	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs

The valid parameter values are listed as follows:

Table 2-13 Valid Parameter Values

GTP_INBUFG	
IOSTANDARD	**TERM_DDR**
LVCMOS33	None
LVCMOS25	
LVCMOS18	
LVCMOS15	
LVCMOS12	
SSTL18_I	OFF/ON
SSTL18_II	OFF/ON
SSTL15_I	OFF/ON
SSTL15_II	OFF/ON
HSTL18_I	OFF/ON

GTP_INBUFG	
IOSTANDARD	**TERM_DDR**
HSTL18_II	OFF/ON
HSTL15_I	OFF/ON
SSTL15_I	OFF/ON
SSTL15_II	OFF/ON
HSTL15_I	OFF/ON

- GTP_OUTBUF

Ports are described as follows:

Table 2-14 GTP_OUTBUF Port Descriptions

Port	Direction	Function Description
I	IN	Single-ended signal input
O	OUT	Buffer output

Parameters are described as follows:

Table 2-15 GTP_OUTBUF Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	Refer to Table 2-16	LVCMOS33	Input IO standard
SLEW_RATE	string	“SLOW”, “FAST”	SLOW	Slew rate
DRIVE_STRENGTH	string	“2”, “4”, “6”, “8”, “12”, “16”, “24”	8	Drive current strength

The valid parameter values are listed as follows:

Table 2-16 Valid Parameter Values

GTP_OUTBUF		
IOSTANDARD	**SLEW_RATE**	**DRIVE_STRENGTH**
PCI33	FAST/SLOW	“1.5”
LVTTL33	FAST/SLOW	“4”, “6”, “12”, “16”, “24”
LVCMOS33	FAST/SLOW	
LVCMOS25	FAST/SLOW	“4”, “8”, “12”, “16”
LVCMOS18	FAST/SLOW	
LVCMOS15	FAST/SLOW	“4”, “8”, “12”,
LVCMOS12	FAST/SLOW	“2”, “6”,
SSTL18_I	FAST/SLOW	
SSTL18_II	FAST/SLOW	
SSTL15_I	FAST/SLOW	
SSTL15_II	FAST/SLOW	
HSTL18_I	FAST/SLOW	

GTP_OUTBUF		
IOSTANDARD	**SLEW_RATE**	**DRIVE_STRENGTH**
HSTL18_II	FAST/SLOW	
HSTL15_I	FAST/SLOW	
SSTL15_I	FAST/SLOW	
SSTL15_II	FAST/SLOW	
HSTL15_I	FAST/SLOW	

- GTP_OUTBUFT

Ports are described as follows:

Table 2-17 GTP_OUTBUFT Port Description

Port	Direction	Function Description
I	IN	Single-ended signal input
O	OUT	Buffer output
T	IN	Enable signal; 1: Active

Parameters are described as follows:

Table 2-18 GTP_OUTBUFT Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	Refer to Table 2-19	LVCMOS33	Input IO standard
SLEW_RATE	string	“SLOW”, “FAST”	SLOW	Slew rate
DRIVE_STRENGTH	string	“2”, “4”, “6”, “8”, “12”, “16”, “24”	8	Drive current strength

The valid parameter values are listed as follows:

Table 2-19 Valid Parameter Values

GTP_OUTBUFT		
IOSTANDARD	**SLEW_RATE**	**DRIVE_STRENGTH**
PCI33	FAST/SLOW	“1.5”
LVTTL33	FAST/SLOW	“4”, “6”, “12”, “16”, “24”
LVCMOS33	FAST/SLOW	
LVCMOS25	FAST/SLOW	“4”, “8”, “12”, “16”
LVCMOS18	FAST/SLOW	
LVCMOS15	FAST/SLOW	“4”, “8”, “12”,
LVCMOS12	FAST/SLOW	“2”, “6”,
SSTL18_I	FAST/SLOW	
SSTL18_II	FAST/SLOW	
SSTL15_I	FAST/SLOW	
SSTL15_II	FAST/SLOW	

GTP_OUTBUFT		
IOSTANDARD	**SLEW_RATE**	**DRIVE_STRENGTH**
HSTL18_I	FAST/SLOW	
HSTL18_II	FAST/SLOW	
HSTL15_I	FAST/SLOW	
SSTL15_I	FAST/SLOW	
SSTL15_II	FAST/SLOW	
HSTL15_I	FAST/SLOW	

- GTP_IOBUF

  Ports are described as follows:

Table 2-20 GTP_IOBUF Port Descriptions

Port	Direction	Function Description
I	IN	Single-ended signal input
O	OUT	Output from input buffer to the chip
T	IN	Enable output buffer
IO	INOUT	PAD

Parameters are described as follows:

Table 2-21 GTP_IOBUF Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	Refer to Table 2-22	LVCMOS33	Input IO standard
TERM_DDR	string	“ON”, “OFF”	ON	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs
SLEW_RATE	string	“SLOW”, “FAST”	SLOW	Slew rate
DRIVE_STRENGTH	string	“4”, “6”, “8”, “12”, “16”, “24”	8	Drive current strength

The valid parameter values are listed as follows:

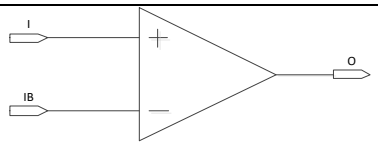
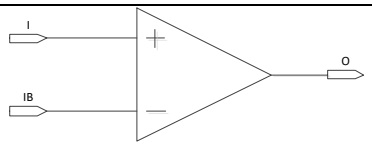
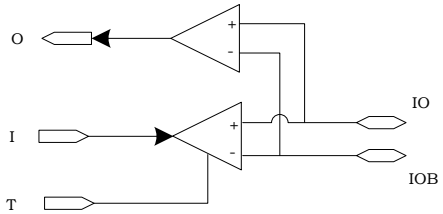
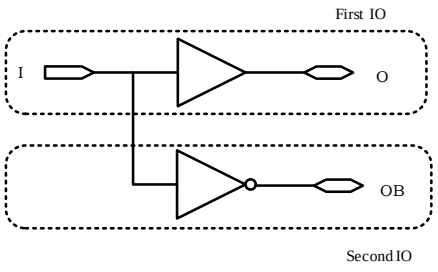
Table 2-22 Valid Parameter Values

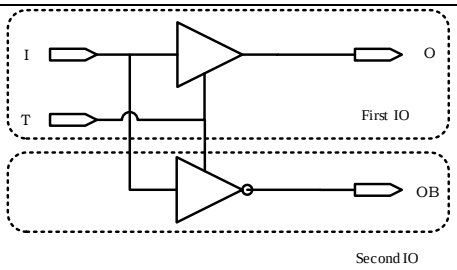
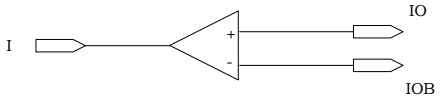
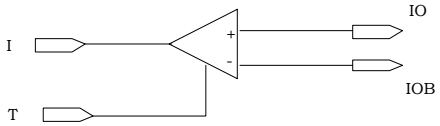
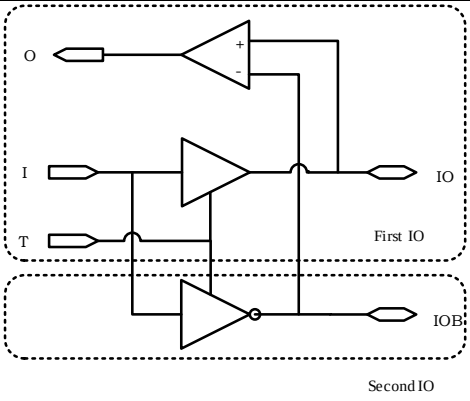
GTP_IOBUF			
IOSTANDARD	**SLEW_RATE**	**TERM_DDR**	**DRIVE_STRENGTH**
PCI33	FAST/SLOW	None	“1.5”
LVTTL33	FAST/SLOW		“4”, “6”, “12”, “16”, “24”
LVCMOS33			
LVCMOS25			“4”, “8”, “12”, “16”
LVCMOS18			
LVCMOS15			“4”, “8”, “12”,

GTP_IOBUF			
IOSTANDARD	**SLEW_RATE**	**TERM_DDR**	**DRIVE_STRENGTH**
LVCMOS12			“2”, “6”,
SSTL18_I		OFF/ON	
SSTL18_II		OFF/ON	
SSTL15_I		OFF/ON	
SSTL15_II		OFF/ON	
HSTL18_I		OFF/ON	
HSTL18_II		OFF/ON	
HSTL15_I		OFF/ON	
SSTL15_I		OFF/ON	
SSTL15_II		OFF/ON	
HSTL15_I		OFF/ON	

The table below lists the most commonly used GTPs for differential IO.

Table 2-23 Differential IO’s GTPs

GTP Name	**Description**	**Illustration**
GTP_INBUFDS	Differential input driving function. INBUFDS has 2 inputs: I and IB, representing the P-channel and N-channel input pins of the differential pair respectively.	
GTP_INBUFGDS	Differential clock input	
GTP_IOBUFDS	Supports true differential input and output	
GTP_OUTBUFCO	Pseudo-differential output driving function	

GTP Name	Description	Illustration
GTP_OUTBUFTCO	Pseudo-differential output driving function and tri-state output	
GTP_OUTBUFDS	True differential output function. IO input standards supported include: “LVDS”, “MINI-LVDS” and “TMDS”	
GTP_OUTBUFTDS	True differential output function. IO input standards supported include: “LVDS”, “MINI-LVDS”, “TMDS”	
GTP_IOBUFCO	Single-ended input and pseudo-differential output driving function	

- GTP_INBUFDS

  Ports are described as follows:

Table 2-24 GTP_INBUFDS Port Description

Port	Direction	Function Description
I	IN	Noninverting differential input
IB	IN	Inverting differential input
O	OUT	Differential output to the chip

Parameters are described as follows:

Table 2-25 GTP_INBUFDS Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	Refer to Table 2-26	LVDS	Input IO standard
TERM_DIFF	string	Refer to Table 2-26	ON	The built-in termination resistor is enabled or disabled during differential input

The valid parameter values are listed as follows:

Table 2-26 Valid Parameter Values

GTP_INBUFDS	
IOSTANDARD	**TERM_DIFF**
LVDS	OFF/ON
MINI-LVDS	OFF/ON
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON
HSTL18D_I	OFF/ON
HSTL18D_II	OFF/ON
HSTL15D_I	OFF/ON
RSDS	OFF/ON
PPDS	OFF/ON
TMDS	OFF/ON
BLVDS	NA
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON
HSTL15D_I	OFF/ON

- GTP_INBUFGDS

Ports are described as follows:

Table 2-27 GTP_INBUFGDS Port Description

Port	**Direction**	**Function Description**
I	IN	Noninverting differential input
IB	IN	Inverting differential input
O	OUT	Differential output to the chip

Parameters are described as follows:

Table 2-28 GTP_INBUFGDS Parameter Descriptions

Parameter Name	**Parameter Type**	**Valid Values**	**Defaults**	**Function Description**
IOSTANDARD	string	Refer to Table 2-29	LVDS	Input IO standard
TERM_DIFF	string	Refer to Table 2-29	ON	Internal termination resistor is enabled or disabled during differential input

The valid parameter values are listed as follows:

Table 2-29 Valid Parameter Values

GTP_INBUFGDS	
IOSTANDARD	**TERM_DIFF**
LVDS	OFF/ON
MINI-LVDS	OFF/ON
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON
HSTL18D_I	OFF/ON
HSTL18D_II	OFF/ON
HSTL15D_I	OFF/ON
HSUL12D	NA
RSDS	OFF/ON
PPDS	OFF/ON
TMDS	OFF/ON
BLVDS	NA
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON
HSTL15D_I	OFF/ON

- GTP_IOBUFDS

Ports are described as follows:

Table 2-30 GTP_IOBUFDS Port Description

Port	**Direction**	**Function Description**
I	IN	Single-ended signal input
O	OUT	Output from input buffer to the chip
T	IN	Enable signal
IO	INOUT	IO's PAD
IOB	INOUT	IO's PAD, opposite to the IO value

Parameters are described as follows:

Table 2-31 GTP_IOBUFDS Parameter Descriptions

Parameter Name	**Parameter Type**	**Valid Values**	**Defaults**	**Function Description**
IOSTANDARD	string	"LVDS", "MINI-LVDS", "TMDS"	LVDS	Input IO standard
TERM_DIFF	string	"ON", "OFF"	ON	The built-in differential termination resistor is enabled or disabled during LVDS and

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				other standard inputs

- GTP_OUTBUFCO

Ports are described as follows:

Table 2-32 GTP_OUTBUFCO Port Description

Port	Direction	Function Description
I	IN	Single-ended signal input
O	OUT	The first IO's PAD
OB	OUT	The second IO's PAD, opposite to the first IO's value

Parameters are described as follows:

Table 2-33 GTP_OUTBUFCO Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	"SSTL18D_I", "SSTL18D_II", "SSTL15D_I", "SSTL15D_II", "HSTL15D_I", "HSUL12D", "LVPECL", "RSDS", "PPDS", "BLVDS"	LVCMOS33	Input IO standard

- GTP_OUTBUFTCO

Ports are described as follows:

Table 2-34 GTP_OUTBUFTCO Port Description

Port	Direction	Function Description
I	IN	Single-ended signal input
O	OUT	The first IO's PAD
OB	OUT	The second IO's PAD, opposite to the first IO's value
T	IN	Enabled

Parameters are described as follows:

Table 2-35 GTP_OUTBUFTCO Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	"SSTL18D_I", "SSTL18D_II", "SSTL15D_I", "SSTL15D_II", "HSTL15D_I", "SSTL15D", "HSTL15D", "HSUL12D", "RSDS", "PPDS", "BLVDS"	LVCMOS33	Input IO standard

- GTP_OUTBUFDS

Ports are described as follows:

Table 2-36 GTP_OUTBUFDS Port Description

Port	Direction	Function Description
I	IN	Single-ended signal input
O	OUT	The first IO's PAD
OB	OUT	The second IO's PAD, opposite to the first IO's value

Parameters are described as follows:

Table 2-37 GTP_OUTBUFDS Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	"LVDS", "MINI-LVDS", "TMDS"	LVDS	Input IO standard

- GTP_OUTBUFTDS

Ports are described as follows:

Table 2-38 GTP_OUTBUFTDS Port Description

Port	Direction	Function Description
I	IN	Single-ended signal input
O	OUT	The first IO's PAD
OB	OUT	The second IO's PAD, opposite to the first IO's value
T	IN	Enable signal

Parameters are described as follows:

Table 2-39 GTP_OUTBUFTDS Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	"LVDS", "MINI-LVDS", "TMDS"	LVDS	Input IO standard

- GTP_IOBUFCO

Ports are described as follows:

Table 2-40 GTP_IOBUFCO Port Description

Port	Direction	Function Description
I	IN	Single-ended signal input
O	OUT	Output from input buffer to the chip
T	IN	Enable output buffer
IO	INOUT	The first IO's PAD
IOB	INOUT	The second IO's PAD, opposite to the first IO's value

Parameters are described as follows:

Table 2-41 GTP_IOBUFCO Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	“SSTL18D_I”, “SSTL18D_II”, “SSTL15D_I”, “SSTL15D_II”, “HSTL15D_I”, “SSTL15D_I”, “SSTL15D_II”, “HSTL15D”, “HSUL12D”, “RSDS”, “PPDS”, “BLVDS”	LVCMOS33	Input IO standard
TERM_DDR	string	“ON”, “OFF”	ON	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs

2.3 IO LOGIC

This section mainly describes the IOL of the Logos2 Family products.

IOL is located between the IOB and the internal logic of the FPGA, and processes data before data enters or exits the internal FPGA. IOL includes I/O delay chain units, input logic (ILOGIC), and output logic (OLOGIC). The structure is as shown below.

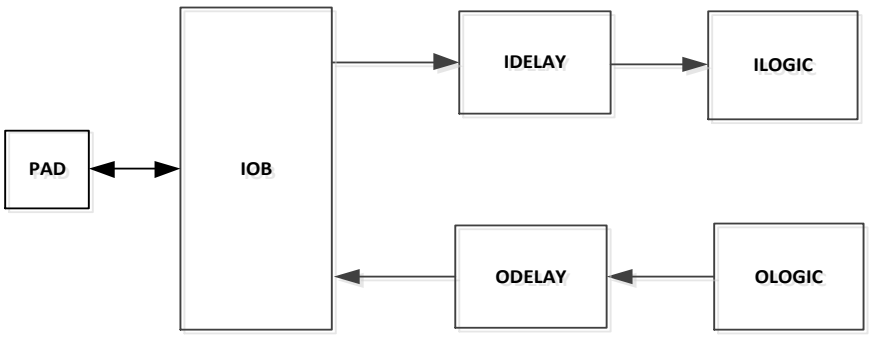


Figure 2-11 IOL Structure Block Diagram

2.3.1 I/O Delay Chain Unit

Each I/O PAD contains an IO DELAY unit that can be used for providing an input or output delay, with a maximum input delay of 247*5*2ps=2.47ns and a maximum output delay of 127*5ps=0.635ns; it can provide a DELAY mode that is either statically configured or dynamically adjusted. IO DELAY is usually used to adjust the sampling window or the output timing.

The PDS software provides dedicated primitives for using the input and output delay chains, namely GTP_IODELAY_E2 and GTP_ZEROHOLDDELAY. GTP_IODELAY_E2 is used for clock

and data delay, while GTP_ZEROHOLDDELAY is only used for data delay. The structural diagrams of both are shown below.

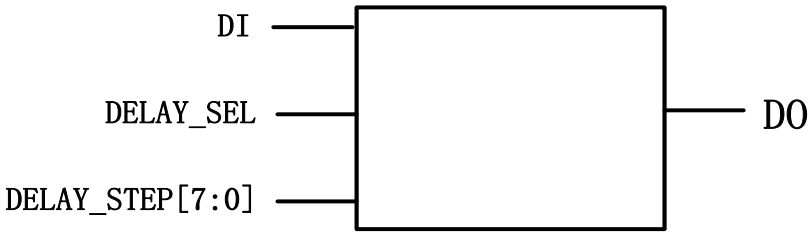


Figure 2-12 GTP_IODELAY_E2 Structure Diagram

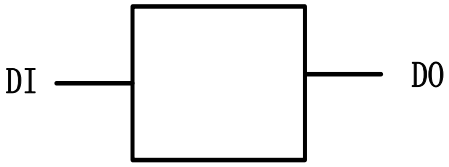


Figure 2-13 GTP_ZEROHOLDDELAY Structure Diagram

The Verilog instantiation for GTP_IODELAY_E2 is shown as follows:

```
GTP_IODELAY_E2 #
(
.DELAY_STEP_SEL (“PARAMETER”),
.DELAY_STEP_VALUE( 8’h00 )
) GTP_IODELAY_E2_inst (
.DI (di),
.DELAY_SEL (delay_sel),
.DELAY_STEP (delay_step),
.DO (do)
);
```

The parameter and signal descriptions for the GTP_IODELAY_E2 prototype module are as follows:

Table 2-42 GTP_IODELAY_E2 Port Descriptions

Port Signal	**Input/Output**	**Width**	**Defaults**	**Description**
DI	Input	1 bit		Input data
DELAY_SEL	Input	1 bit	1’b1	Cascade selection
DELAY_STEP	Input	8 bit	8’hFF	Delay step. The actual maximum effective value is

Port Signal	Input/Output	Width	Defaults	Description
				8’d247 for input delay, and 8’d127 for output delay. The input type must be grey code.
DO	Output	1 bit		Data output

Table 2-43 GTP_IODELAY_E2 Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Description
DELAY_STEP_SEL	String	“PARAMETER” “PORT”	“PARAMETER”	Select PARAMETER as the static configuration and PORT as the dynamic configuration
DELAY_STEP_VALUE	Constant	8’h00–8’hF7	8’h00	Static configuration of delay control code

The Verilog instantiation of GTP_ZEROHOLDDELAY is shown as follows:

```
GTP_ZEROHOLDDELAY #
(
. ZHOLD_SET (“NODELAY”)
) GTP_ZEROHOLDDELAY_inst (
.DI (di),
. DO (do)
);
```

Table 2-44 GTP_ZEROHOLDDELAY Port Descriptions

Port Signal	Input/Output	Width	Description
DI	Input	1 bit	Data Input
DO	Output	1 bit	Data output

Table 2-45 GTP_ZEROHOLDDELAY Parameter Descriptions

Parameter Name	Parameter Type	Valid Values	Defaults	Description
ZHOLD_SET	String	“NODELAY”, “100ps”, “200ps”, “300ps”, “400ps”, “500ps”, “600ps”, “700ps”, “800ps”, “900ps”, “1000ps”, “1100ps”, “1200ps”, “1300ps”, “1400ps”, “1500ps”	“NODELAY”	zeroholddelay delay value

2.3.2 Input Logic

The input logic of the IOL is used to process received high-speed data, converting high-speed serial data into parallel data. To achieve the serial-to-parallel conversion function in IOL, PDS provides the GTP_ISERDES_E2 primitive. GTP_ISERDES_E2 is used for data processing in the input direction, supporting direct input and output, ILATCH, IDFF, networking SDR/DDR, oversampling, Low-Speed MEMORY DDR, and High-Speed MEMORY DDR. It also supports rate conversion of SDR1TO2, SDR1TO3, SDR1TO4, SDR1TO5, SDR1TO6, SDR1TO7, SDR1TO8, DDR1TO2_SAME_PIPELINED, DDR1TO2_SAME_EDGE, DDR1TO2_OPPOSITE_EDGE, DDR1TO4, DDR1TO6, DDR1TO8, DDR1TO10, DDR1TO14, HMDDR1TO4, HMDDR1TO8, LMDDR1TO4, LMDDR1TO8, and OVERSAMPLE modes. The structure block diagram is shown below:

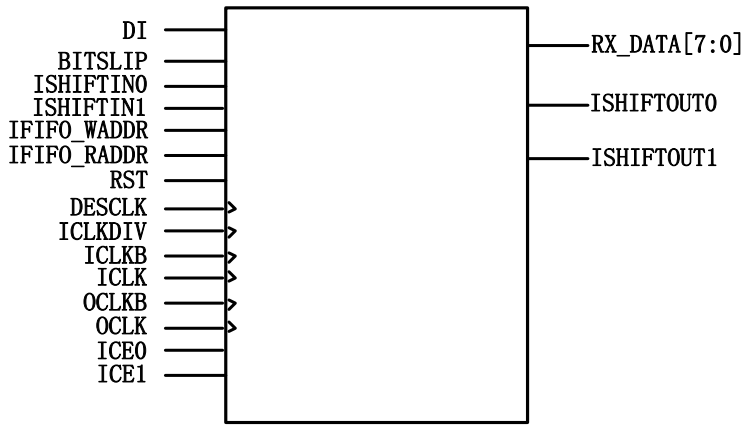


Figure 2-14 GTP_ISERDES_E2 Structure Diagram

The Verilog instantiation of GTP_ISERDES_E2 is shown as follows:

```
    GTP_ISERDES_E2 #
(
    .ISERDES_MODE (“SDR1TO4”),
    .CASCADE_(“MASTER”),
    .BITSLIP_EN(“FALSE”),
    .GRS_EN (“TRUE”),
    .NUM_ICE(1’b0),
    .GRS_TYPE_Q0(“RESET”),
    .GRS_TYPE_Q1(“RESET”),
    .GRS_TYPE_Q2(“RESET”),
    .GRS_TYPE_Q3(“RESET”),
    .LRS_TYPE_Q0(“ASYNC_RESET”),
    .LRS_TYPE_Q1(“ASYNC_RESET”),
    .LRS_TYPE_Q2(“ASYNC_RESET”),
    .LRS_TYPE_Q3(“ASYNC_RESET”)
) gtp_iserdes_inst (
    .RST(rst),
    .ICE0(ice0),
    .ICE1(ice1),
    .DESCLK (desclk),
    .ICLK (iclk),
    .ICLK DIV(iclkdiv),
    .DI (di),
    .BITSLIP(bitslip),
    .ISHIFTIN0(ishiftin0),
    .ISHIFTIN1(ishiftin1),
    .IFIFO_WADDR(ififo_waddr),
    .IFIFO_RADDR(ififo_raddr),
    .DO(DO),
    .ISHIFTOUT0(ishiftout0),
    .ISHIFTOUT1(ishiftout1)
);
```

GTP_ISERDES_E2 is usually used in conjunction with GTP_INBUF, GTP_INBUFG, GTP_INBUFDS, and GTP_INBUFGDS.

Table 2-46 GTP_ISERDES_E2 Parameter Descriptions

Parameter Name	Type	Valid Values	Defaults	Description
ISERDES_MODE	String	“SDR1TO2” “SDR1TO3” “SDR1TO4” “SDR1TO5” “SDR1TO6” “SDR1TO7” “SDR1TO8” “ILATCH “IDFF” “DDR1TO2_SAME_PIPELINED” “DDR1TO2_SAME_EDGE” “DDR1TO2_OPPOSITE_EDGE” “DDR1TO4” “DDR1TO6” “DDR1TO8” “DDR1TO10” “DDR1TO14” “HMDDR1TO4” “HMDDR1TO8” “LMDDR1TO4” “LMDDR1TO8” “OVERSAMPLE”	SDR1TO4	“SDR1TO2”: networking SDR 1:2 “SDR1TO3”: networking SDR 1:3 “SDR1TO4”: networking SDR 1:4 “SDR1TO5”: networking SDR 1:5 “SDR1TO6”: networking SDR 1:6 “SDR1TO7”: networking SDR 1:7 “SDR1TO8”: networking SDR 1:8 “ILATCH” latch input mode “IDFF” register input mode “DDR1TO2_SAME_PIPELINED”: networking DDR 1:2 SAME_PIPELINED “DDR1TO2_SAME_EDGE”: networking DDR 1:2 SAME_EDGE “DDR1TO2_OPPOSITE_EDGE”: networking DDR 1:2 OPPOSITE_EDGE “DDR1TO4”: networking DDR 1:4 “DDR1TO6”: networking DDR 1:6 “DDR1TO8”: networking DDR 1:8 “DDR1TO10”: networking DDR 1:10 “DDR1TO14”: networking DDR 1:14 deserialisation mode “HMDDR1TO4”: High-Speed Memory DDR 1:4 “HMDDR1TO8”: High-Speed Memory DDR 1:8 “LMDDR1TO4”: Low-Speed Memory DDR 1:4 “LMDDR1TO8”: Low-Speed Memory DDR 1:8 “OVERSAMPLE”
CASCADE_MODE	String	“MASTER” “SLAVE”	“MASTER”	Deserialisation cascade master mode
BITSLIP_EN	String	“FALSE” “TRUE”	“FALSE”	bitslip enabled
GRS_EN	String	“TRUE” “FALSE”	“TRUE”	Global reset/set enabled
NUM_ICE	Constance	1’b0 1’b1	1’b0	Selection of the number of ices
GRS_TYPE_Q0	String	“RESET” “SET”	“RESET”	Global asynchronous reset/set result of DFF0 in ILOGIC gear;
GRS_TYPE_Q1	String	“RESET” “SET”	“RESET”	Global asynchronous reset/set result of DFF1 in ILOGIC gear;
GRS_TYPE_Q2	String	“RESET” “SET”	“RESET”	Global asynchronous reset/set result of DFF2 in ILOGIC gear;
GRS_TYPE_Q3	String	“RESET” “SET”	“RESET”	Global asynchronous reset/set result of DFF3 in ILOGIC gear;
LRS_TYPE_Q0	String	“ASYNC_RESET” “ASYNC_SET” “SYNC_RESET”	“ASYNC_RESET”	Local asynchronous/synchronous/ reset/set result of DFF0 in ILOGIC gear

Parameter Name	Type	Valid Values	Defaults	Description
		“SYNC_SET”		
LRS_TYPE_Q1	String	“ASYNC_RESET” “ASYNC_SET” “SYNC_RESET” “SYNC_SET”	“ASYNC_RESET”	Local asynchronous/synchronous/ reset/set result of DFF1 in ILOGIC gear
LRS_TYPE_Q2	String	“ASYNC_RESET” “ASYNC_SET” “SYNC_RESET” “SYNC_SET”	“ASYNC_RESET”	Local asynchronous/synchronous/ reset/set result of DFF2 in ILOGIC gear
LRS_TYPE_Q3	String	“ASYNC_RESET” “ASYNC_SET” “SYNC_RESET” “SYNC_SET”	“ASYNC_RESET”	Local asynchronous/synchronous/ reset/set result of DFF3 in ILOGIC gear

Table 2-47 GTP_ISERDES_E2 Port Descriptions

Port	Direction	Width	Description
DI	Input	1	Data Input
BITSLIP	Input	1	Data Input
ISHIFTIN0	Input	1	Cascade input signal
ISHIFTIN1	Input	1	Cascade input signal
IFIFO_WADDR	Input	3	FIFO write pointer, grey code as input
IFIFO_RADDR	Input	3	FIFO read pointer, grey code as input
RST	Input	1	Local reset signal of ILOGIC, active-high.
DESCLK	Input	1	ILOGIC deserialisation high-speed clock
ICLKDIV	Input	1	ILOGIC low-speed clock
ICLK	Input	1	ILOGIC first-stage high-speed clock
ICE0	Input	1	Clock enable signal of ILOGIC, ICE0 enable control must be pulled up before the RST signal
ICE1	Input	1	Clock enable signal of ILOGIC, ICE1 enable control must be pulled up before the RST signal
DO	Output	8	Output signals after deserialisation, the high bits of parallel data are occupied by the low bits of received serial data. Swap the active-high and low bits based on the mode used. For example: sdr 1:4 will only use the lower 4 bits, so only the lower 4 bits need to be swapped.
ISHIFTOUT0	Output	1	Cascade output signals
ISHIFTOUT1	Output	1	Cascade output signals

2.3.2.1 Direct Input

The following describes the register input mode and latch input mode, where the input logic is configured into direct input mode.

IDFF

When the input logic is configured into IDFF mode, its functional diagram can be simplified as below.

Figure 2-15 IDFF Functional Diagram

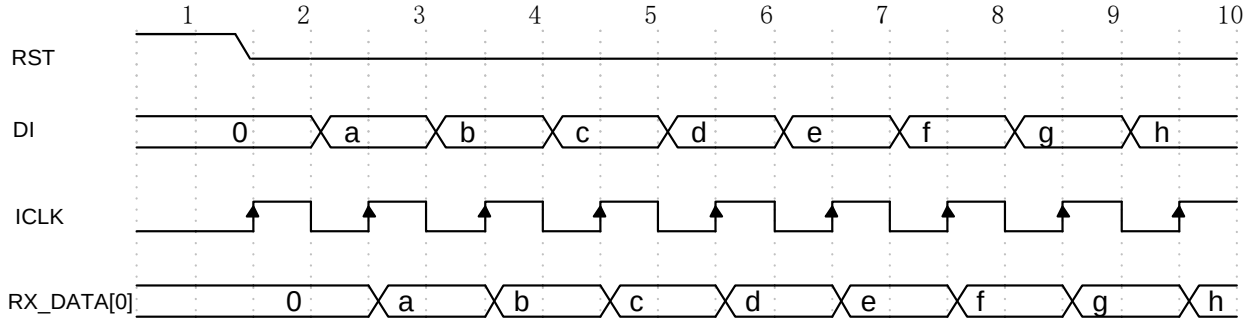


Figure 2-16 IDFF Timing Diagram

ILATCH

When the input logic is configured as ILATCH mode, its functional diagram can be simplified as below.

Figure 2-17 ILATCH Functional Diagram

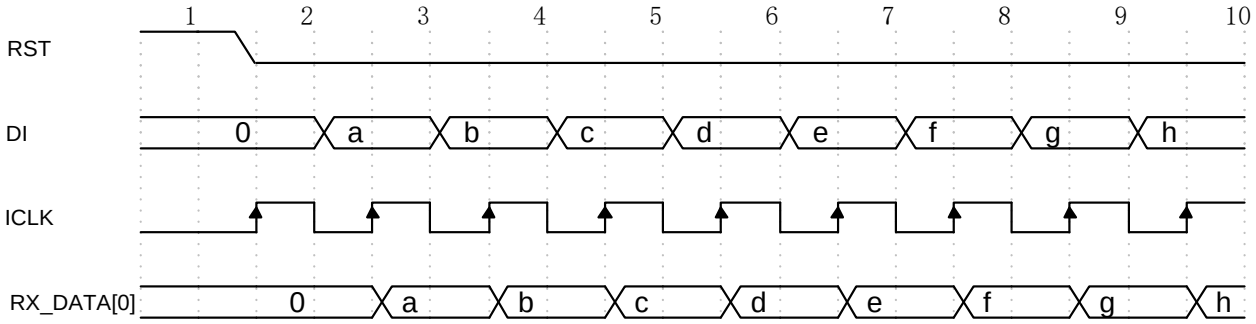


Figure 2-18 ILATCH Timing Diagram

2.3.2.2 ISERDES

The following describes the different operating modes in which the input logic is configured as ISERDES.

SDR1TO2

When the input logic is configured into SDR1TO2 mode, its functional diagram can be simplified as below.

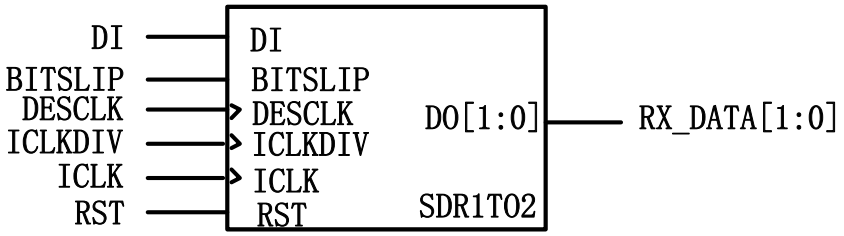


Figure 2-19 SDR1TO2 Functional Diagram

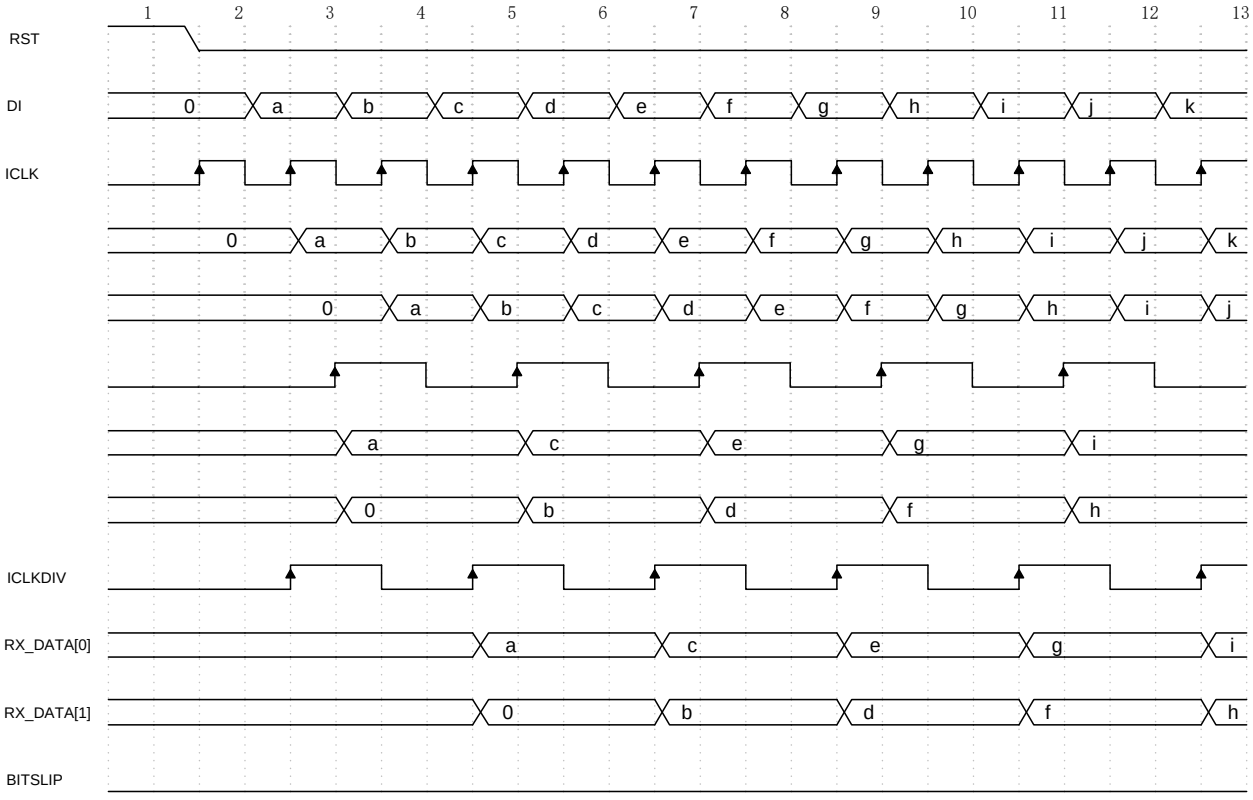


Figure 2-20 SDR1TO2 Timing Diagram

SDR1TO3

When the input logic is configured into SDR1TO3 mode, its functional diagram can be simplified as below.

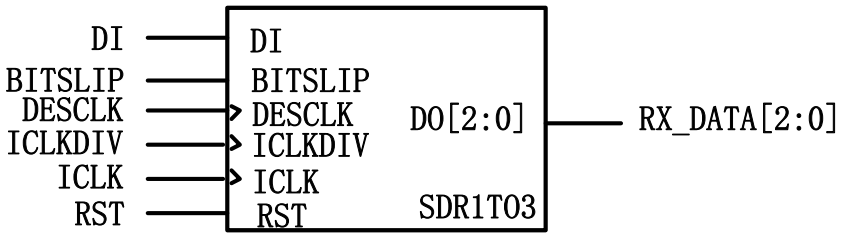


Figure 2-21 SDR1TO3 Functional Diagram

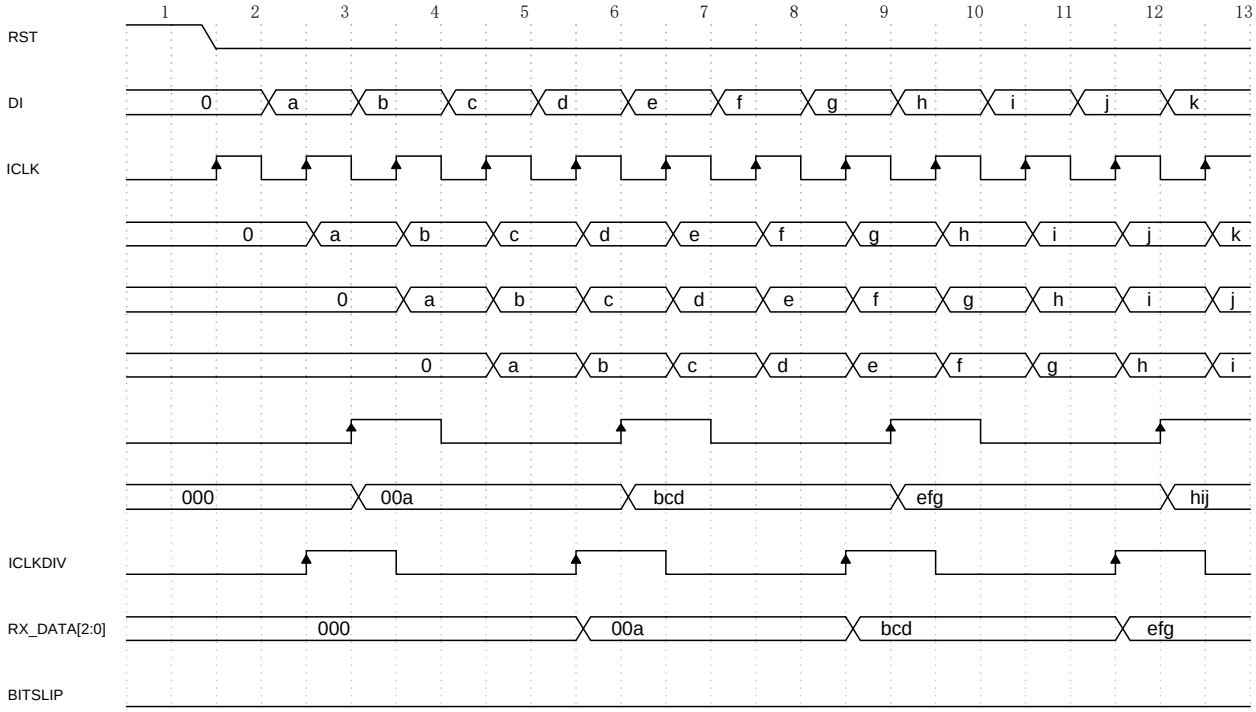


Figure 2-22 SDR1TO3 Timing Diagram

SDR1TO4

When the input logic is configured into SDR1TO4 mode, its functional diagram can be simplified as below.

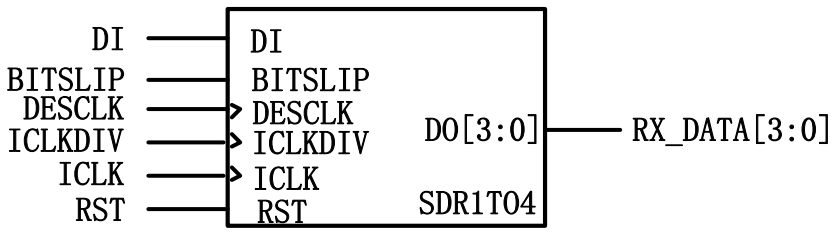


Figure 2-23 SDR1TO4 Functional Diagram

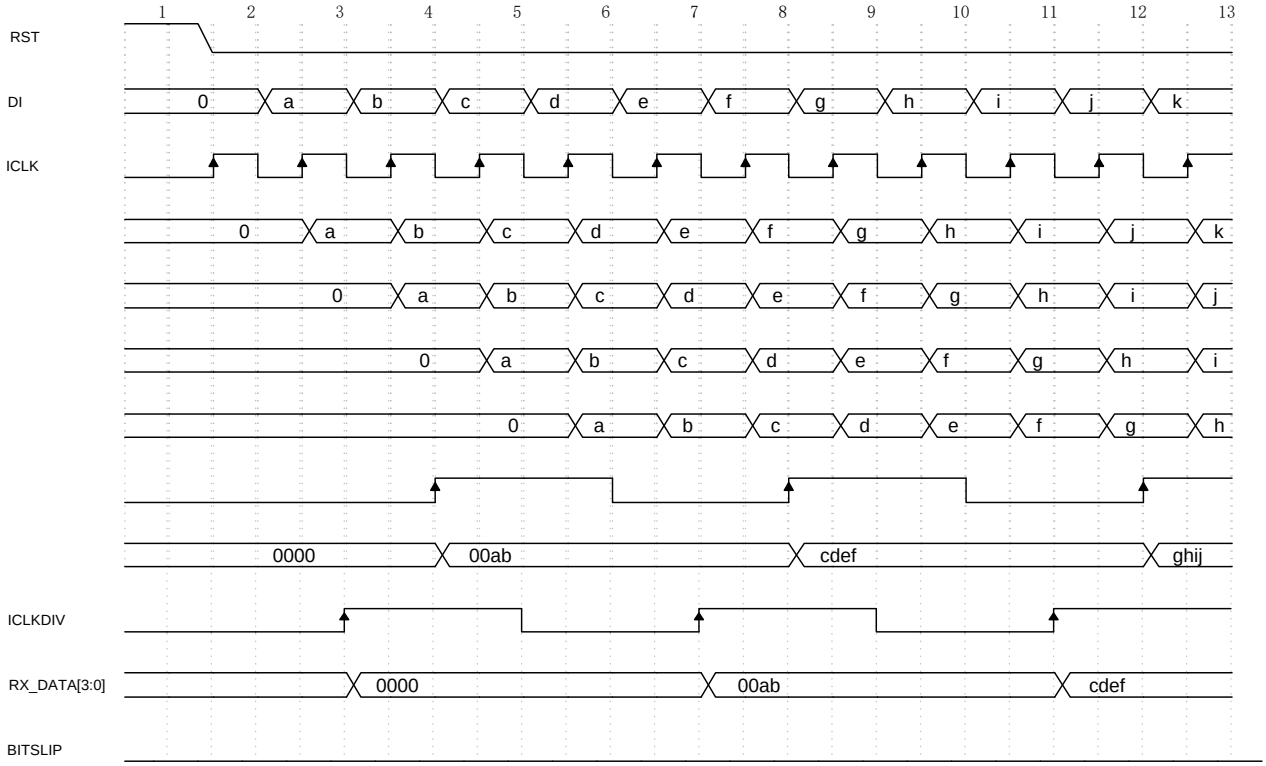


Figure 2-24 SDR1TO4 Timing Diagram

SDR1TO5

When the input logic is configured into SDR1TO5 mode, its functional diagram can be simplified as below.

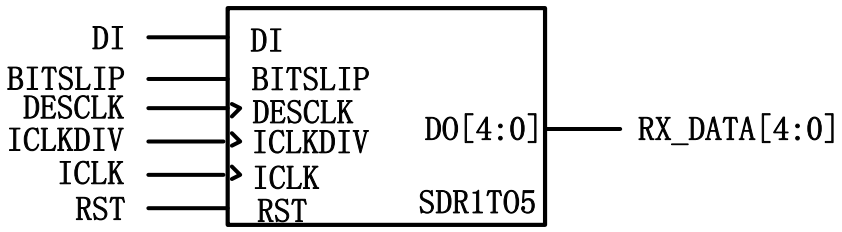


Figure 2-25 SDR1TO5 Functional Diagram

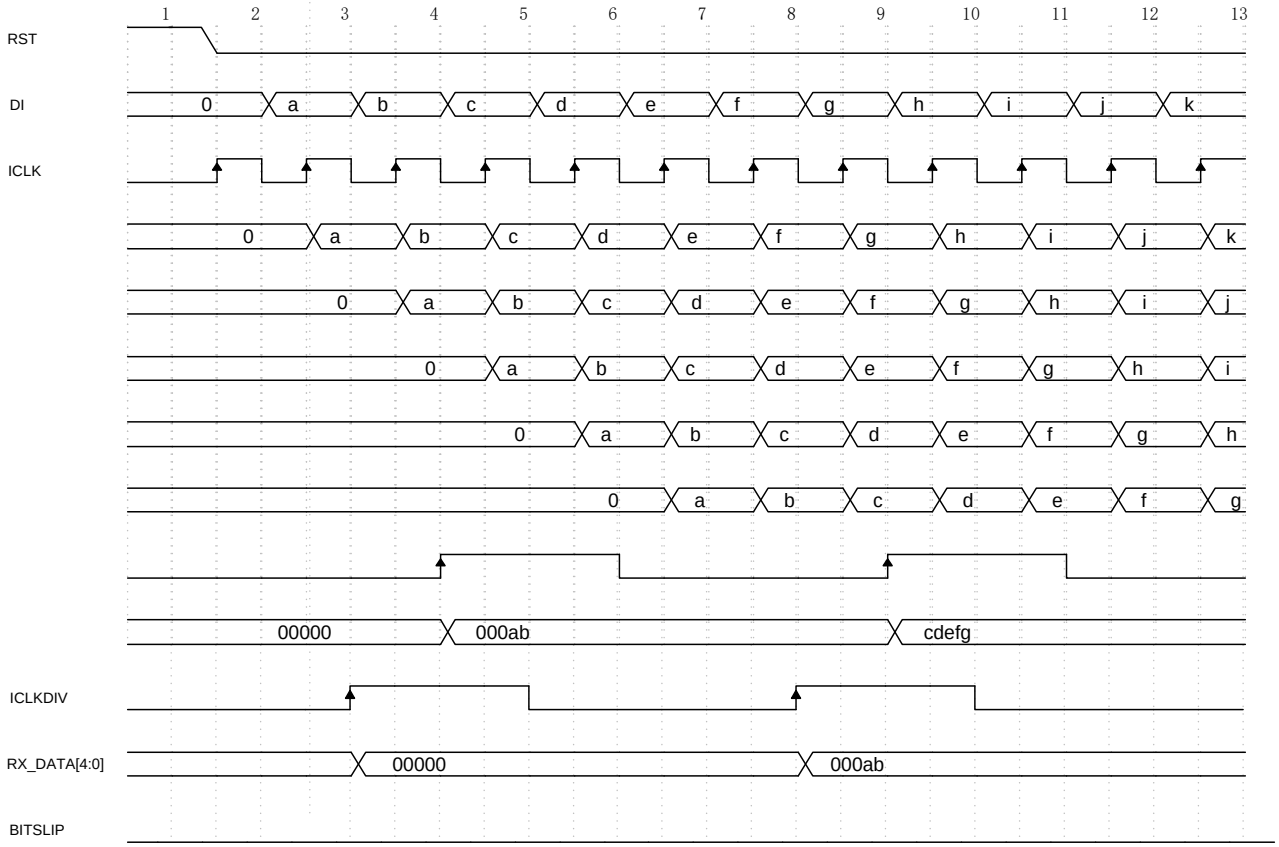


Figure 2-26 SDR1TO5 Timing Diagram

SDR1TO6

When the input logic is configured into SDR1TO6 mode, its functional diagram can be simplified as below.

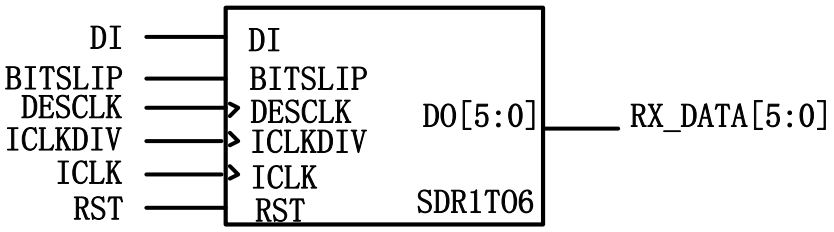


Figure 2-27 SDR1TO6 Functional Diagram

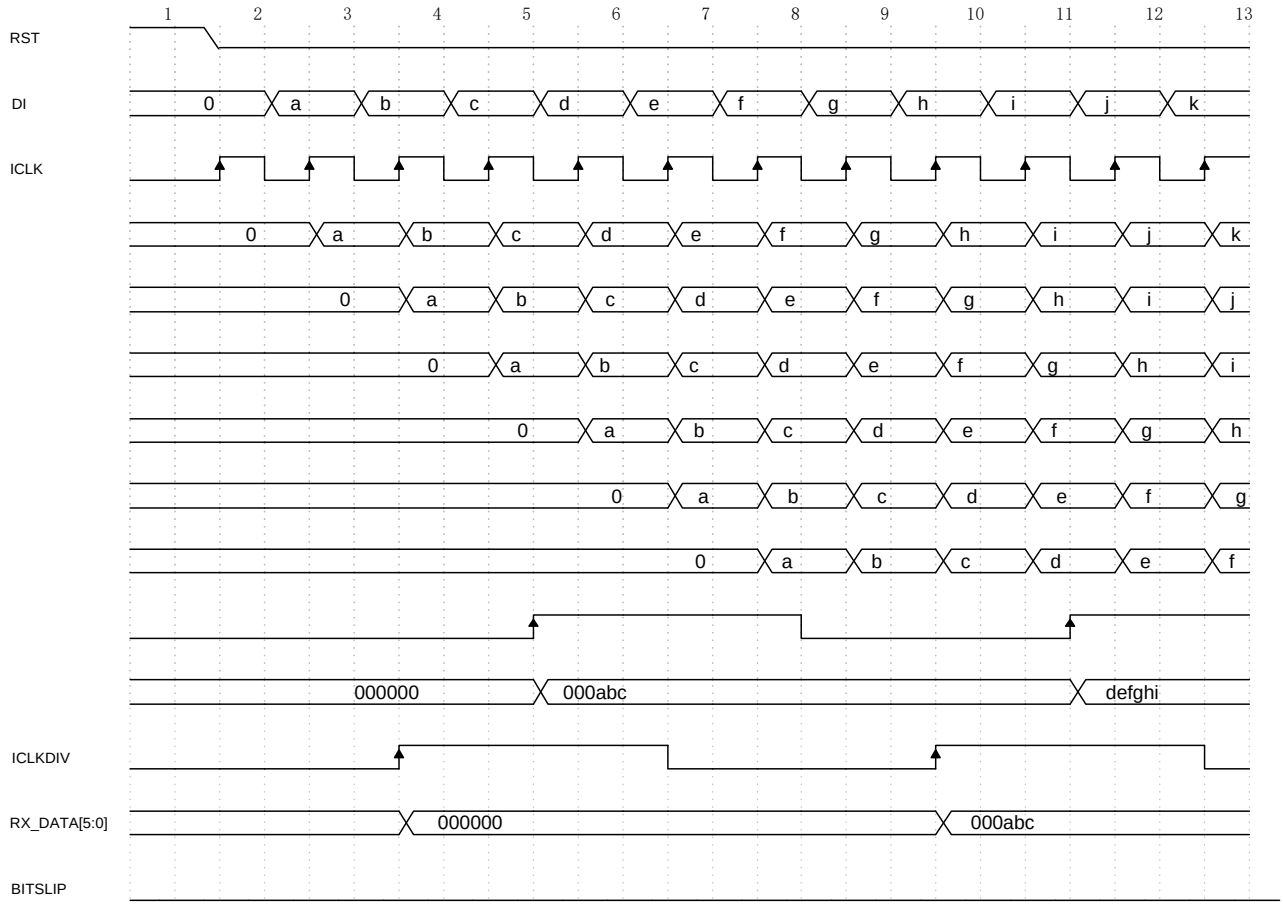


Figure 2-28 SDR1TO6 Timing Diagram

SDR1TO7

When the input logic is configured into SDR1TO7 mode, its functional diagram can be simplified as below.

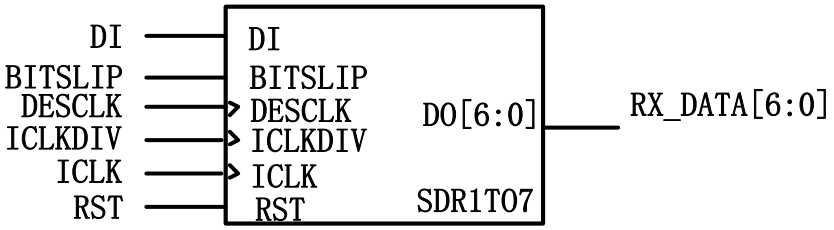


Figure 2-29 SDR1TO7 Functional Diagram

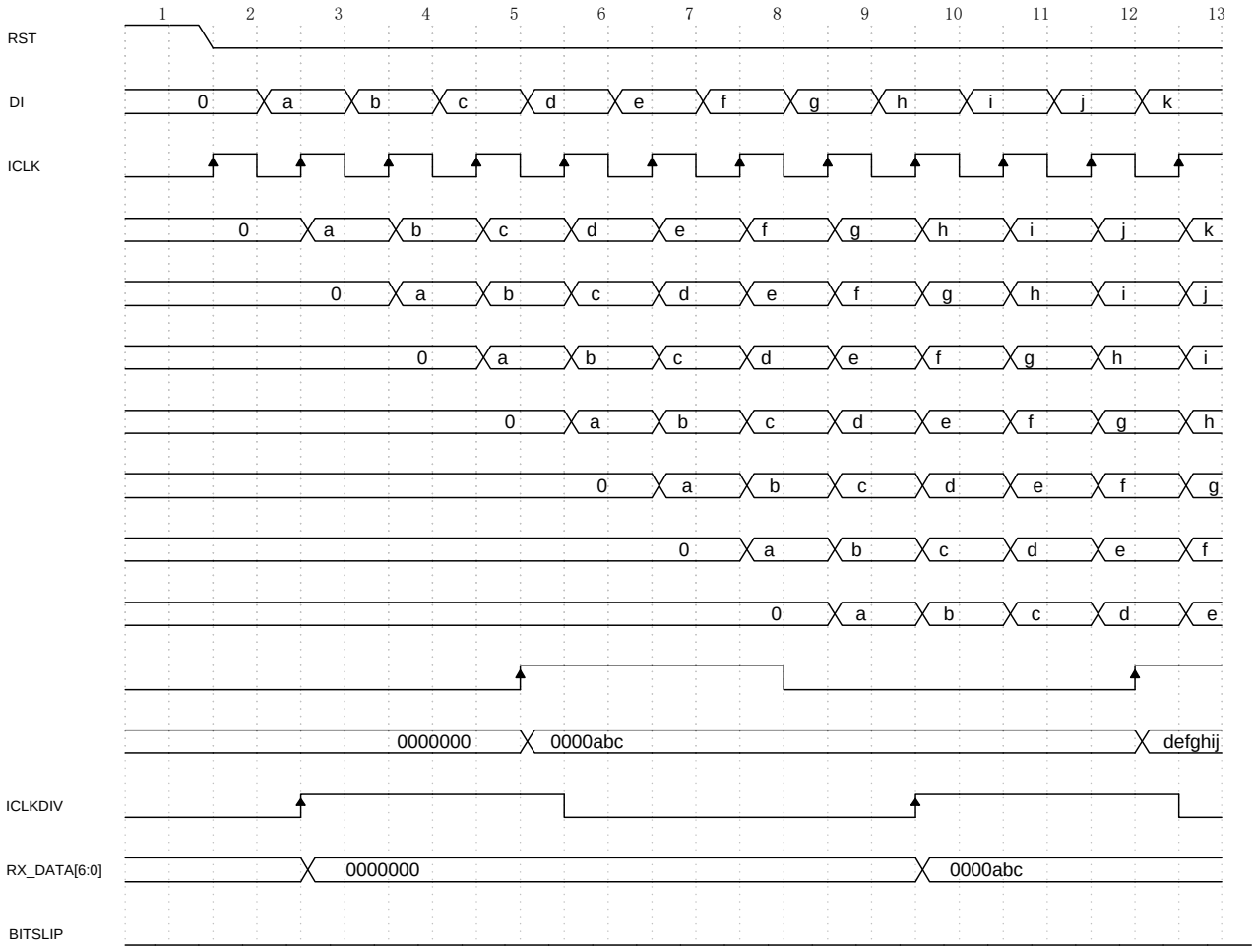


Figure 2-30 SDR1TO7 Timing Diagram

SDR1TO8

When the input logic is configured into SDR1TO8 mode, its functional diagram can be simplified as below.

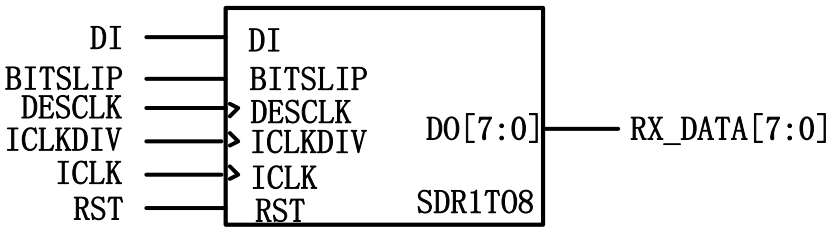


Figure 2-31 SDR1TO8 Functional Diagram

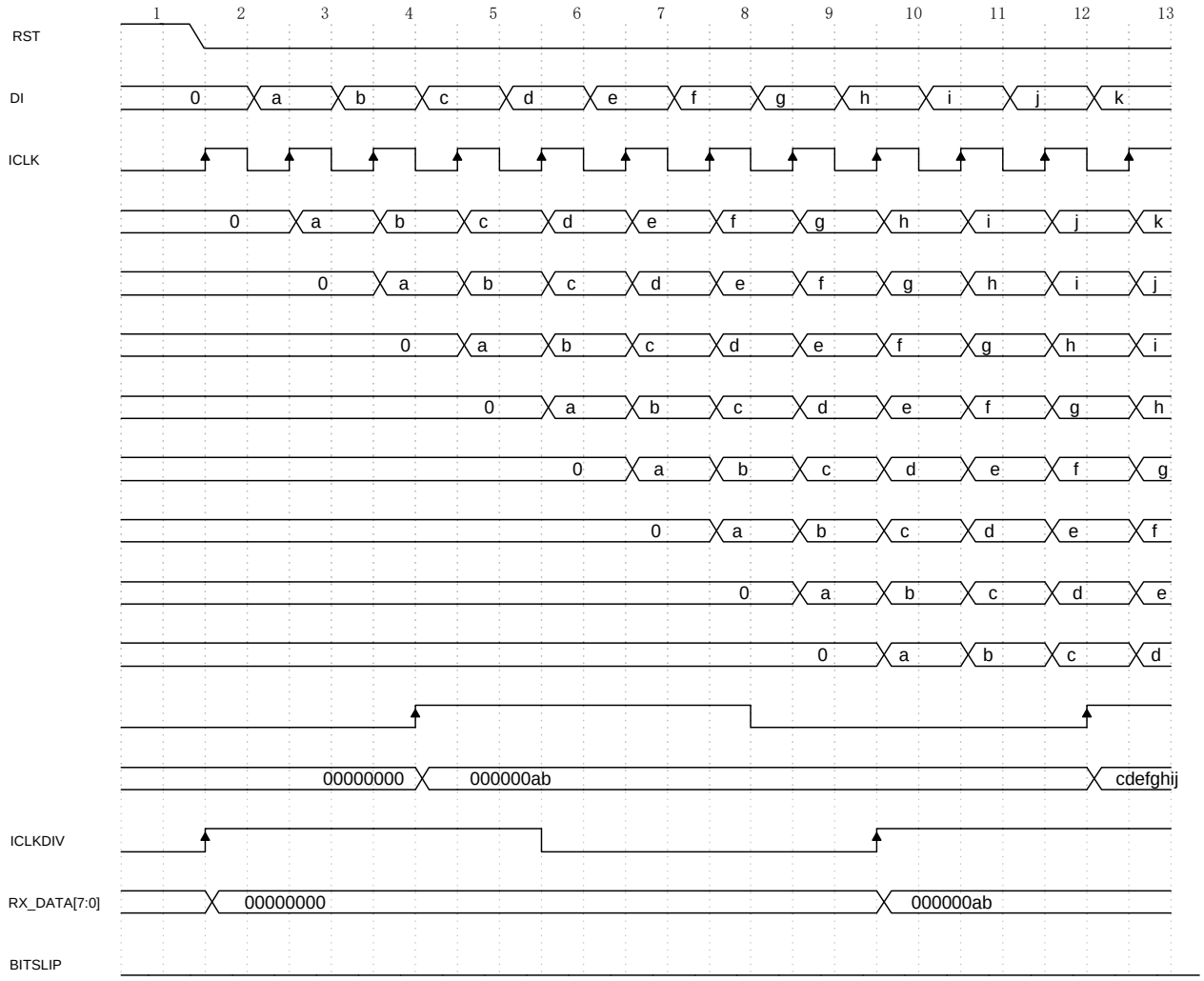


Figure 2-32 SDR1TO8 Timing Diagram

DDR1TO2_ OPPOSITE_EDGE

When the input logic is configured to DDR1TO2_OPPOSITE_EDGE mode, its functional diagram can be simplified as below.

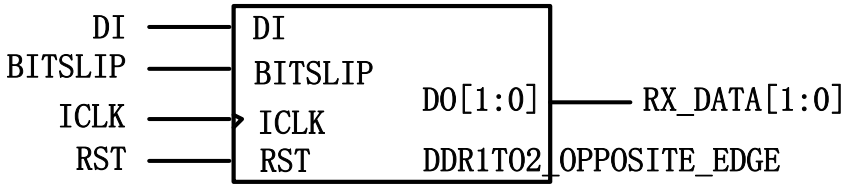


Figure 2-33 DDR1TO2_OPPOSITE_EDGE Functional Diagram

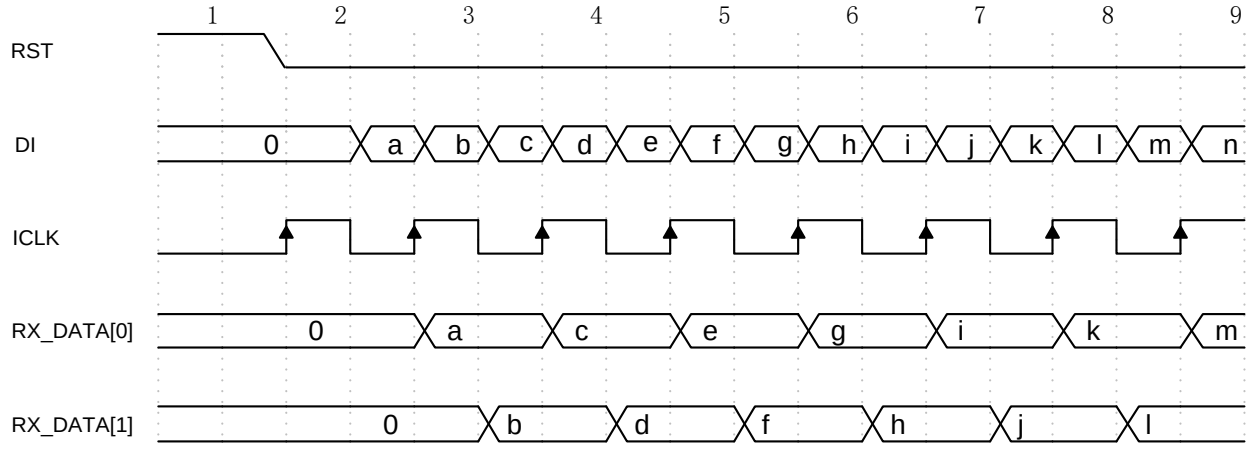


Figure 2-34 DDR1TO2_OPPOSITE_EDGE Timing Diagram

DDR1TO2_SAME_EDGE

When the input logic is configured into DDR1TO2_SAME_EDGE mode, its functional diagram can be simplified as below.

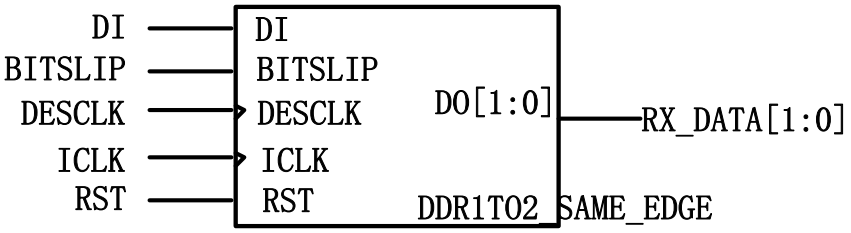


Figure 2-35 DDR1TO2_SAME_EDGE Functional Diagram

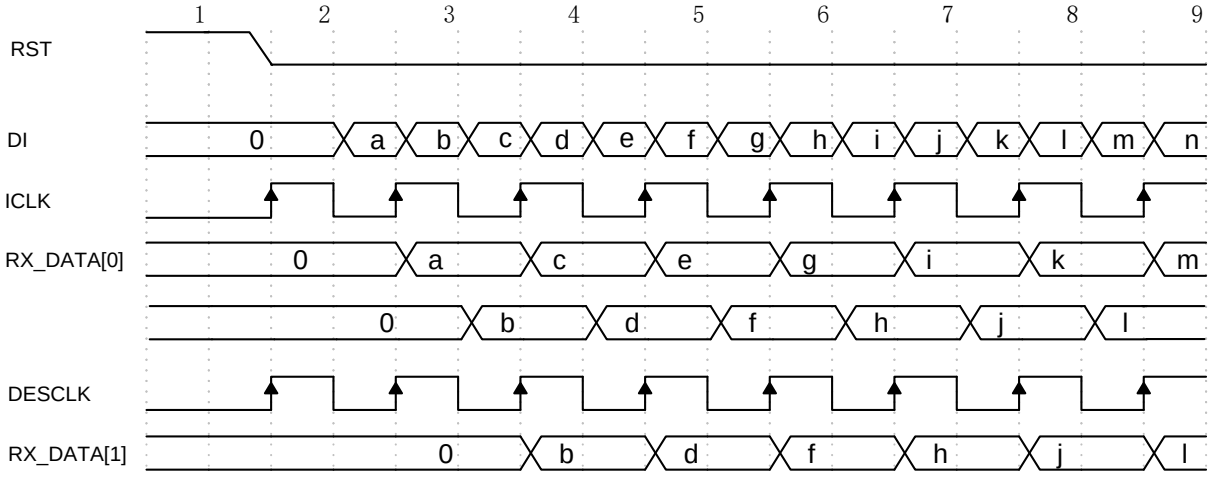


Figure 2-36 DDR1TO2_SAME_EDGE Timing Diagram

DDR1TO2_SAME_PIPELINED

When the input logic is configured into DDR1TO2_SAME_PIPELINED mode, its functional diagram can be simplified as below.

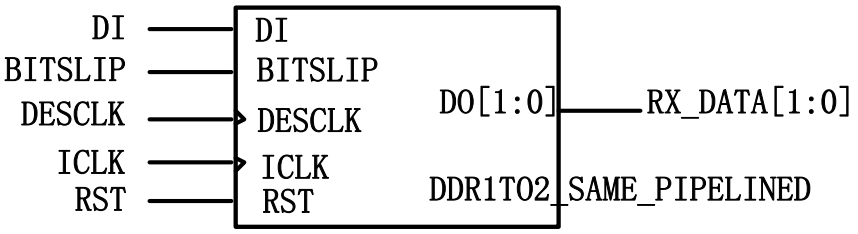


Figure 2-37 DDR1TO2_SAMEPIPELINE Functional Diagram

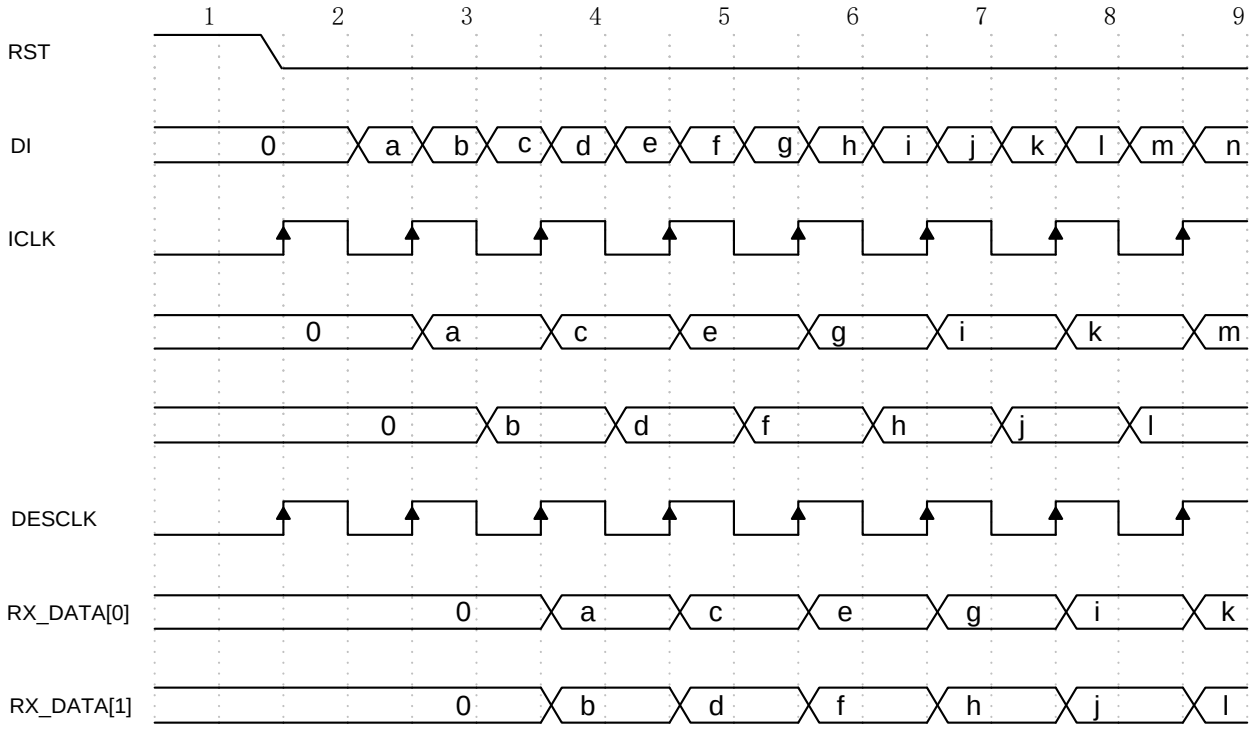


Figure 2-38 DDR1TO2_SAMEPIPELINE Timing Diagram

DDR1TO4

When the input logic is configured into DDR1TO4 mode, its functional diagram can be simplified as below.

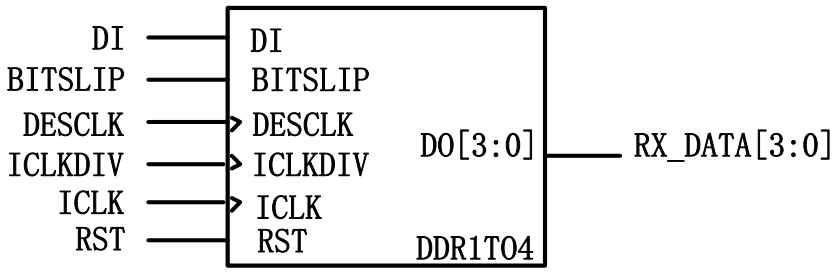


Figure 2-39 DDR1TO4 Functional Diagram

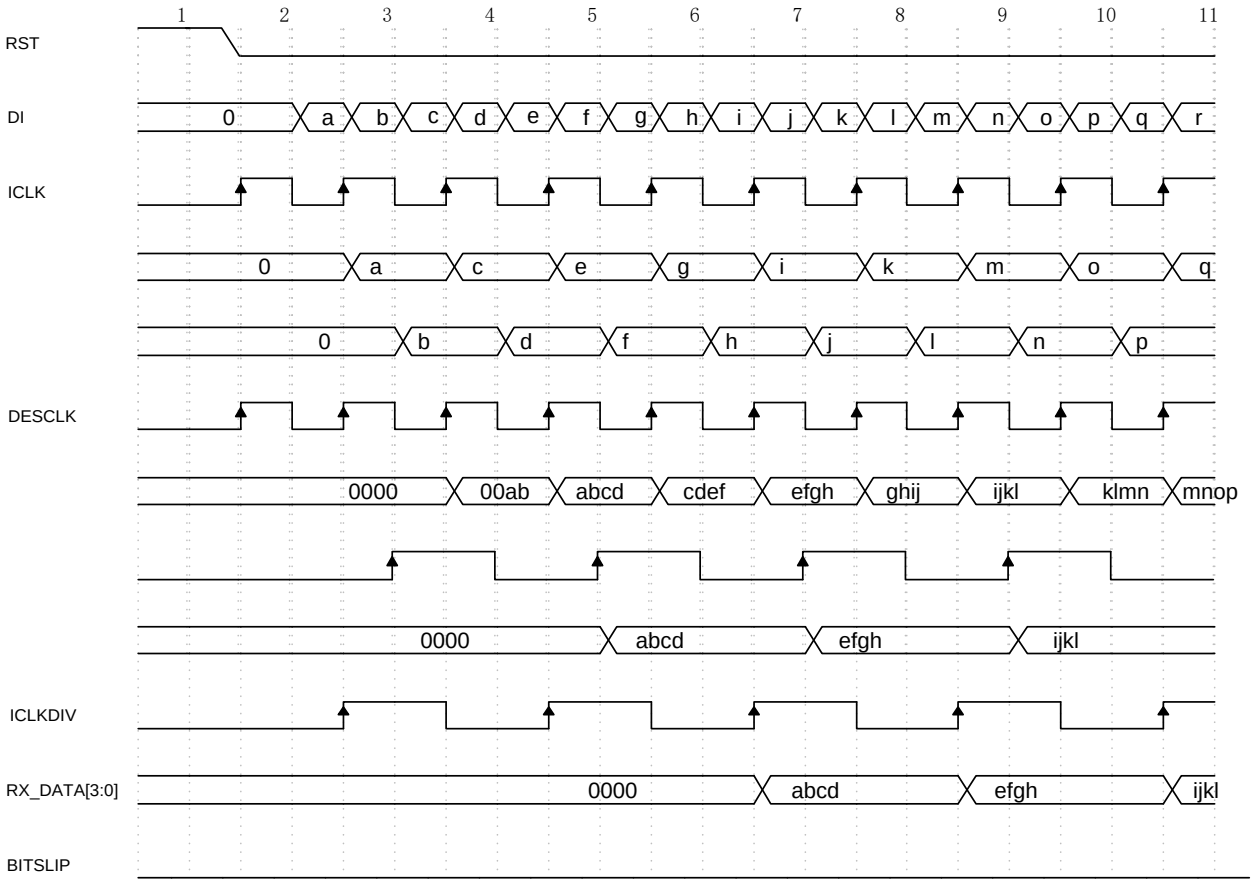


Figure 2-40 DDR1TO4 Timing Diagram

DDR1TO6

When the input logic is configured into DDR1TO6 mode, its functional diagram can be simplified as below.

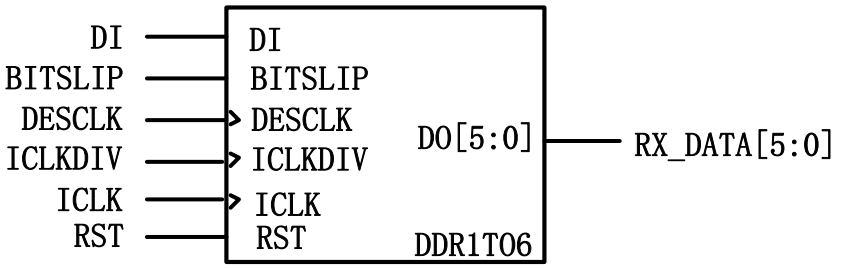


Figure 2-41 DDR1TO6 Functional Diagram

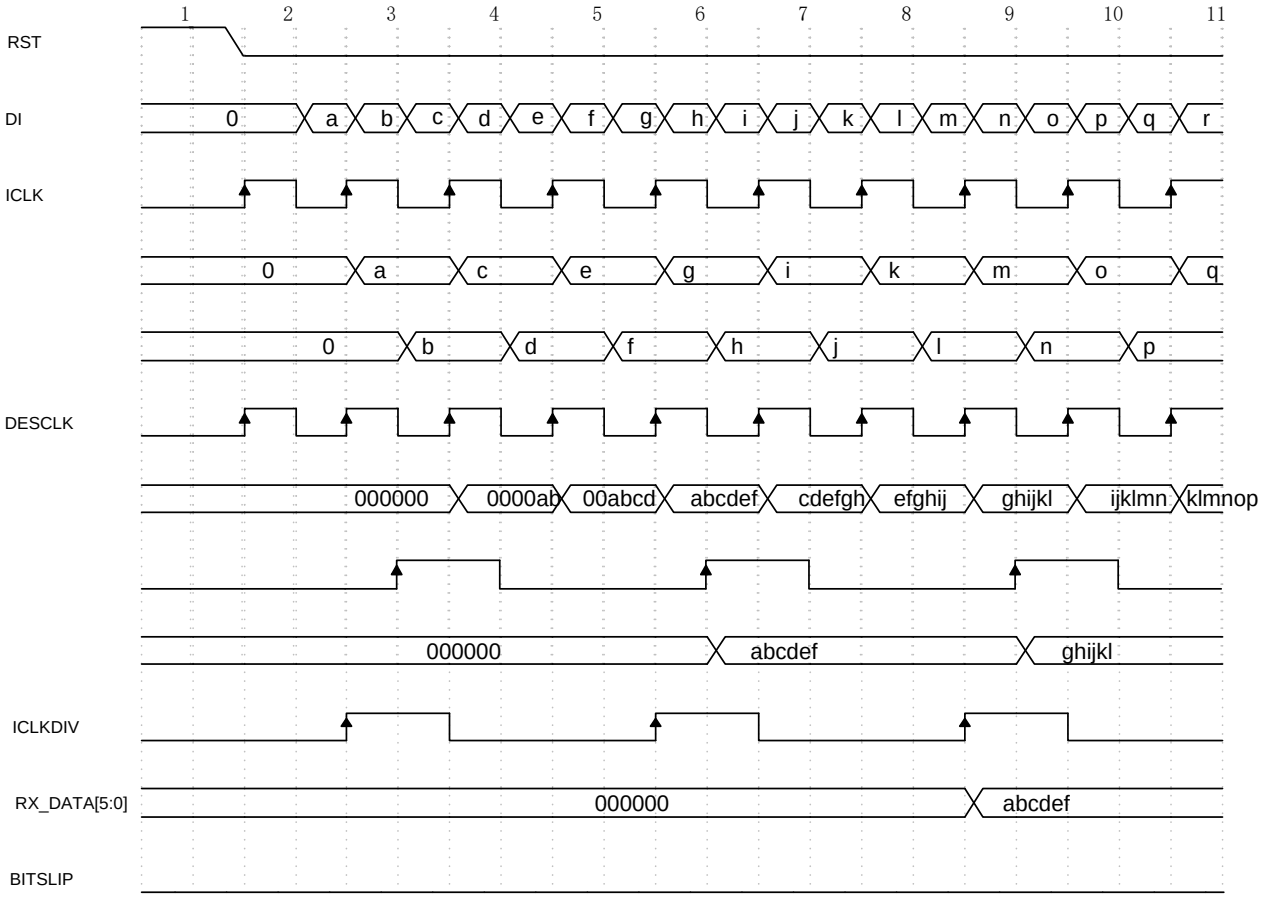


Figure 2-42 DDR1TO6 Timing Diagram

DDR1TO8

When the input logic is configured into DDR1TO8 mode, its functional diagram can be simplified as below.

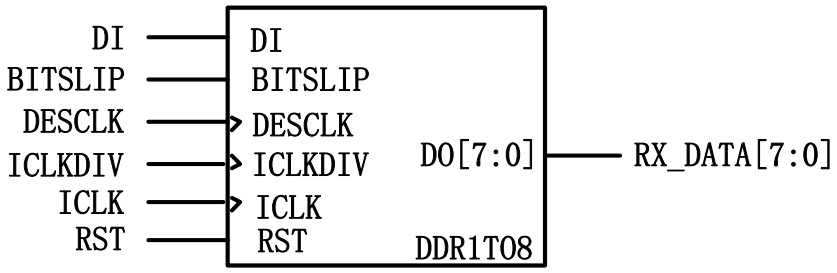


Figure 2-43 DDR1TO8 Functional Diagram

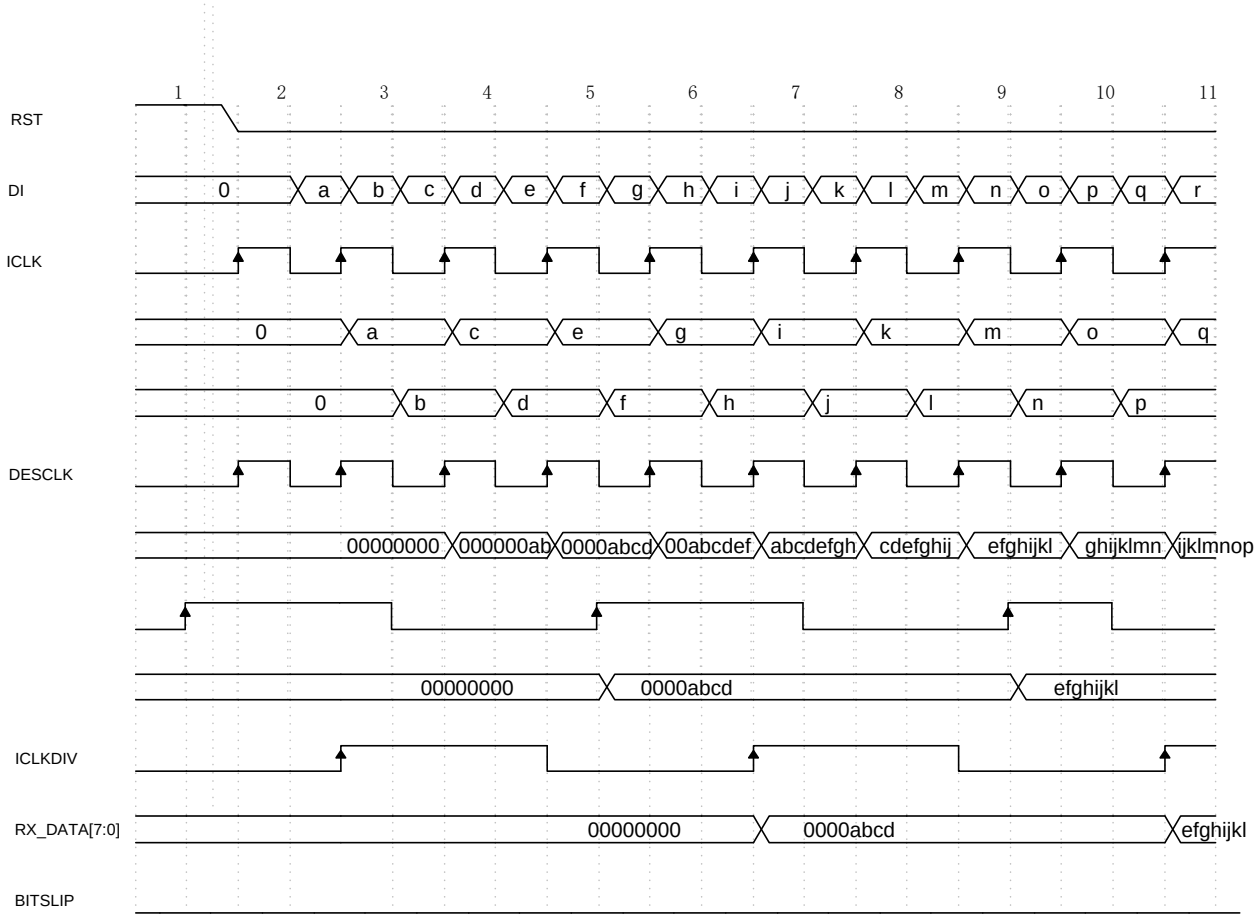


Figure 2-44 DDR1TO8 Timing Diagram

DDR1TO10

When the input logic is configured into DDR1TO10 mode, two GTPs need to be instantiated. Set the parameter CASCADE_MODE of GTP_ISERDES_INST0 to “MASTER”, and the parameter CASCADE_MODE of GTP_ISERDES_INST1 to “SLAVE”. The functional diagram can be simplified as below.

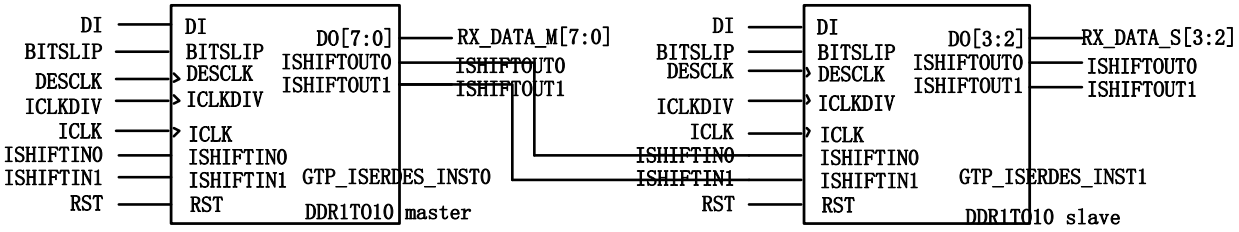


Figure 2-45 DDR1TO10 Functional Diagram

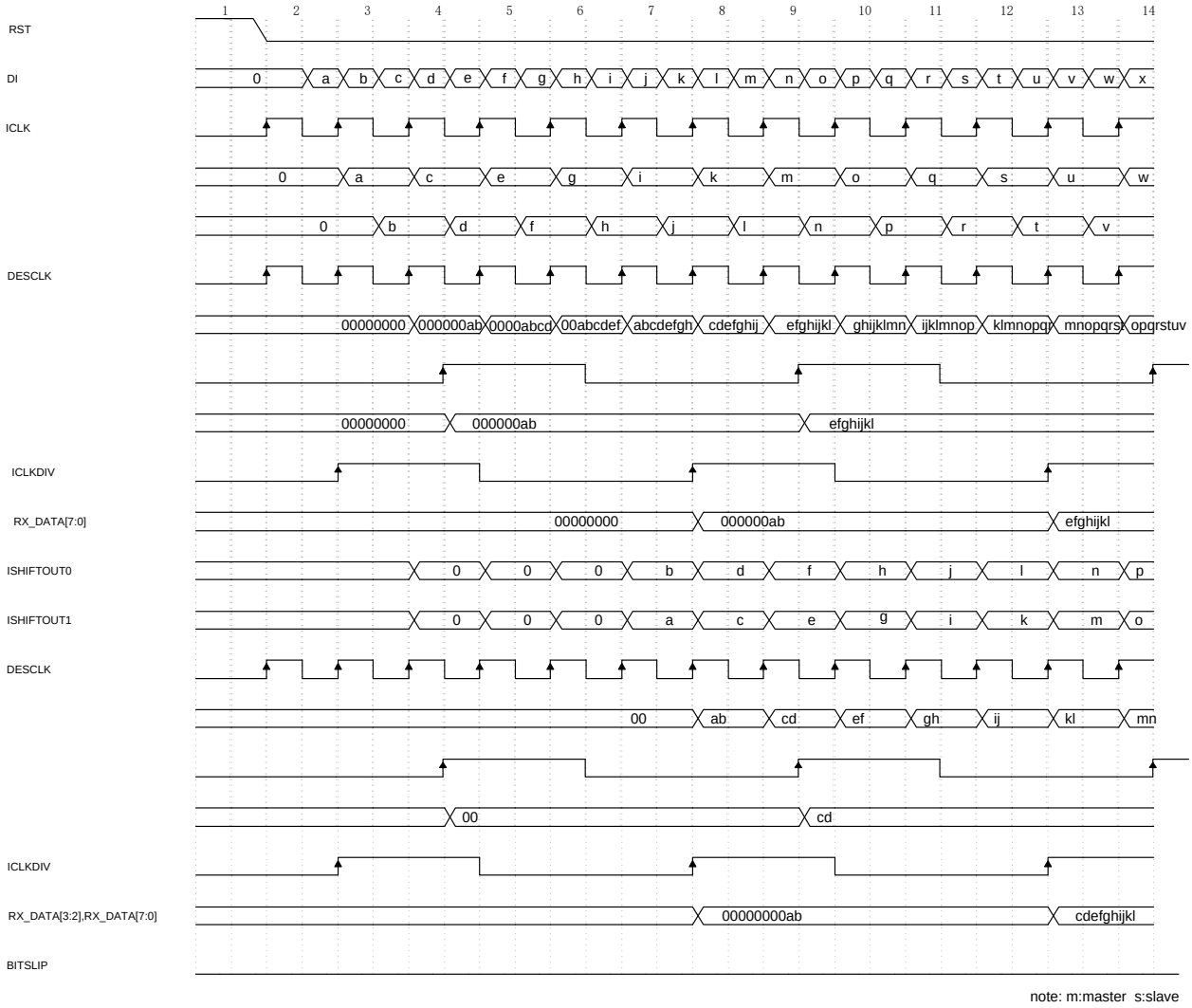


Figure 2-46 DDR1TO10 Timing Diagram

DDR1TO14

When the input logic is configured into DDR1TO14 mode, two GTPs need to be instantiated. Set the parameter CASCADE_MODE of GTP_ISERDES_INST0 to “MASTER” and the parameter CASCADE_MODE of GTP_ISERDES_INST1 to “SLAVE”. The functional diagram can be simplified as below.

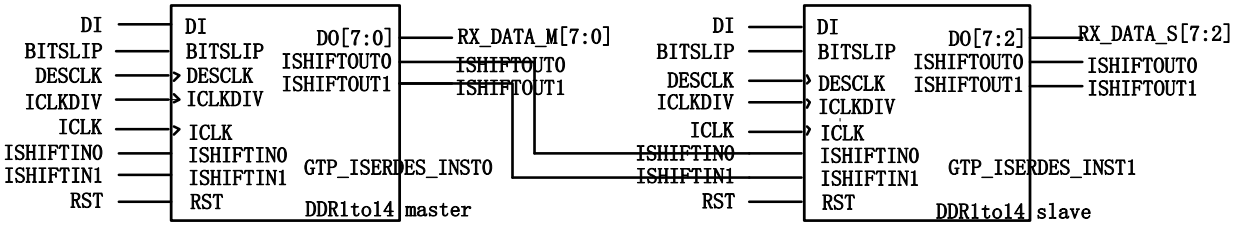


Figure 2-47 DDR1TO14 Functional Diagram

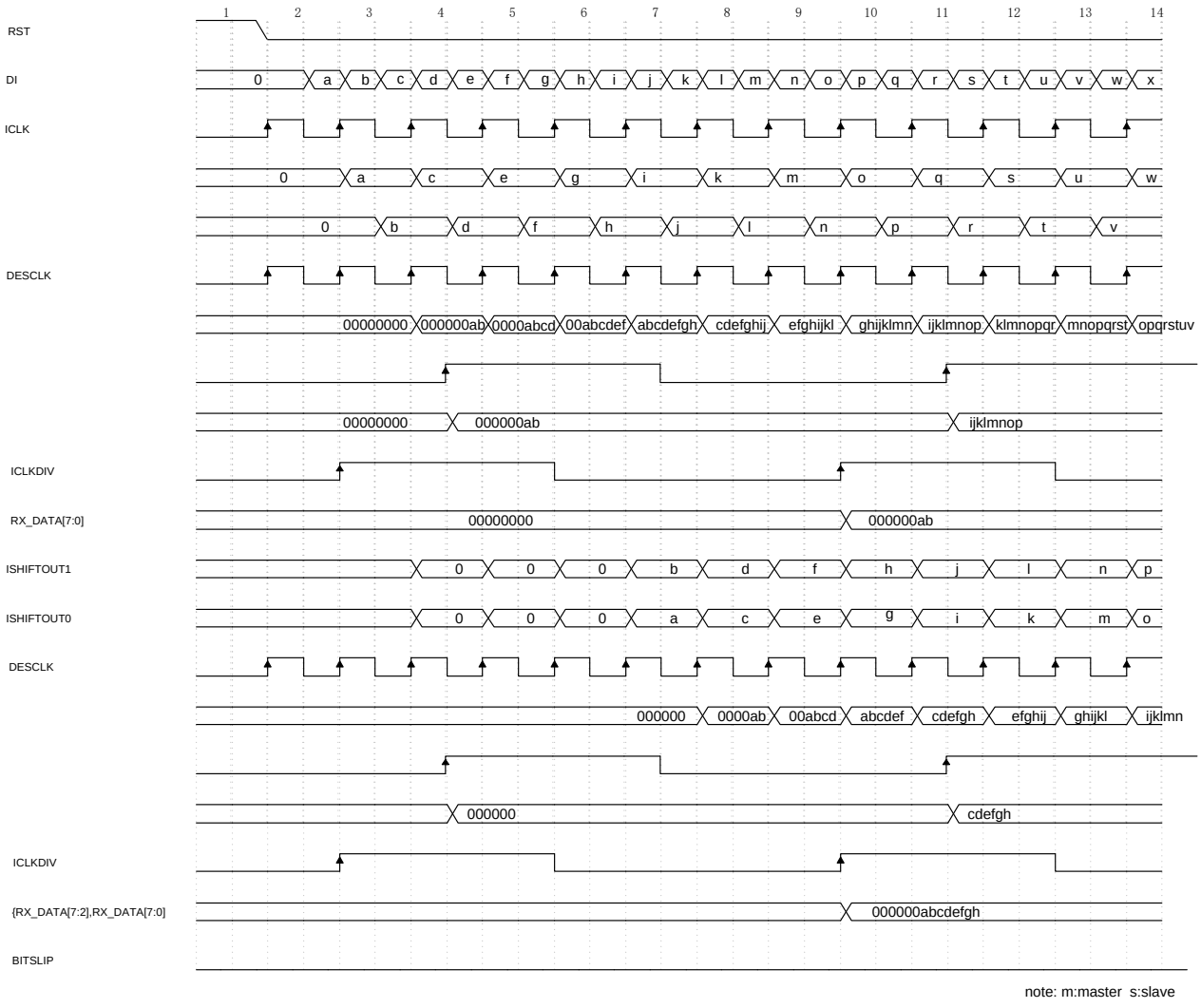


Figure 2-48 DDR1TO14 Timing Diagram

HMDDR1TO4

When the input logic is configured into HMDDR1TO4 mode, its functional diagram can be simplified as below.

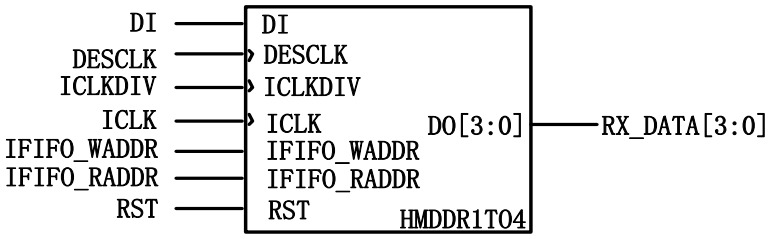


Figure 2-49 HMDDR1TO4 Functional Diagram

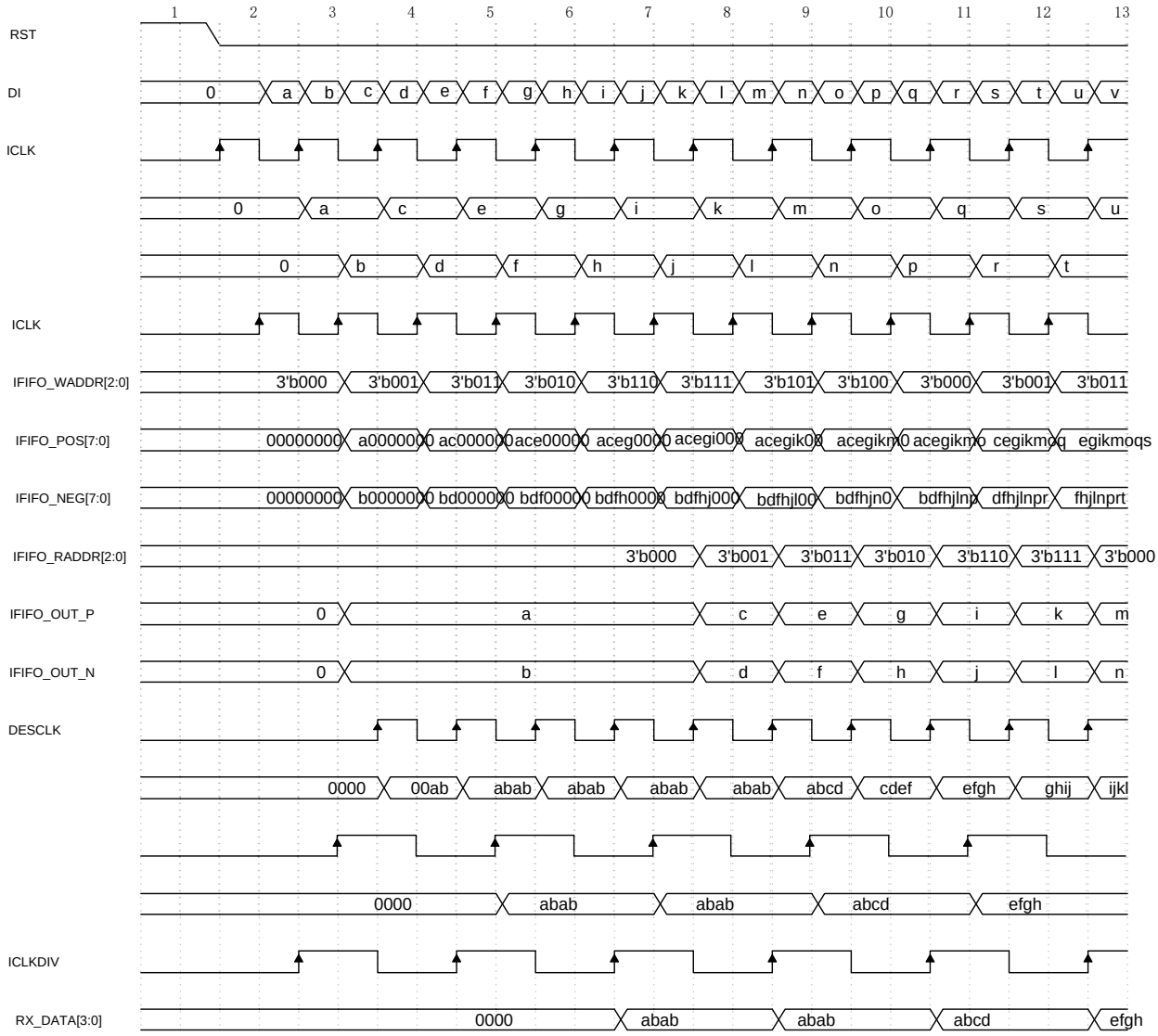


Figure 2-50 HMDDR1TO4 Timing Diagram

HMDDR1TO8

When the input logic is configured into HMDDR1TO8 mode, its functional diagram can be simplified as below.

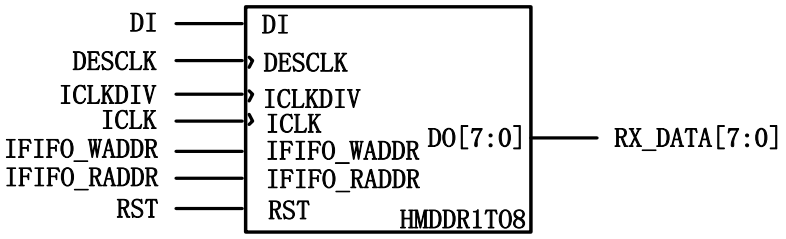


Figure 2-51 HMDDR1TO8 Functional Diagram

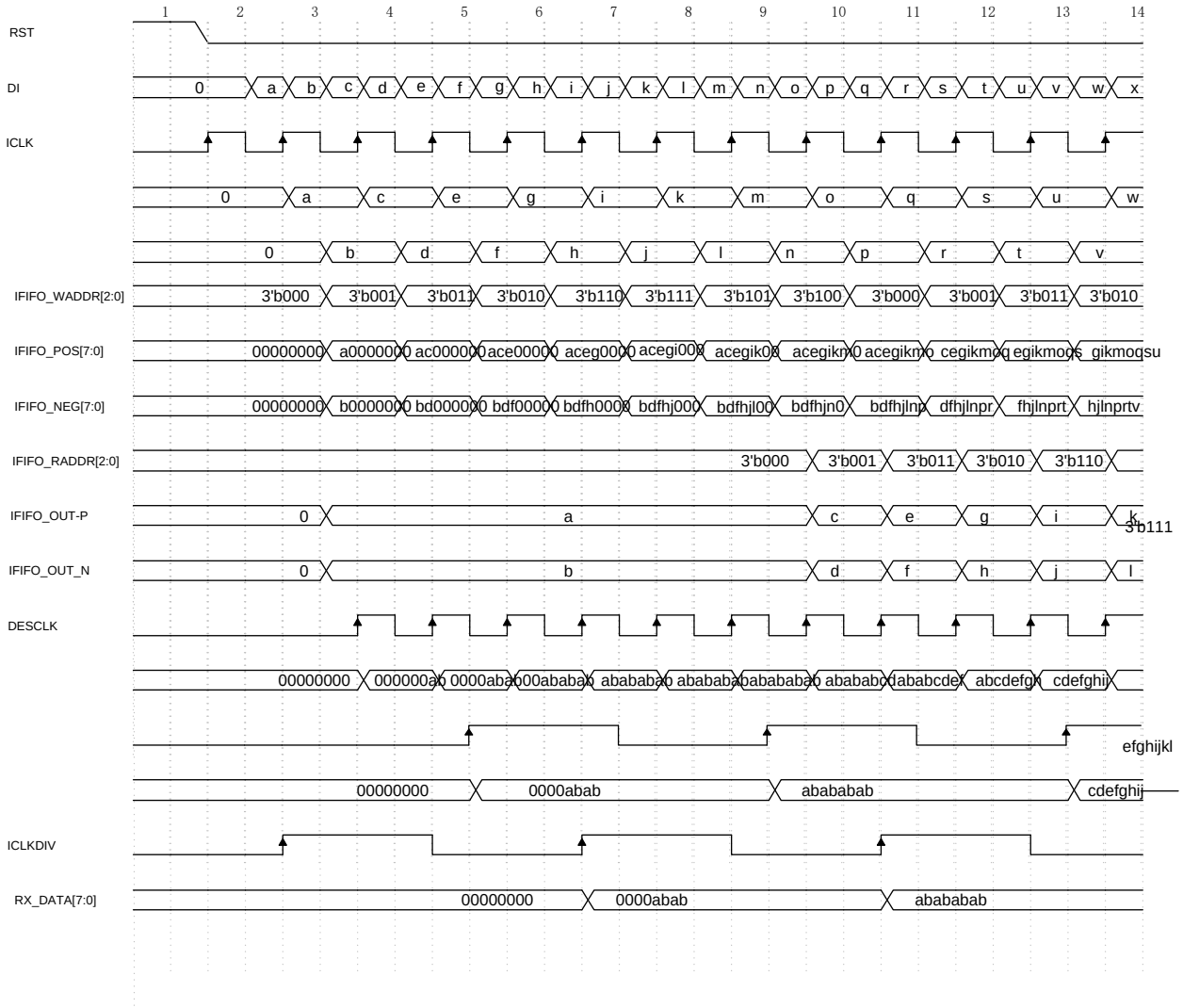


Figure 2-52 HMDDR1TO8 Timing Diagram

LMDDR1TO4

When the input logic is configured into LMDDR1TO4 mode, its functional diagram can be simplified as below.

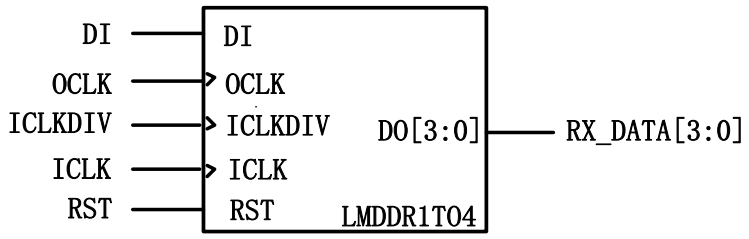


Figure 2-53 LMDDR1TO4 Functional Diagram

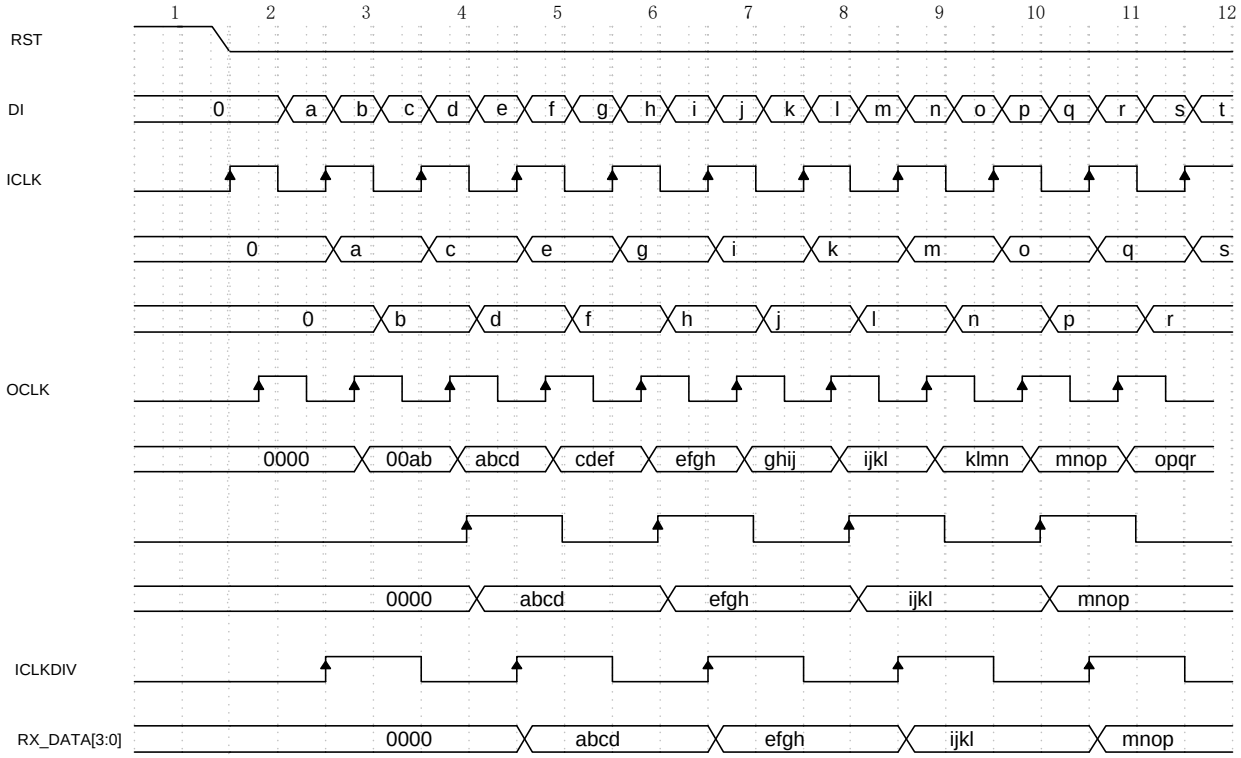


Figure 2-54 LMDDR1TO4 Timing Diagram

LMDDR1TO8

When the input logic is configured into LMDDR1TO4 mode, its functional diagram can be simplified as below.

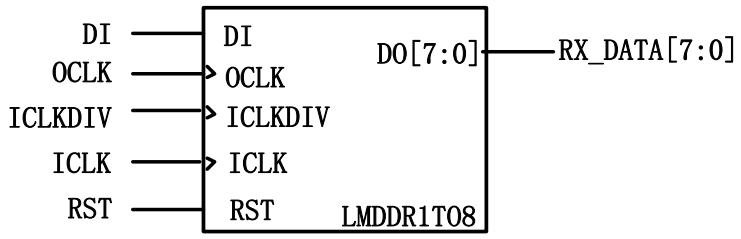


Figure 2-55 LMDDR1TO8 Functional Diagram

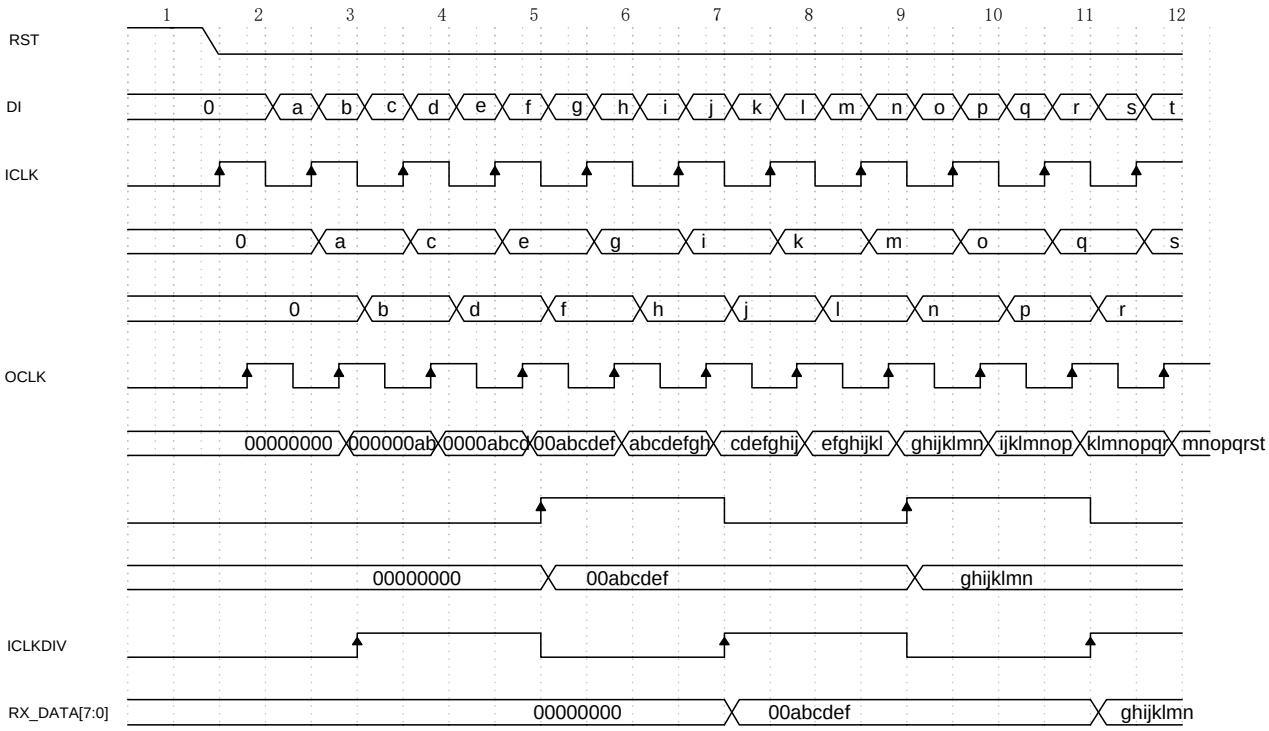


Figure 2-56 LMDDR1TO8 Timing Diagram

OVERSAMPLE

When the input logic is configured into OVERSAMPLE mode, its functional diagram can be simplified as below.

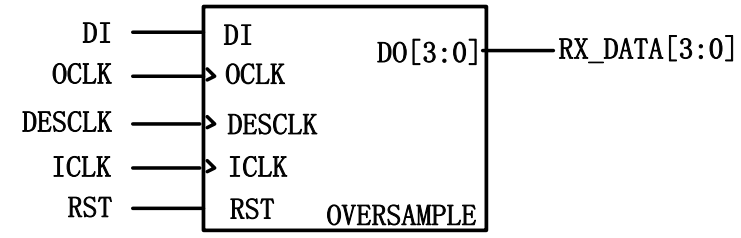


Figure 2-57 OVERSAMPLE Functional Diagram

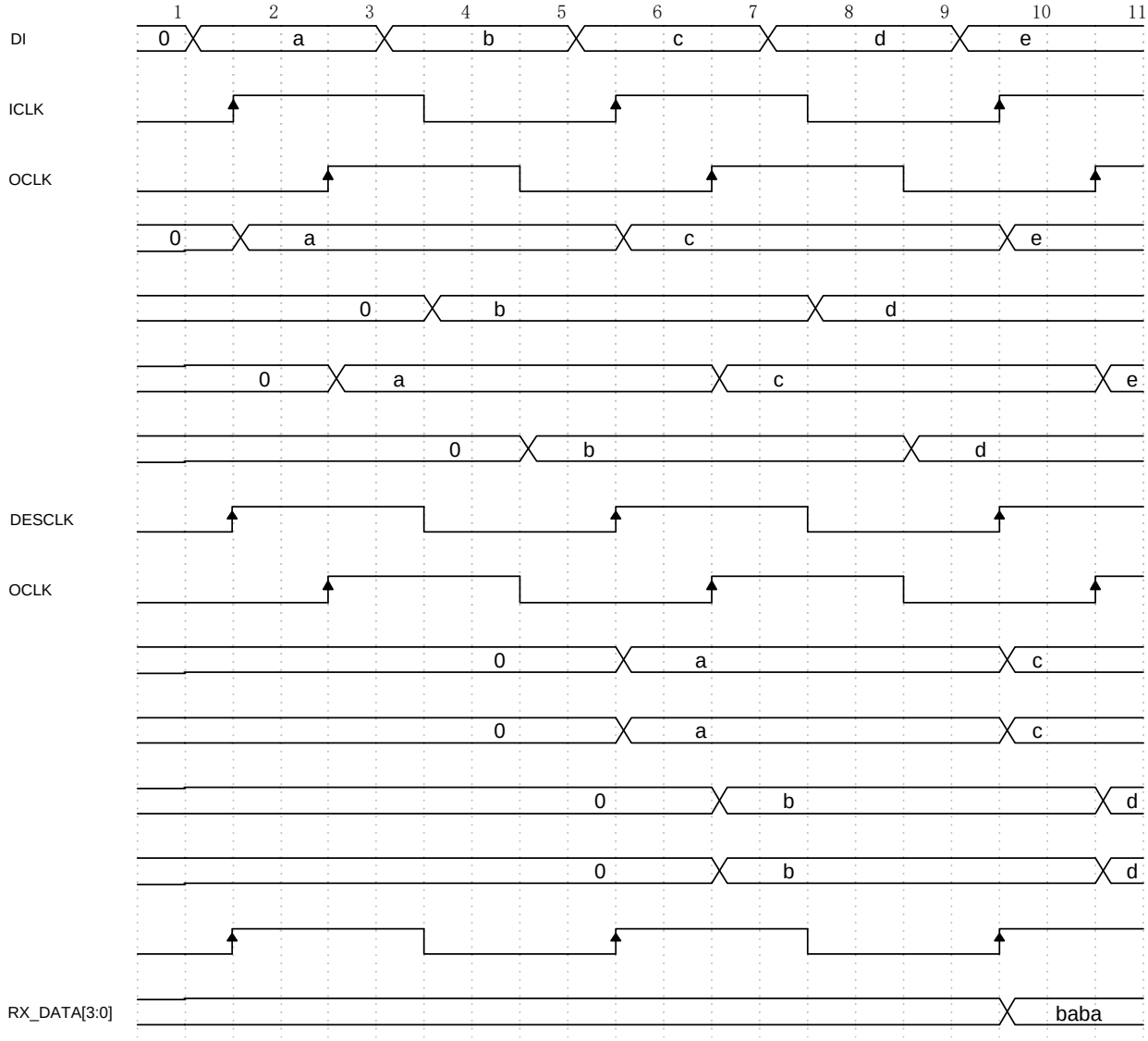


Figure 2-58 OVERSAMPLE Timing Diagram

As shown in the above figure, 4 clock signals with a phase difference of 90 degrees are used to sample the input data di. The sampled results, rx_data[3:0], are then sent to the internal for further processing.

2.3.3 Output Logic

The output logic of the IOL is used to process the transmitted high-speed data, converting high-speed parallel data into serial data. To achieve the parallel-to-serial conversion in IOL, PDS provides the GTP_OSERDES_E2 primitive. The GTP_OSERDES_E2 data output conversion module supports rate conversions for ODFF, OLATCH, SDR2TO1, SDR3TO1, SDR4TO1, SDR5TO1, SDR6TO1, SDR7TO1, SDR8TO1, DDR2TO1_SAME_EDGE, DDR2TO1_OPPOSITE_EDGE, DDR4TO1, DDR6TO1, DDR8TO1, DDR10TO1, DDR14TO1, HMSDR4TO1, and HMSDR8TO1 modes. The structure block diagram is shown below:

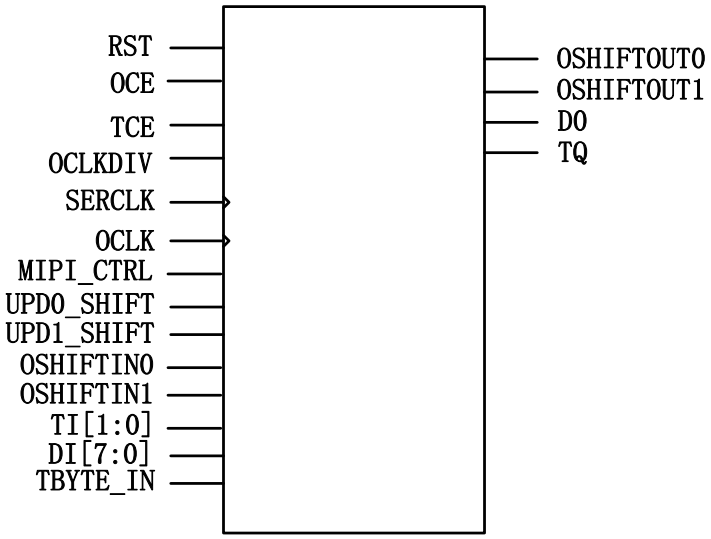


Figure 2-59 GTP_OSERDES_E2 Structure Diagram

The Verilog instantiation of GTP_OSERDES_E2 is shown as follows:

```
    GTP_OSERDES_E2 #
(
    .GRS_EN (“TRUE”),
    . OSERDES_MODE (“SDR4TO1”)
    . TSERDES_EN (“FALSE”),
    . UPD0_SHIFT_EN (“FALSE”),
    . UPD1_SHIFT_EN (“FALSE”),
    . INIT_SET (2’b00),
    . GRS_TYPE_DQ (“RESET”),
    . LRS_TYPE_DQ0 (“ASYNC_RESET”),
    . LRS_TYPE_DQ1 (“ASYNC_RESET”),
    . LRS_TYPE_DQ2 (“ASYNC_RESET”),
```

```
    . LRS_TYPE_DQ3 (“ASYNC_RESET”),
    . GRS_TYPE_TQ (“RESET”),
    . LRS_TYPE_TQ0 (“ASYNC_RESET”),
    . LRS_TYPE_TQ1 (“ASYNC_RESET”),
    . LRS_TYPE_TQ2 (“ASYNC_RESET”),
    . LRS_TYPE_TQ3 (“ASYNC_RESET”),
    . TRI_EN (“FALSE”),
    . TBYTE_EN (“FALSE”),
    . MIPI _EN (“FALSE”),
    . OCASCADE_EN (“FALSE”)
) GTP_OSERDES_E2_INST (
    . RST (RST),
    . OCE (OCE),
    . TCE (TCE),
    . OCLKDIV (OCLKDIV),
    . SERCLK (SERCLK),
    . OCLK (OCLK),
    . MIPI_CTRL (MIPI_CTRL),
    . UPD0_SHIFT (UPD0_SHIFT),
    . UPD1_SHIFT (UPD1_SHIFT),
    . OSHIFTIN0 (OSHIFTIN0),
    . OSHIFTIN1 (OSHIFTIN1),
    . DI (DI),
    . TI (TI),
    . TBYTE_IN (TBYTE_IN),
    . OSHIFTOUT0 (OSHIFTOUT0),
    . OSHIFTOUT1 (OSHIFTOUT1),
    . DO (DO),
    . TQ (TQ)
);
```

It is worth noting that GTP_OSERDES_E2 is only used for the OSERDES mode, and the parameter TSERDES_EN of GTP_OSERDES_E2 needs to be set to “FALSE”.

When using OSERDES in conjunction with TSERDES, GTP_OSERDES_E2 needs to be instantiated twice. Set the parameter TSERDES_EN of one GTP_OSERDES_E2 to “FALSE” as

OSERDES, and set the parameter TSERDES_EN of the other GTP_OSERDES_E2 to “TRUE” as TSERDES. TSERDES is used to generate tri-state control signals to process data signals generated by OSERDES.

For high-speed output applications, when OSERDES is SDR 2TO1, TSERDES is SDR 2TO1; when OSERDES is SDR 4TO1, TSERDES is SDR 4TO1; when OSERDES is SDR 8TO1, TSERDES is SDR 8TO1; when OSERDES is DDR 4TO1, TSERDES is DDR 4TO1; and when OSERDES is DDR 8TO1, TSERDES is DDR 8TO1. For MEMORY applications, when OSERDES is SDR 4TO1, TSERDES is SDR 4TO1; when OSERDES is SDR 8TO1, TSERDES is SDR 8TO1. Other modes do not support the use of OSERDES in conjunction with TSERDES.

GTP_OSERDES_E2 cannot be configured as TSERDES alone.

GTP_OSERDES_E2 is usually used in conjunction with GTP_OUTBUF, GTP_OUTBUFDS, GTP_OUTBUFCO, GTP_OUTBUFTCO, GTP_OUTBUFTDS, and GTP_OUTBUFT.

Table 2-48 GTP_OSERDES_E2 Parameter Descriptions

Parameter Name	**Type**	**Valid Values**	**Defaults**	**Description**
OSERDES_MODE	String	“SDR2TO1” “SDR3TO1” “SDR4TO1” “SDR5TO1” “SDR6TO1” “SDR7TO1” “SDR8TO1” “OLATCH” “ODFF” “DDR2TO1_SAME_EDGE” “DDR2TO1_OPPOSITE_EDGE” “DDR4TO1” “DDR6TO1” “DDR8TO1” “DDR10TO1” “DDR14TO1” “HMSDR4TO1” “HMSDR8TO1”	SDR4TO1	“SDR2TO1”: Generic SDR 2:1 “SDR3TO1”: Generic SDR 3:1 “SDR4TO1”: Generic SDR 4:1 “SDR5TO1”: Generic SDR 5:1 “SDR6TO1”: Generic SDR 6:1 “SDR7TO1”: Generic SDR 7:1 “SDR8TO1”: Generic SDR 8:1 “OLATCH”: Latch output mode “ODFF” Register output mode “DDR2TO1_OPPOSITE_EDGE”: Generic DDR 2:1 “DDR2TO1_SAME_EDGE”: Generic DDR 2:1 “DDR4TO1”: Generic DDR 4:1 “DDR6TO1”: Generic DDR 6:1 “DDR8TO1”: Generic DDR 8:1 “DDR10TO1”: Generic DDR 10:1 “DDR14TO1”: Generic DDR 14:1 “HMSDR4TO1”: High-Speed Memory DDR 4:1 “HMSDR8TO1”: High-Speed Memory DDR 8:1
TSERDES_EN	String	“TRUE” “FALSE”	“FALSE”	*Note: When OSERDES is used in conjunction with TSERDES: TSERDES_EN of OSERDES = “FALSE”, TSERDES_EN of TSERDES = “TRUE”
GRS_EN	String	“TRUE” “FALSE”	“TRUE”	Global reset/set enabled
UPD0_SHIFT_EN	String	“FALSE” “TRUE”	“FALSE”	Position control for upd0 in OLOGIC enabled
UPD1_SHIFT_EN	String	“FALSE” “TRUE”	“FALSE”	Position control for upd1 in OLOGIC enabled

Parameter Name	Type	Valid Values	Defaults	Description
INIT_SET [1:0]	Constance	2'b00, 2'b01, 2'b10, 2'b11	2'b00	Static position control for upd0 and upd1 in OLOGIC 2'b00: Default position 2'b01: Move forward by one cycle 2'b10: Move forward by two cycles 2'b11: Move forward by three cycles
GRS_TYPE_DQ	String	"RESET" "SET"	"RESET"	Global reset results of DFF0, DFF1, DFF2, DFF3, and DFF4 in OLOGIC data gear;
LRS_TYPE_DQ0	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set results of DFF0 and DFF4 in OLOGIC data gear;
LRS_TYPE_DQ1	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF1 in OLOGIC data gear;
LRS_TYPE_DQ2	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF2 in OLOGIC data gear;
LRS_TYPE_DQ3	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF3 in OLOGIC data gear;
GRS_TYPE_TQ	String	"RESET" "SET"	"RESET"	Global reset results of DFF0, DFF1, DFF2, DFF3, and DFF4 in OLOGIC tri-state gear;
LRS_TYPE_TQ0	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF0 in OLOGIC tri-state gear;
LRS_TYPE_TQ1	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF1 in OLOGIC tri-state gear;
LRS_TYPE_TQ2	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF2 in OLOGIC tri-state gear;
LRS_TYPE_TQ3	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF3 in OLOGIC tri-state gear;
TRI_EN	String	"FALSE" "TRUE"	"FALSE"	Tri-state control enabled
TBYTE_EN	String	"FALSE" "TRUE"	"FALSE"	BYTE control enabled
MIPI _EN	String	"FALSE" "TRUE"	"FALSE"	MIPI applications not supported, and should be set to "FALSE"
OCASCADE_EN	String	"FALSE" "TRUE"	"FALSE"	OSERDES extension enabled

Table 2-49 GTP_OSERDES_E2 Port Descriptions

Port	Direction	Width	Description
RST	Input	1	Local reset signal
OCE	Input	1	Clock enable signal of output module
TCE	Input	1	Clock enable signal of tri-state module
OCLKDIV	Input	1	OLOGIC low-speed clock
SERCLK	Input	1	OLOGIC serialisation clock
OCLK	Input	1	OLOGIC output stage high-speed clock
MIPI_CTRL	Input	1	This port is reserved.
UPD0_SHIFT	Input	1	OLOGIC UPD0 position shift
UPD1_SHIFT	Input	1	OLOGIC UPD1 position shift
OSHIFTIN0	Input	1	Cascade input signal
OSHIFTIN1	Input	1	Cascade input signal
DI	Input	8	Parallel input data signals
TI	Input	2	Parallel input tri-state control signal
TBYTE_IN	Input	1	Tri-state control input signal for one byte
OSHIFTOUT0	Output	1	Cascade output signals
OSHIFTOUT1	Output	1	Cascade output signals
DO	Output	1	Data output, low bits first
TQ	Output	1	Tri-State Control Output

2.3.3.1 Direct Output

The following describes the register output mode and latch output mode, where the output logic configured into direct output mode.

ODFF

When the output logic is configured into ODFF mode, its functional diagram can be simplified as below.

Figure 2-60 ODFF Functional Diagram

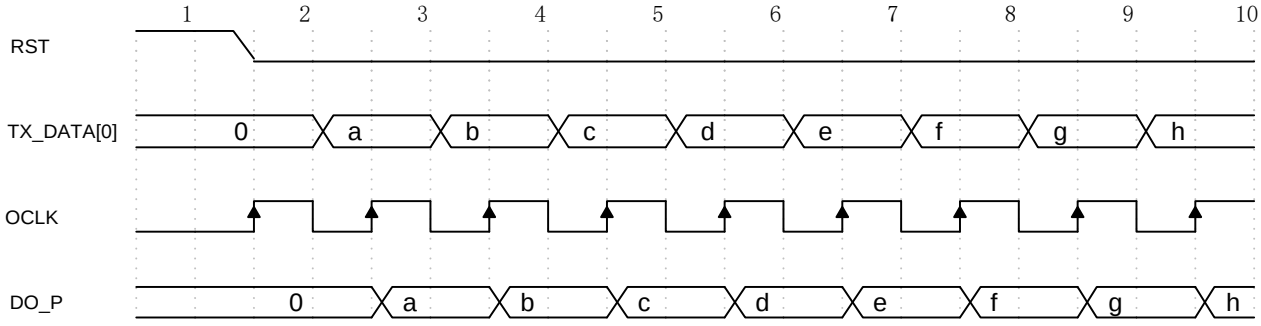


Figure 2-61 ODFF Timing Diagram

OLATCH

When the output logic is configured into OLATCH mode, its functional diagram can be simplified as below.

Figure 2-62 OLATCH Functional Diagram

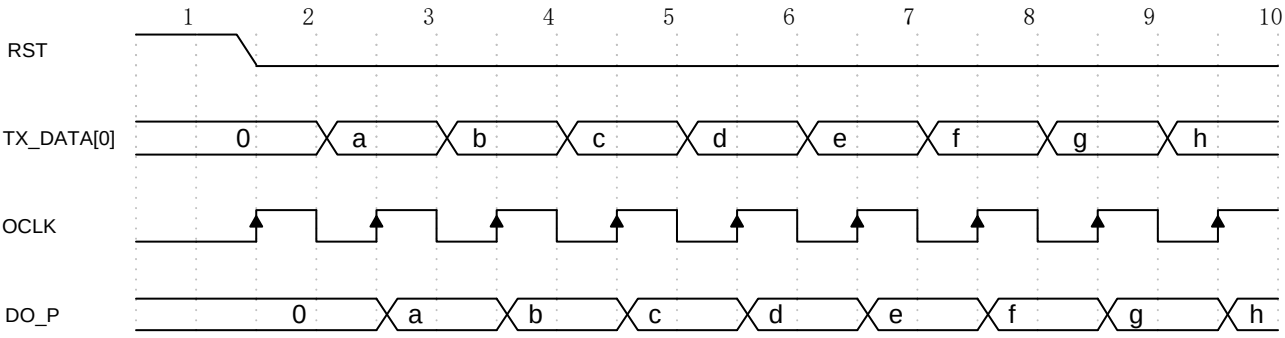


Figure 2-63 OLATCH Timing Diagram

2.3.3.2 OSERDES

The following describes the different operating modes in which the output logic is configured as OSERDES.

SDR2TO1

When the input logic is configured into SDR2TO1 mode, its functional diagram can be simplified as below.

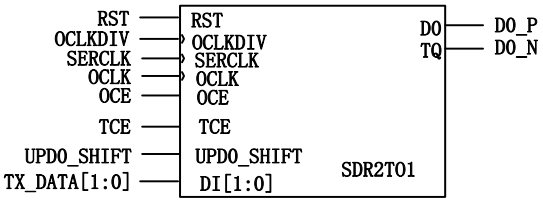


Figure 2-64 SDR2TO1 Functional Diagram

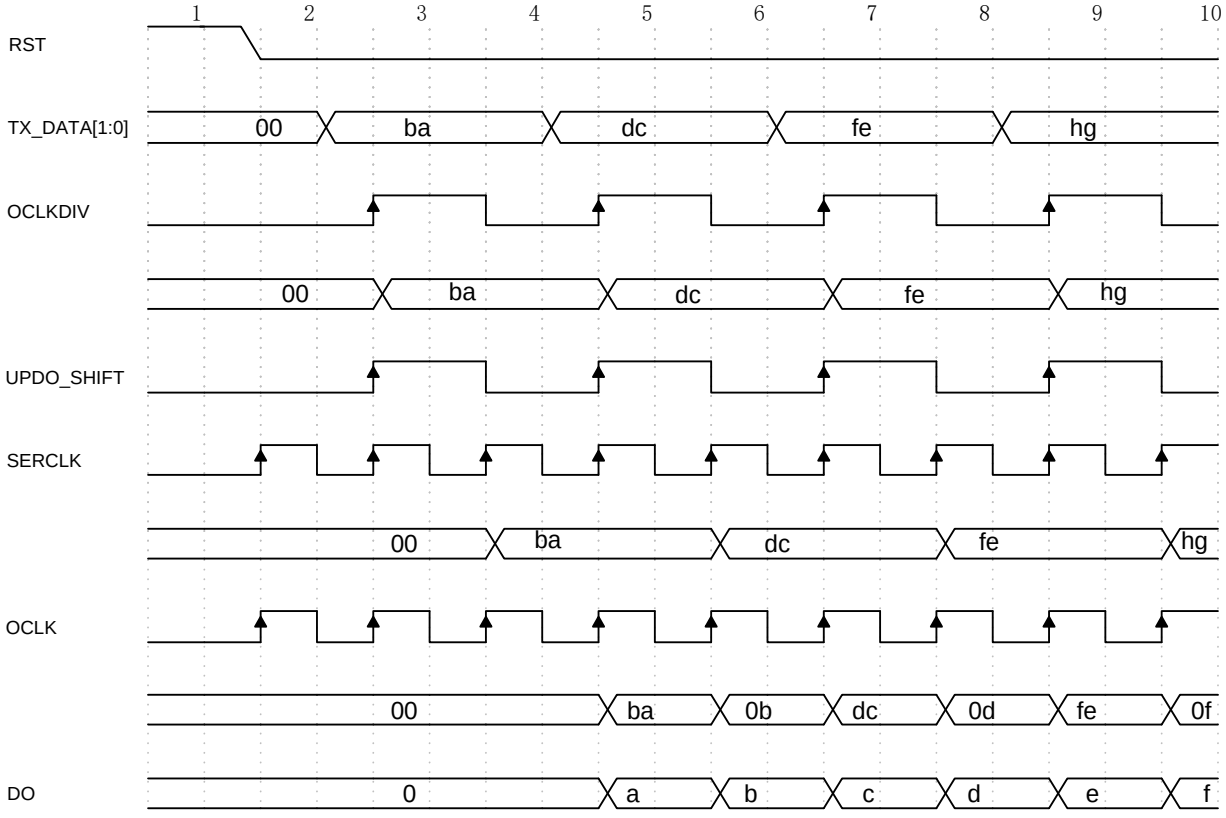


Figure 2-65 SDR2TO1 Timing Diagram

SDR3TO1

When the output logic is configured into SDR3TO1 mode, its functional diagram can be simplified as below.

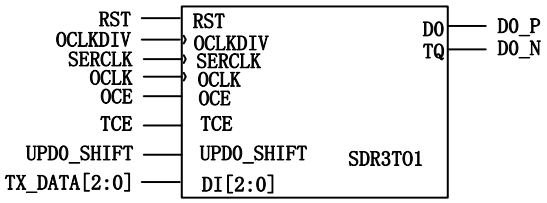


Figure 2-66 SDR3TO1 Functional Diagram

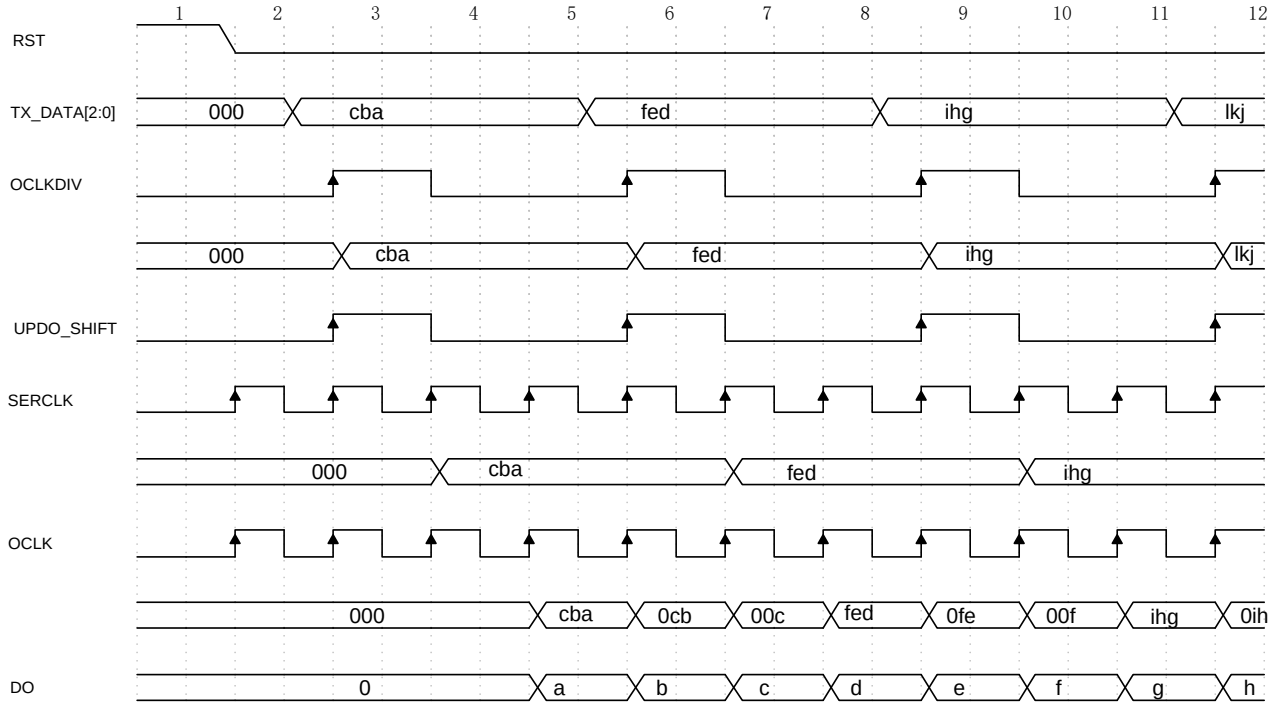


Figure 2-67 SDR3TO1 Timing Diagram

SDR4TO1

When the output logic is configured into SDR4TO1 mode, its functional diagram can be simplified as below.

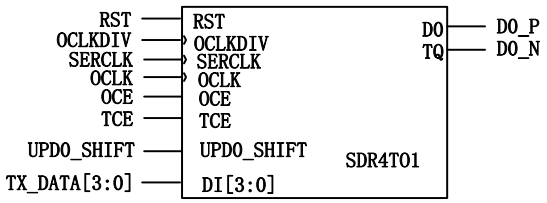


Figure 2-68 SDR4TO1 Functional Diagram

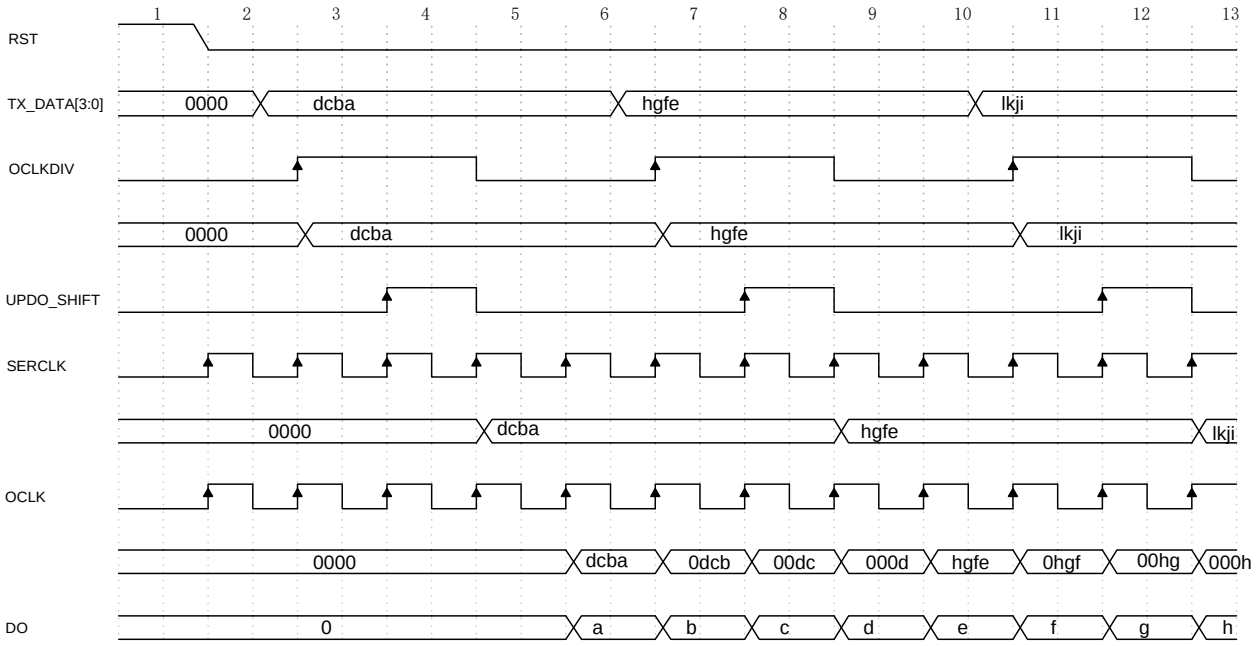


Figure 2-69 SDR4TO1 Timing Diagram

SDR5TO1

When the output logic is configured into SDR5TO1 mode, its functional diagram can be simplified as below.

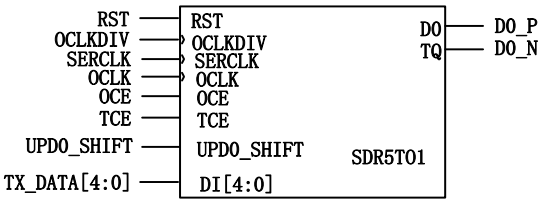


Figure 2-70 SDR5TO1 Functional Diagram

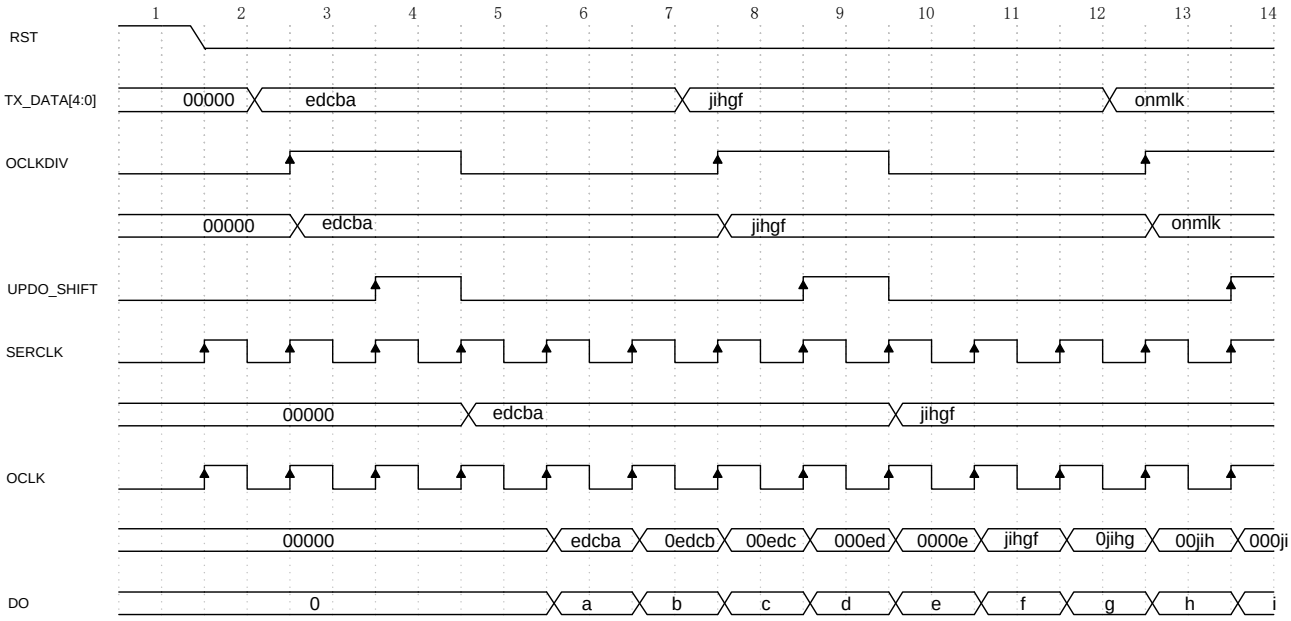


Figure 2-71 SDR5TO1 Timing Diagram

SDR6TO1

When the output logic is configured into SDR6TO1 mode, its functional diagram can be simplified as below.

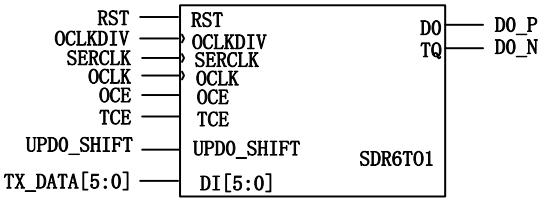


Figure 2-72 SDR6TO1 Functional Diagram

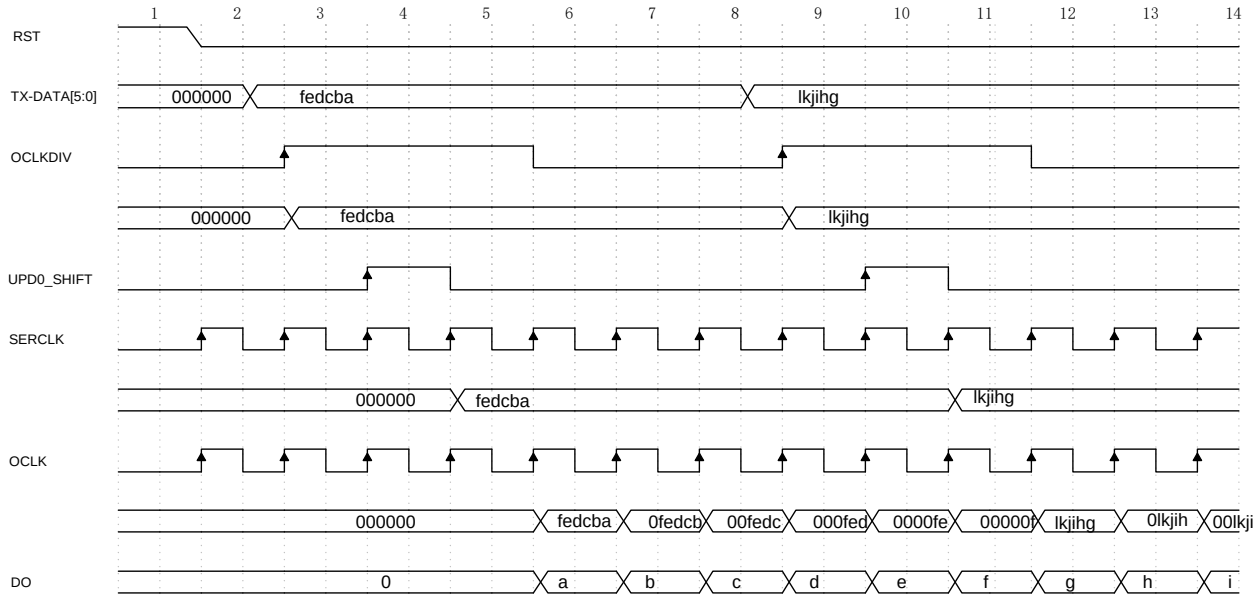


Figure 2-73 SDR6TO1 Timing Diagram

SDR7TO1

When the output logic is configured into SDR7TO1 mode, its functional diagram can be simplified as below.

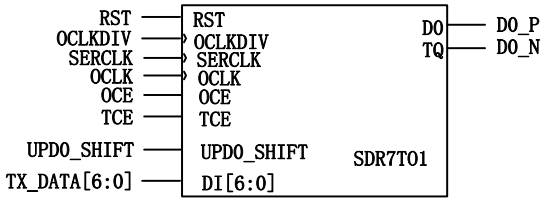


Figure 2-74 SDR7TO1 Functional Diagram

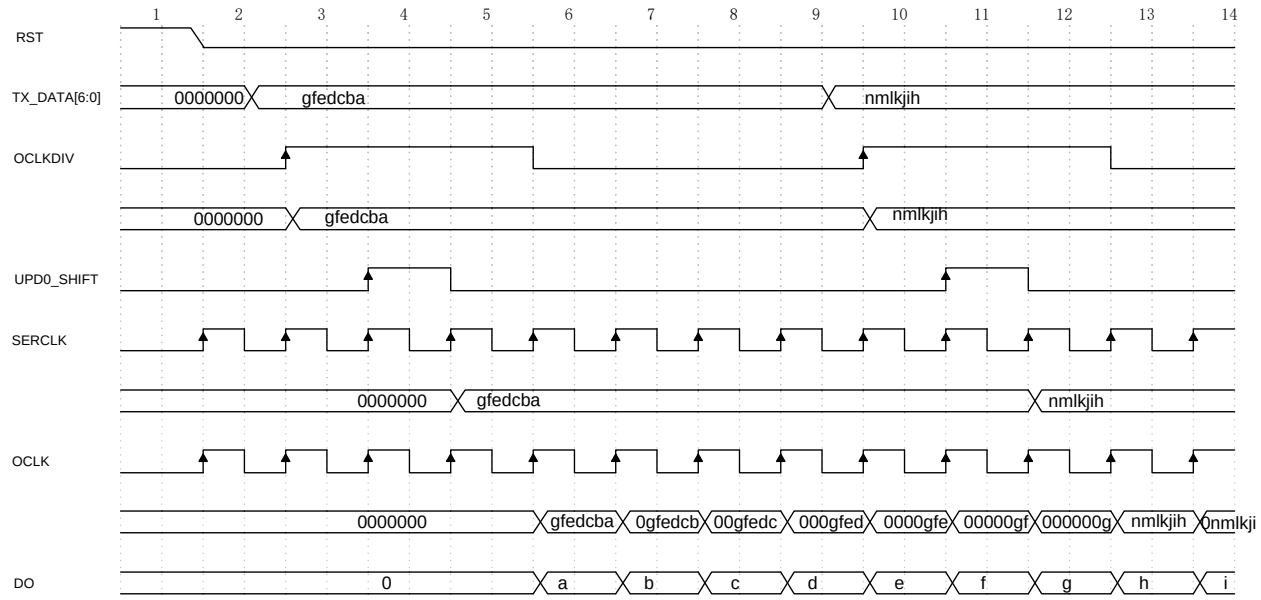


Figure 2-75 SDR7TO1 Timing Diagram

SDR8TO1

When the output logic is configured into SDR8TO1 mode, its functional diagram can be simplified as below.

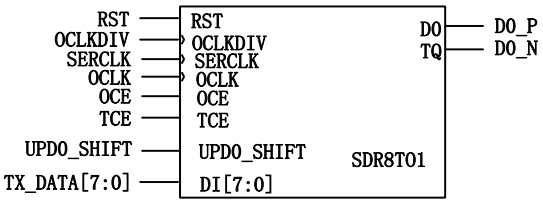


Figure 2-76 SDR8TO1 Functional Diagram

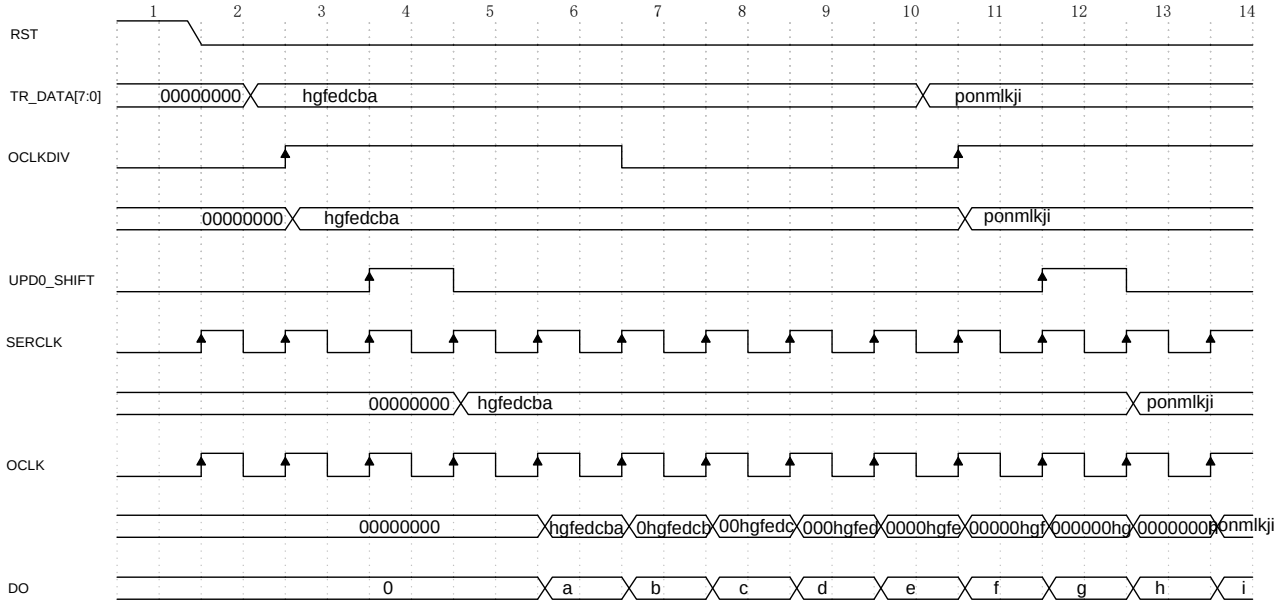


Figure 2-77 SDR8TO1 Timing Diagram

DDR2TO1_OPPOSITE_EDGE

When the output logic is configured into DDR2TO1_OPPOSITE_EDGE mode, its functional diagram can be simplified as below.

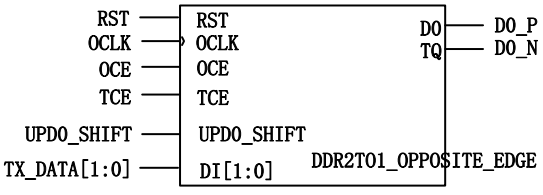


Figure 2-78 DDR2TO1_OPPOSITE_EDGE Functional Diagram

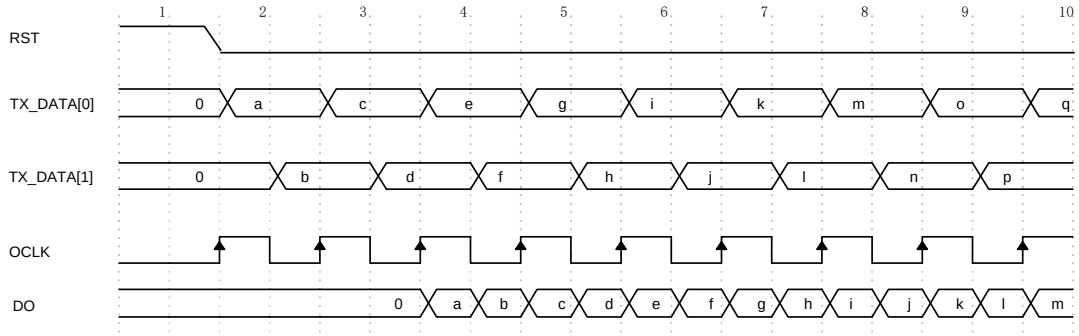


Figure 2-79 DDR2TO1_OPPOSITE_EDGE Timing Diagram

DDR2TO1_SAME_EDGE

When the output logic is configured into DDR2TO1_SAME_EDGE mode, its functional diagram can be simplified as below.

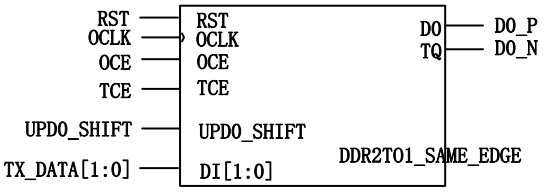


Figure 2-80 DDR2TO1_SAME_EDGE Functional Diagram

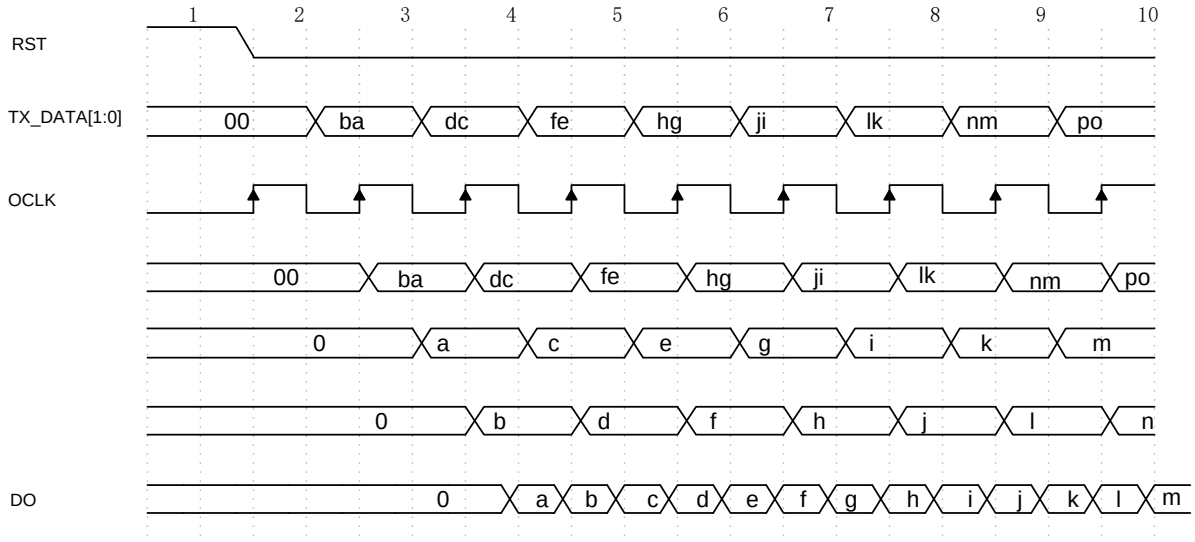


Figure 2-81 DDR2TO1_SAME_EDGE Timing Diagram

DDR4TO1

When the output logic is configured into DDR4TO1 mode, its functional diagram can be simplified as below.

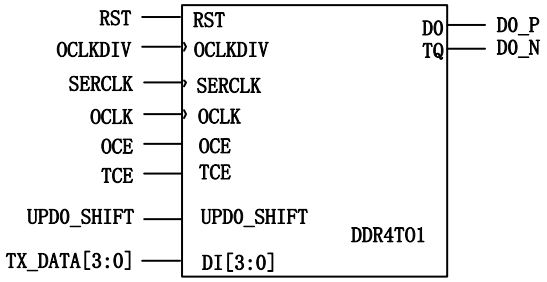


Figure 2-82 DDR4TO1 Functional Diagram

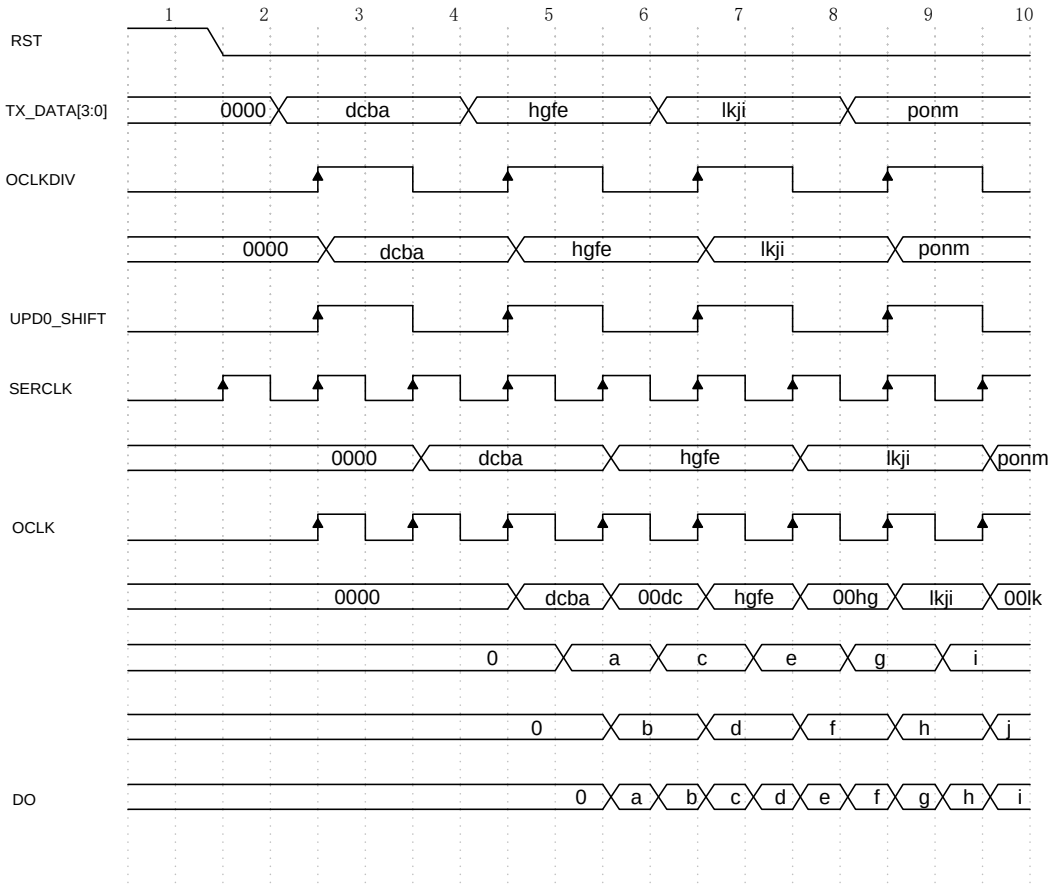


Figure 2-83 DDR4TO1 Timing Diagram

DDR6TO1

When the output logic is configured into DDR6TO1 mode, its functional diagram can be simplified as below.

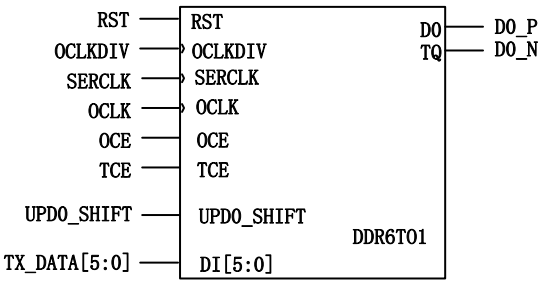


Figure 2-84 DDR6TO1 Functional Diagram

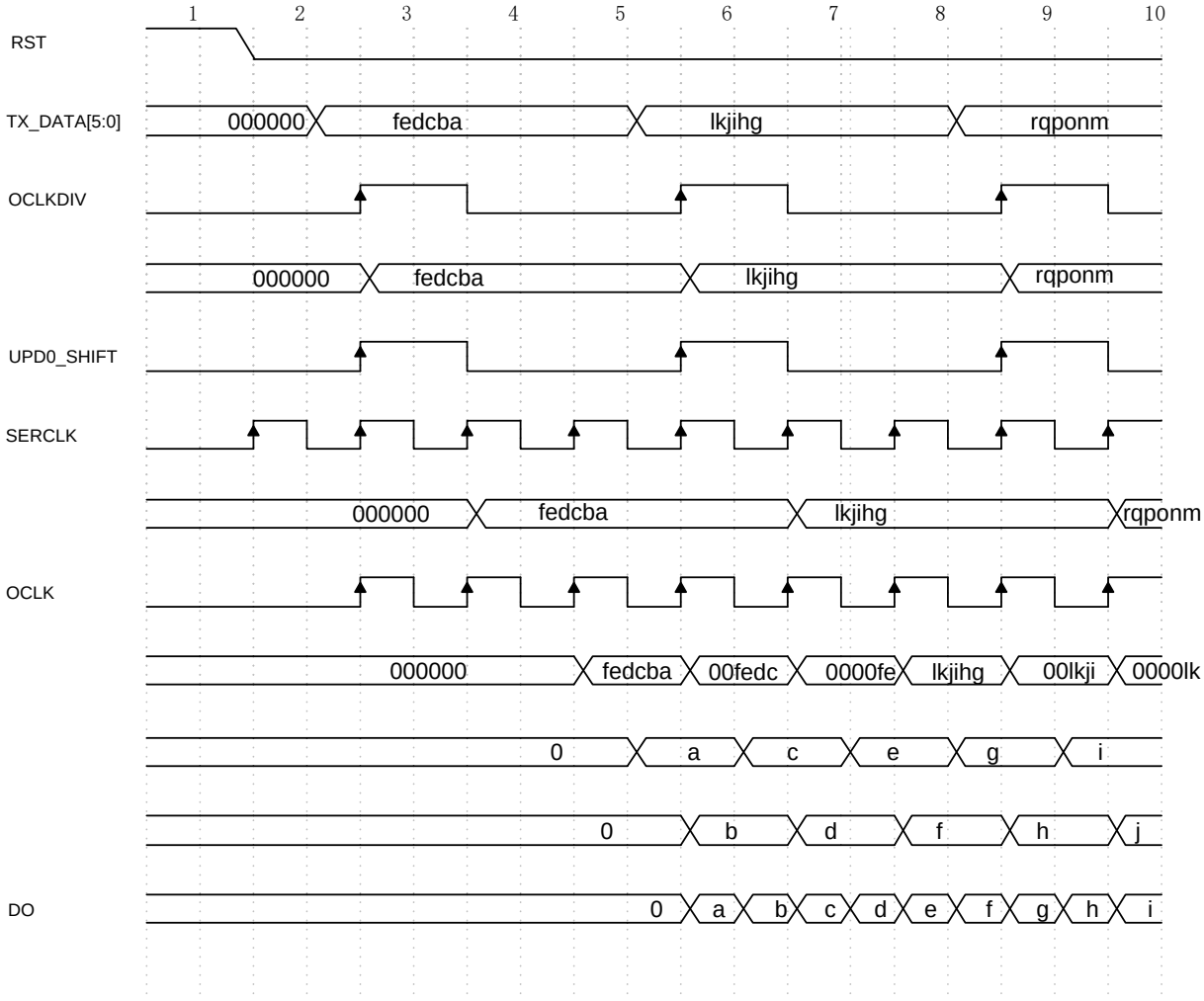


Figure 2-85 DDR6TO1 Timing Diagram

DDR8TO1

When the output logic is configured into DDR8TO1 mode, its functional diagram can be simplified as below.

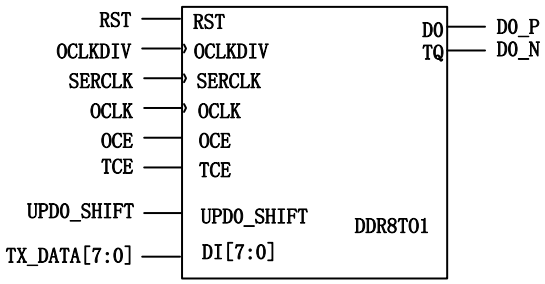


Figure 2-86 DDR8TO1 Functional Diagram

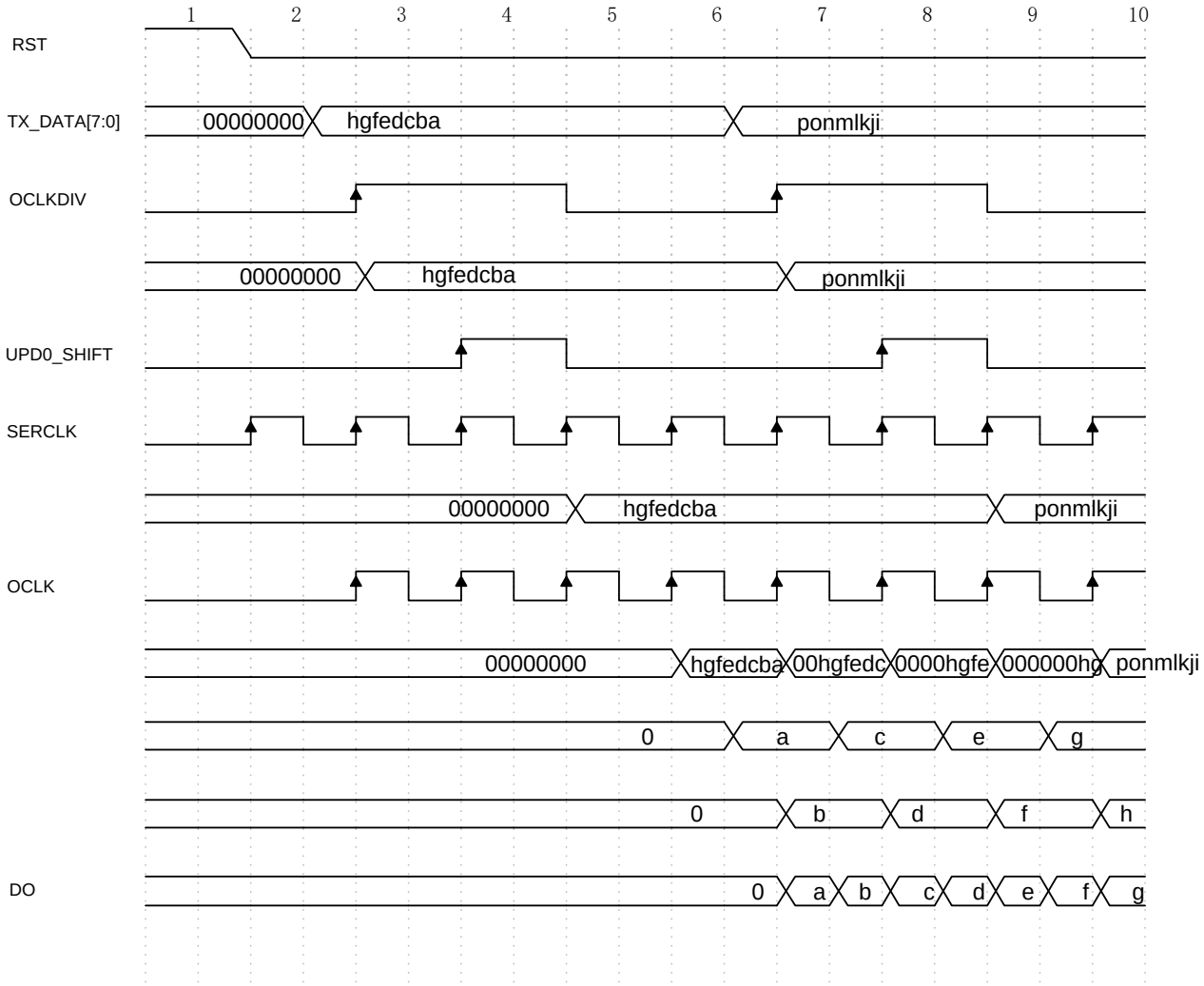


Figure 2-87 DDR8TO1 Timing Diagram

DDR10TO1

When the output logic is configured into DDR10TO1 mode, its functional diagram can be simplified as below.

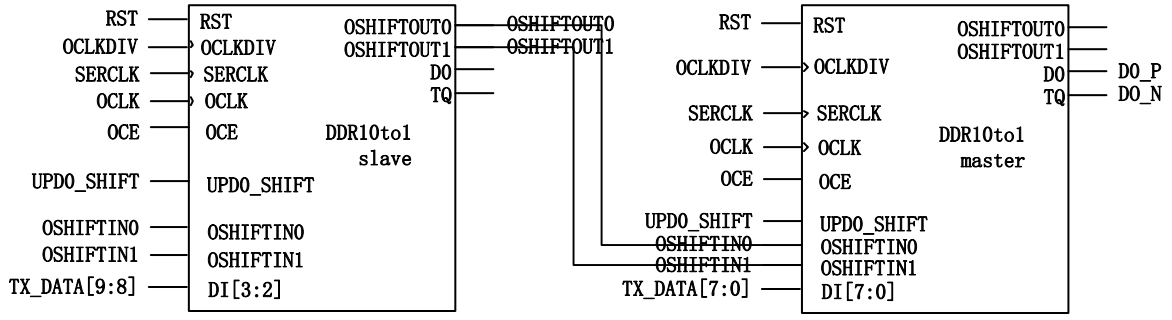


Figure 2-88 DDR10TO1 Functional Diagram

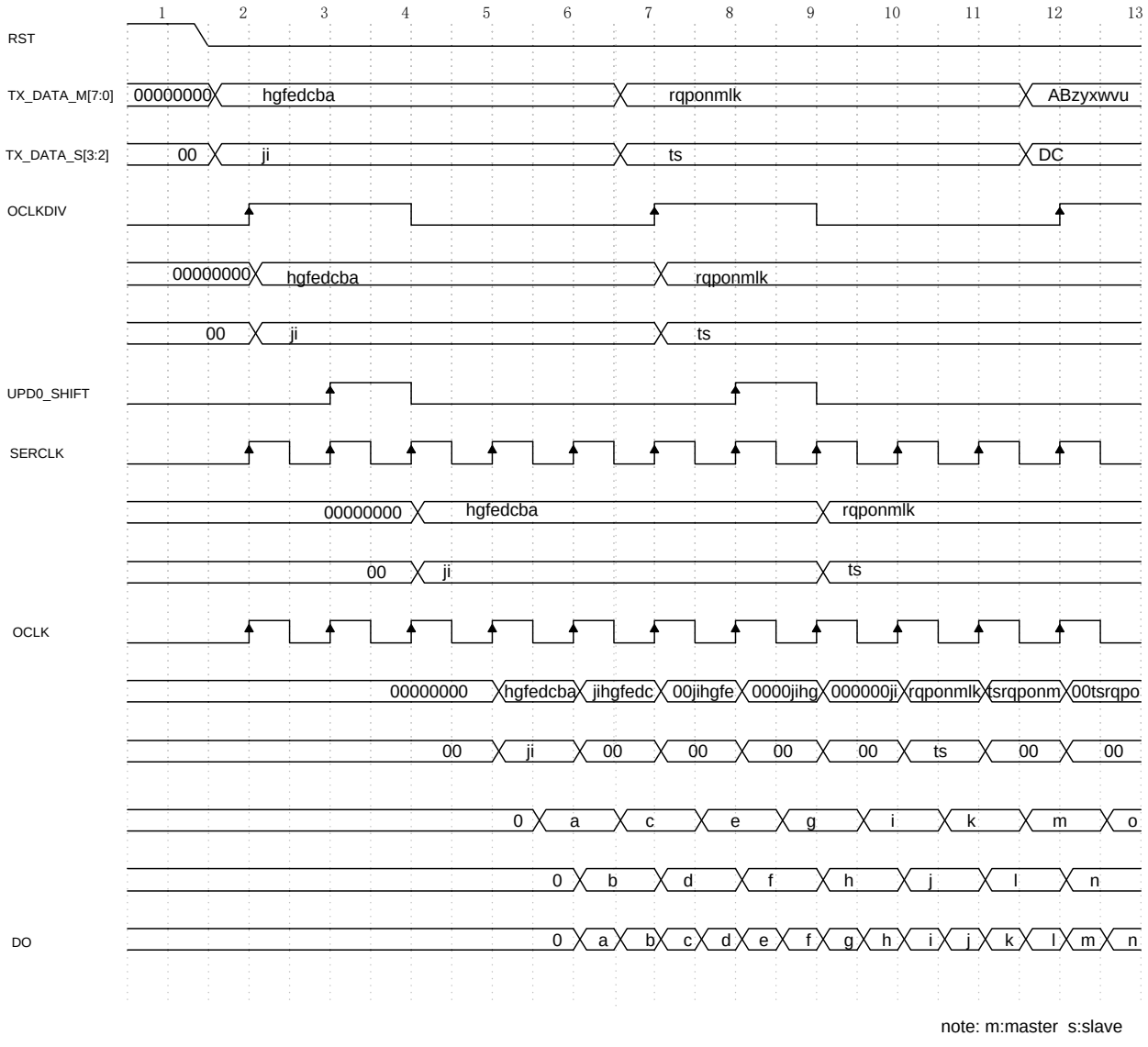


Figure 2-89 DDR10TO1 Timing Diagram

DDR14TO1

When the output logic is configured into DDR14TO1 mode, its functional diagram can be simplified as below.

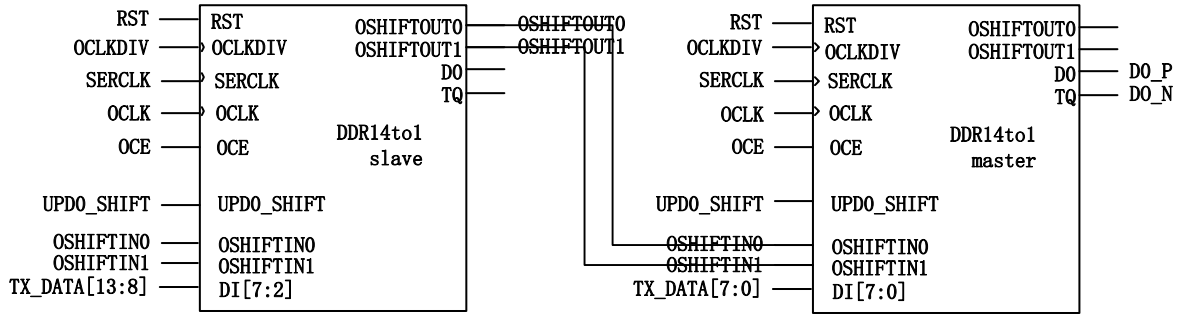


Figure 2-90 DDR14TO1 Functional Diagram

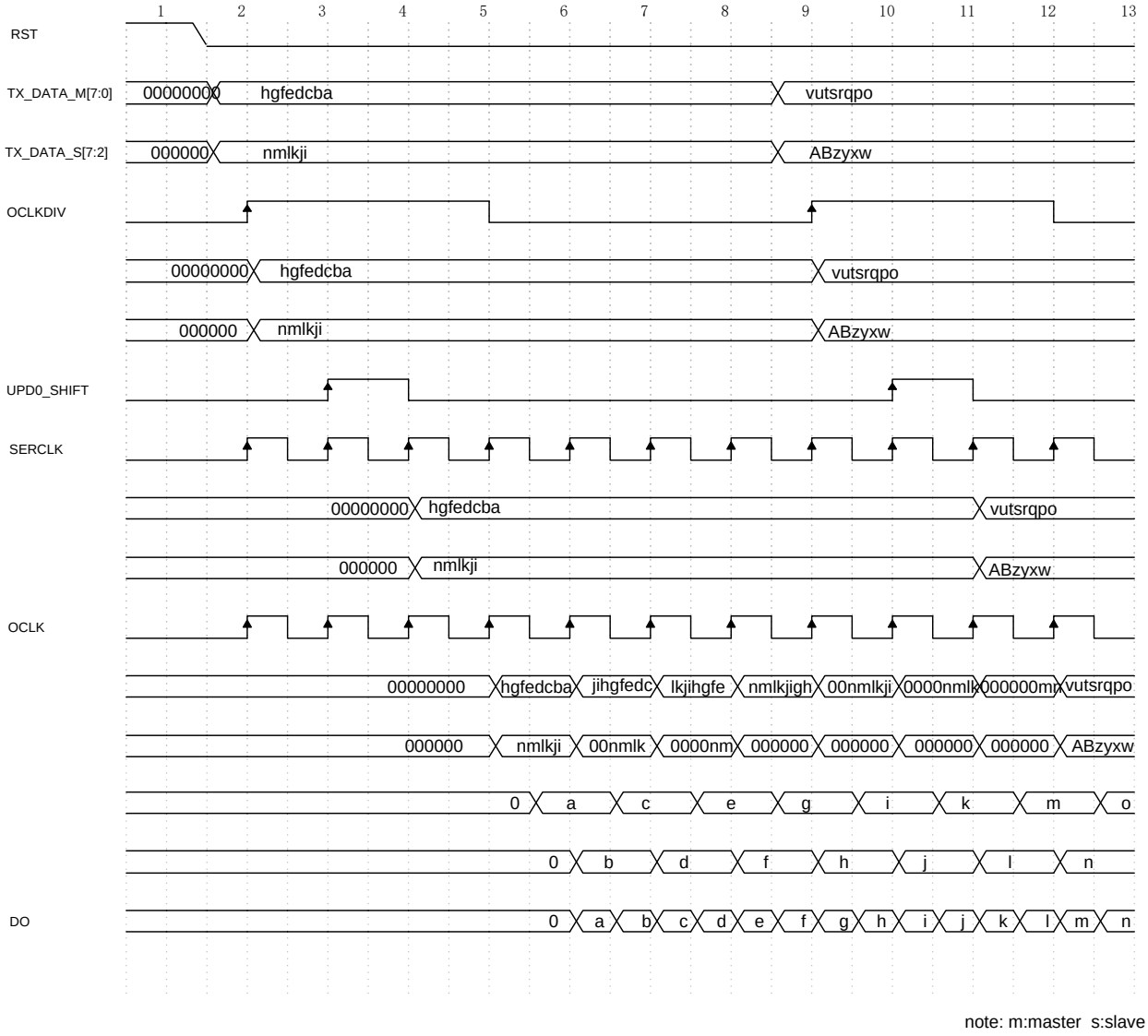


Figure 2-91 DDR14TO1 Timing Diagram

HMSDR4TO1

When the output logic is configured into HMSDR4TO1 mode, its functional diagram can be simplified as below.

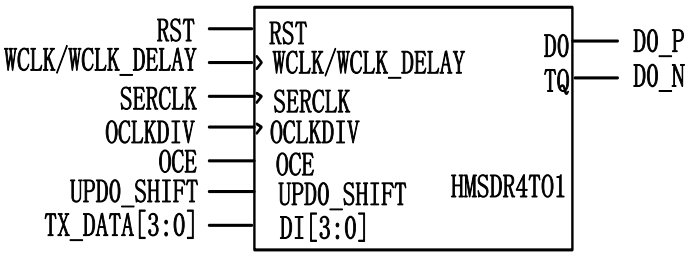


Figure 2-92 HMSDR4TO1 Functional Diagram

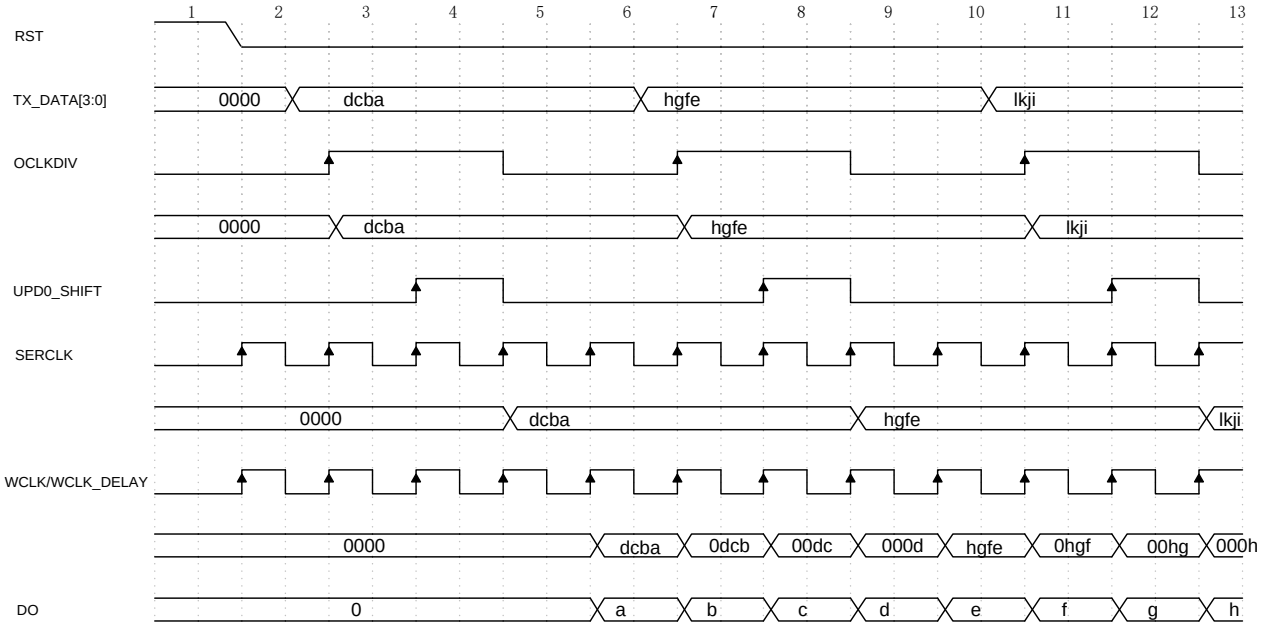


Figure 2-93 HMSDR4TO1 Timing Diagram

HMSDR8TO1

When the output logic is configured into HMSDR8TO1 mode, its functional diagram can be simplified as below.

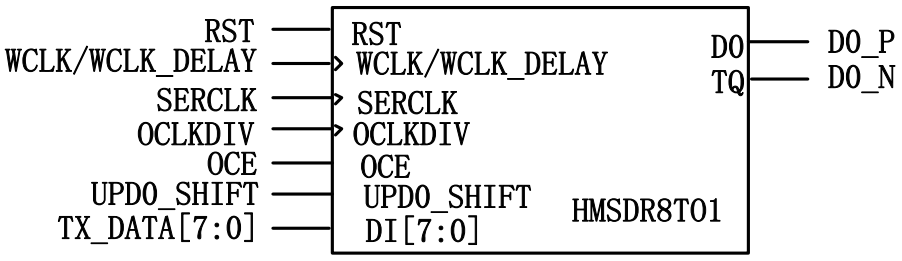


Figure 2-94 HMSDR8TO1 Functional Diagram

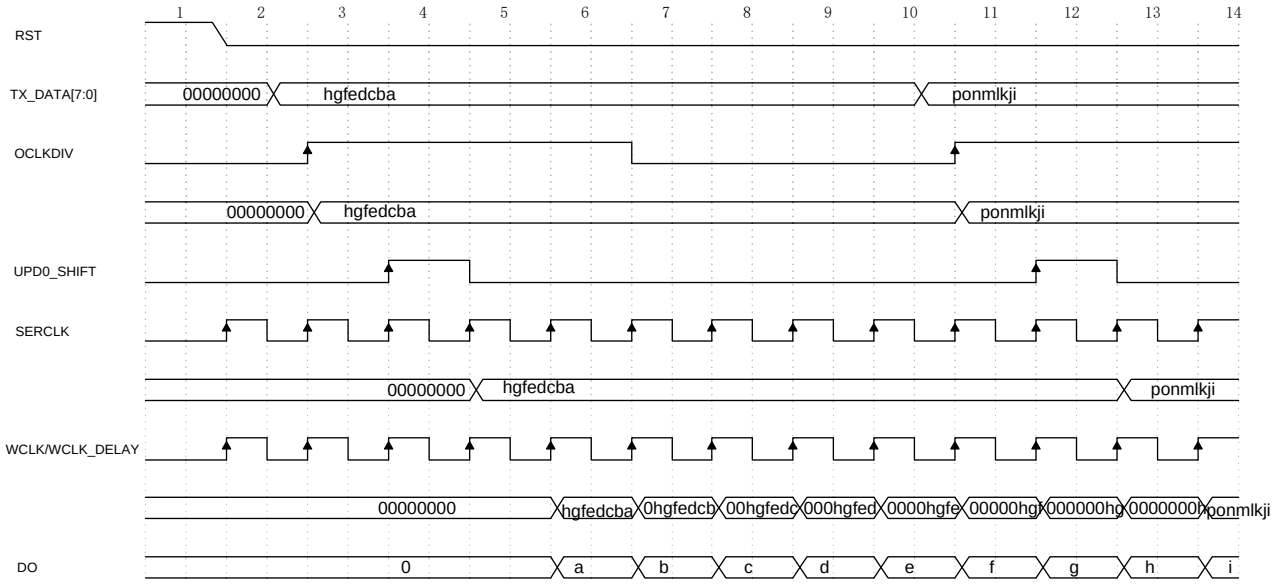


Figure 2-95 HMSDR8TO1 Timing Diagram

2.3.3.3 TSERDES

When OSERDES is used in conjuction with TSERDES, the output logic is set toTSERDES, with the following different operating modes.

SDR2TO1

When the input logic is configured into SDR2TO1 mode, its connection diagram can be simplified as below.

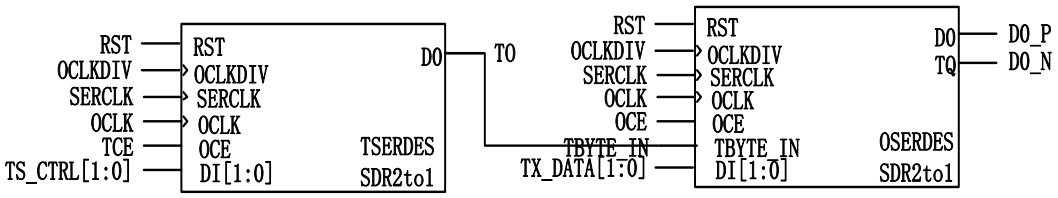


Figure 2-96 TSERDES SDR2TO1 Connection Diagram

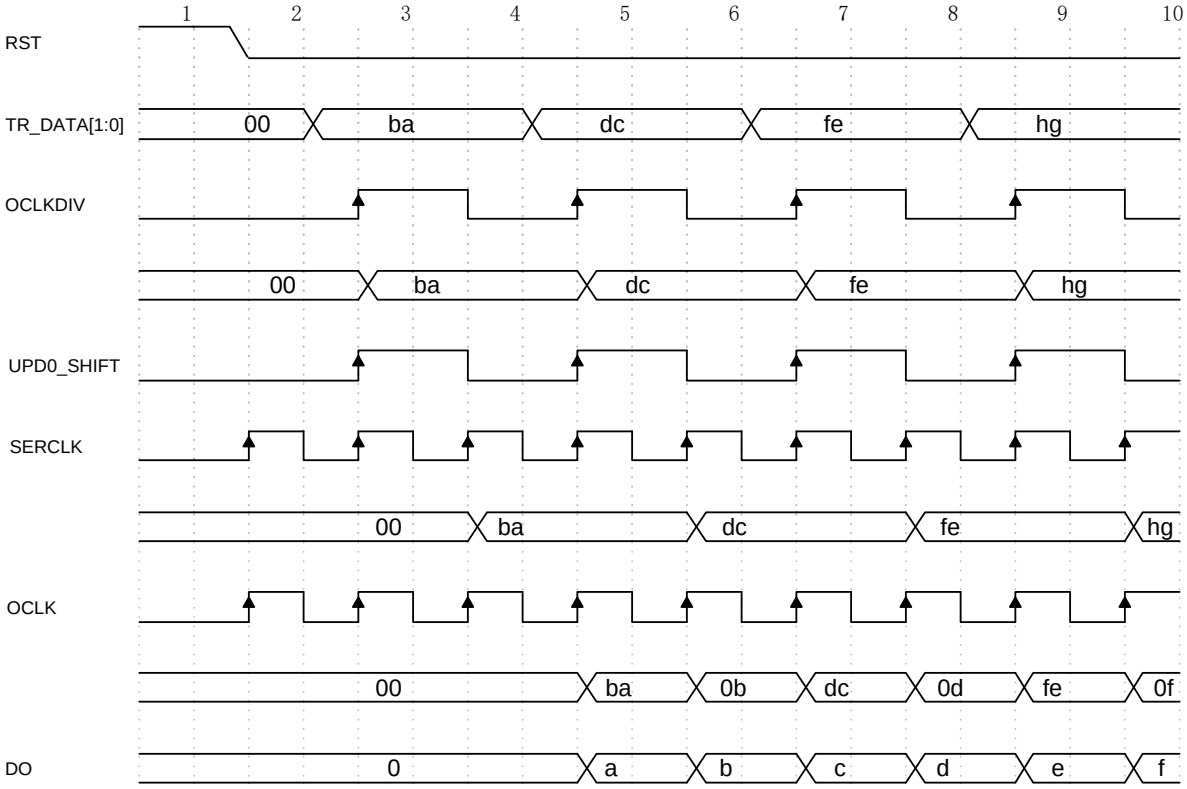


Figure 2-97 TSERDES SDR2TO1 Timing Diagram

SDR4TO1

When the output logic is configured into SDR4TO1 mode, its connection diagram can be simplified as below.

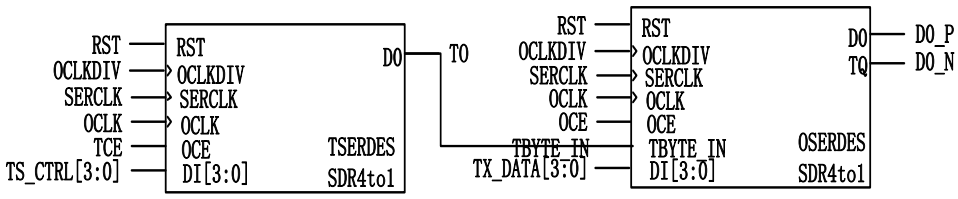


Figure 2-98 TSERDES SDR4TO1 Connection Diagram

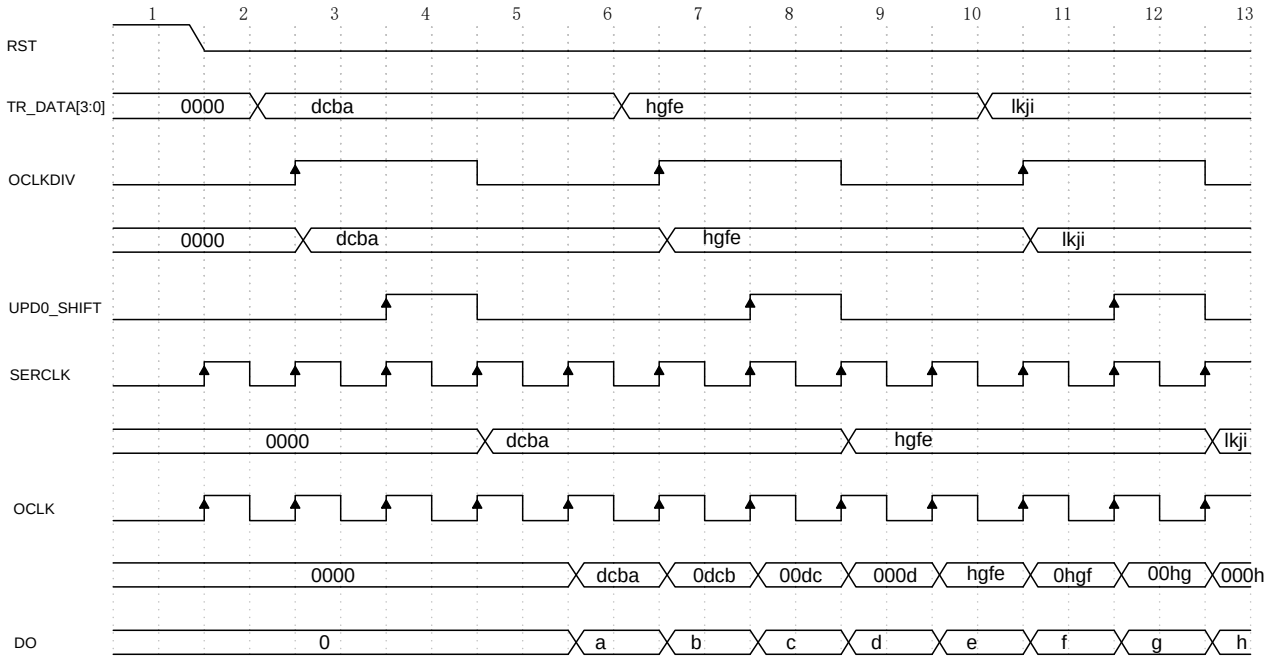


Figure 2-99 TSERDES SDR4TO1 Timing Diagram

SDR8TO1

When the output logic is configured into SDR8TO1 mode, its connection diagram can be simplified as below.

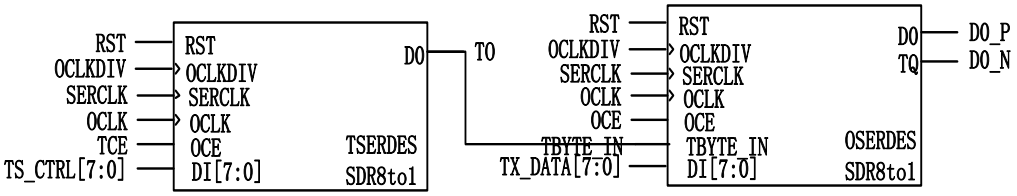


Figure 2-100 TSERDES SDR8TO1 Connection Diagram

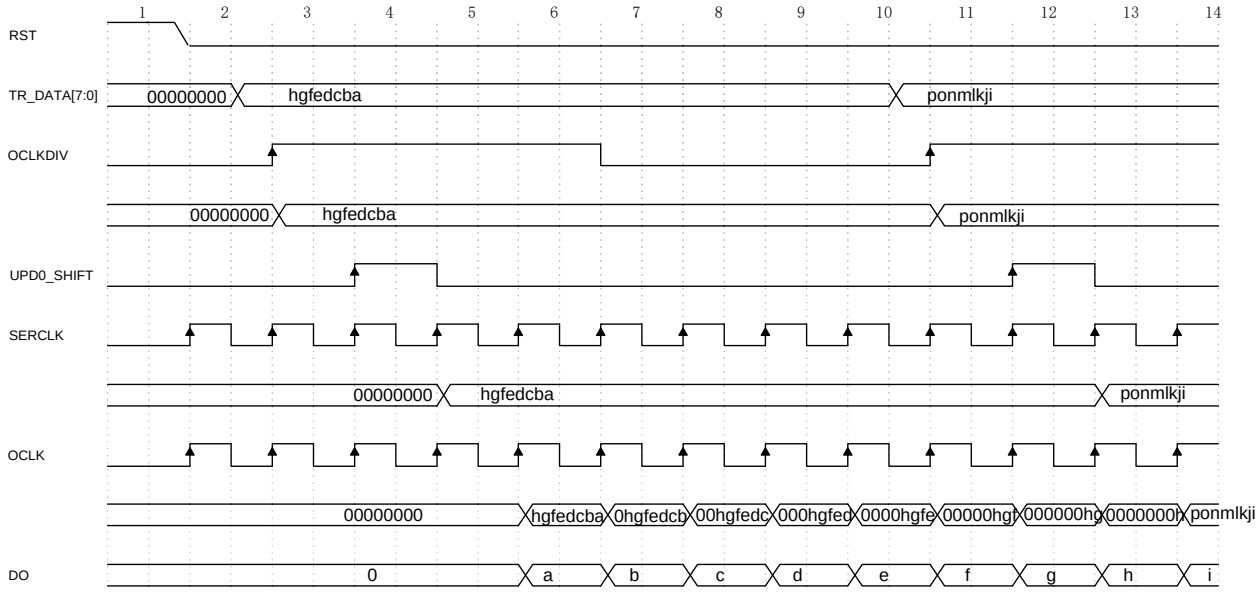


Figure 2-101 TSERDES SDR8TO1 Timing Diagram

DDR4TO1

When the output logic is configured into DDR4TO1 mode, its connection diagram can be simplified as below.

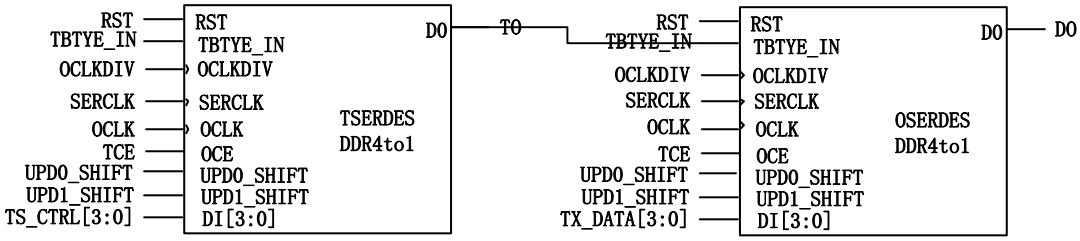


Figure 2-102 TSERDES DDR4TO1 Connection Diagram

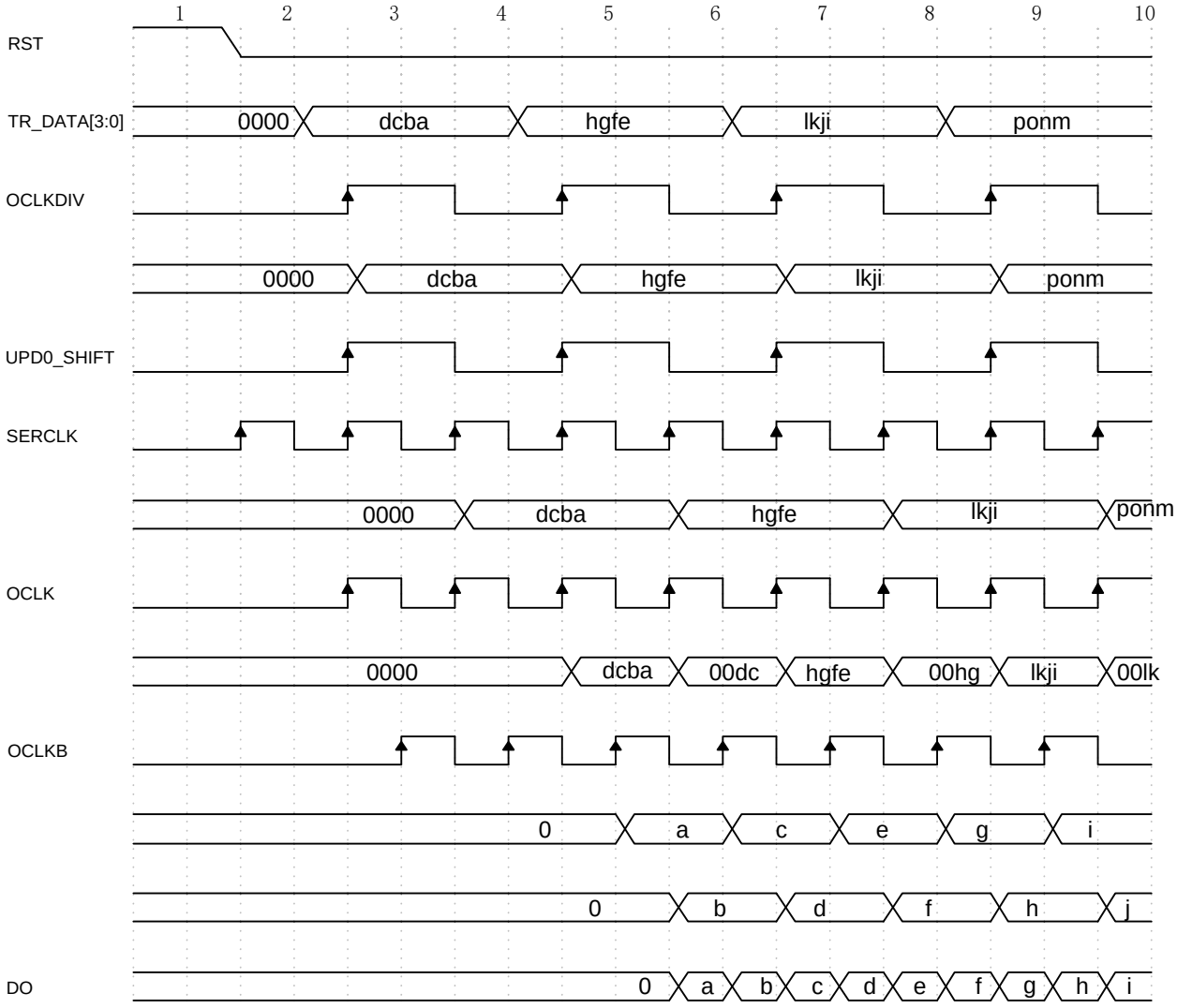


Figure 2-103 TSERDES DDR4TO1 Timing Diagram

DDR8TO1

When the output logic is configured into DDR8TO1 mode, its connection diagram can be simplified as below.

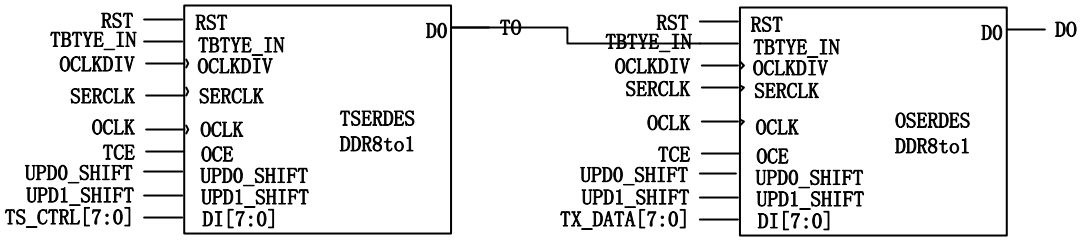


Figure 2-104 TSERDES DDR8TO1 Connection Diagram

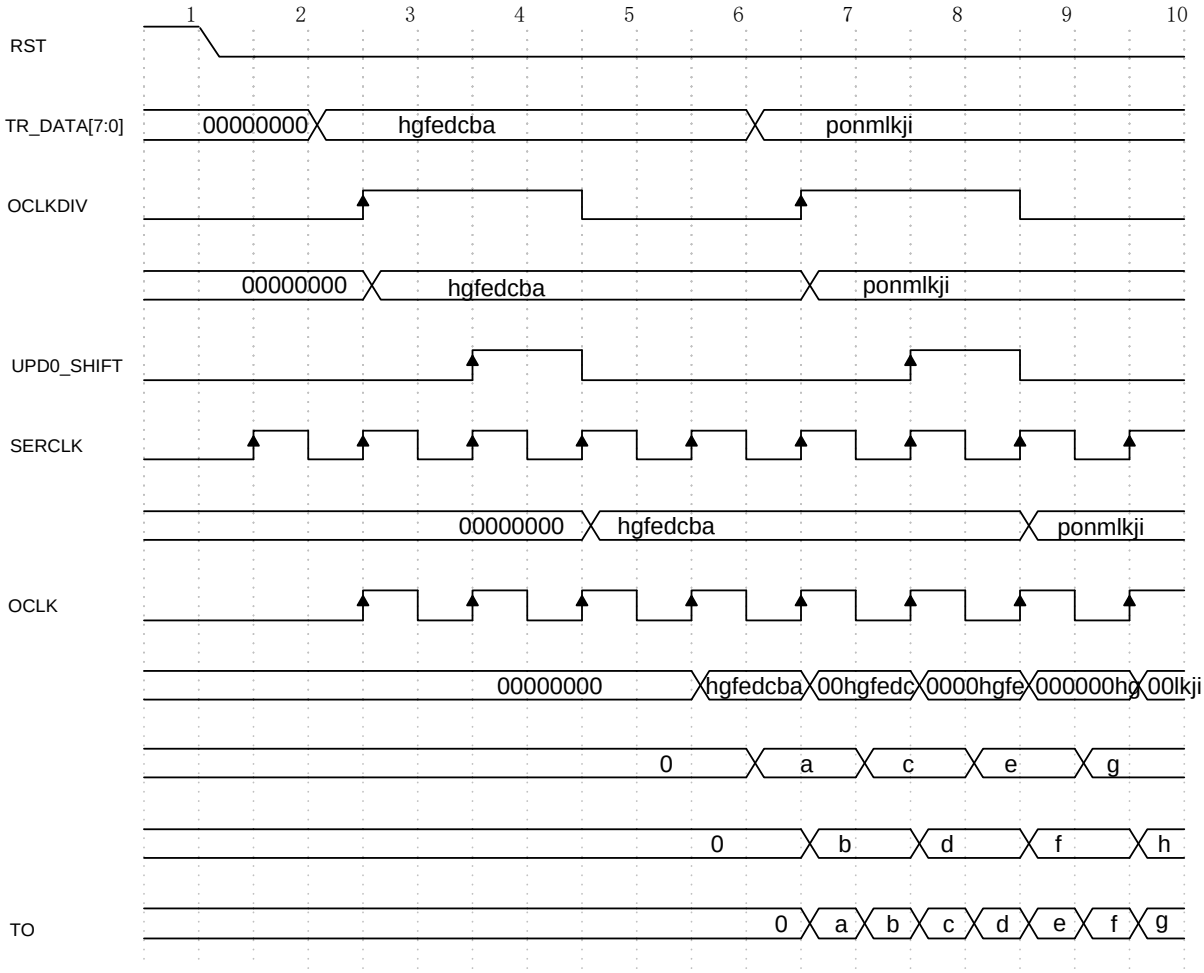


Figure 2-105 TSERDES DDR8TO1 Functional Diagram

HMSDR4TO1

When the output logic is configured into HMSDR4TO1 mode, its connection diagram can be simplified as below.

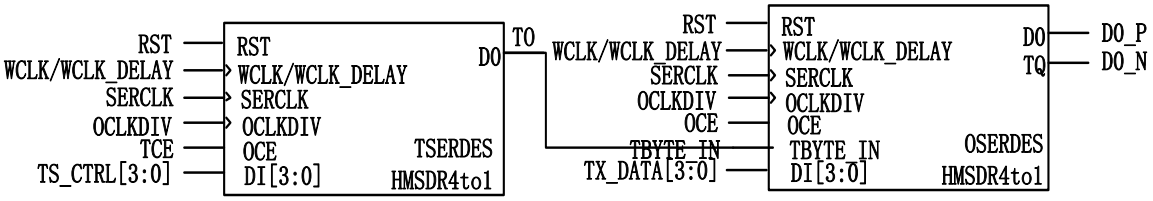


Figure 2-106 TSERDES HMSDR4TO1 Connection Diagram

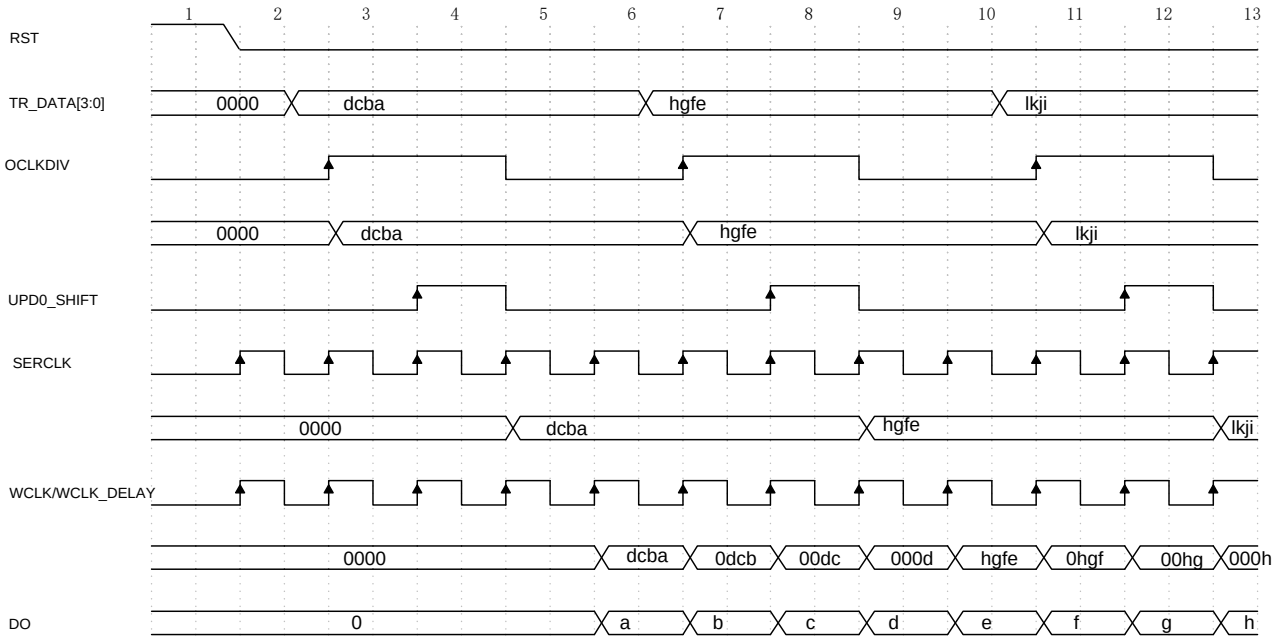


Figure 2-107 TSERDES HMSDR4TO1 Timing Diagram

HMSDR8TO1

When the output logic is configured into HMSDR8TO1 mode, its connection diagram can be simplified as below.

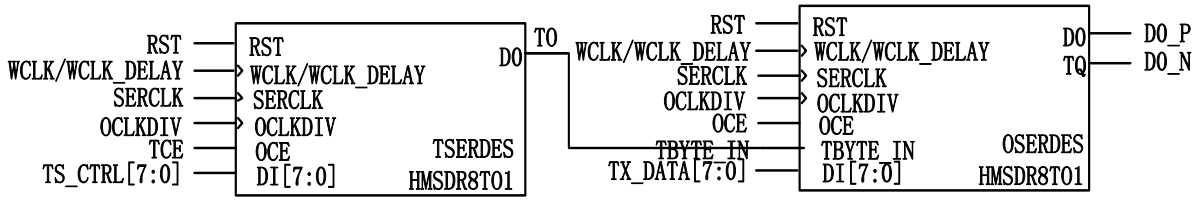


Figure 2-108 TSERDES HMSDR8TO1 Connection Diagram

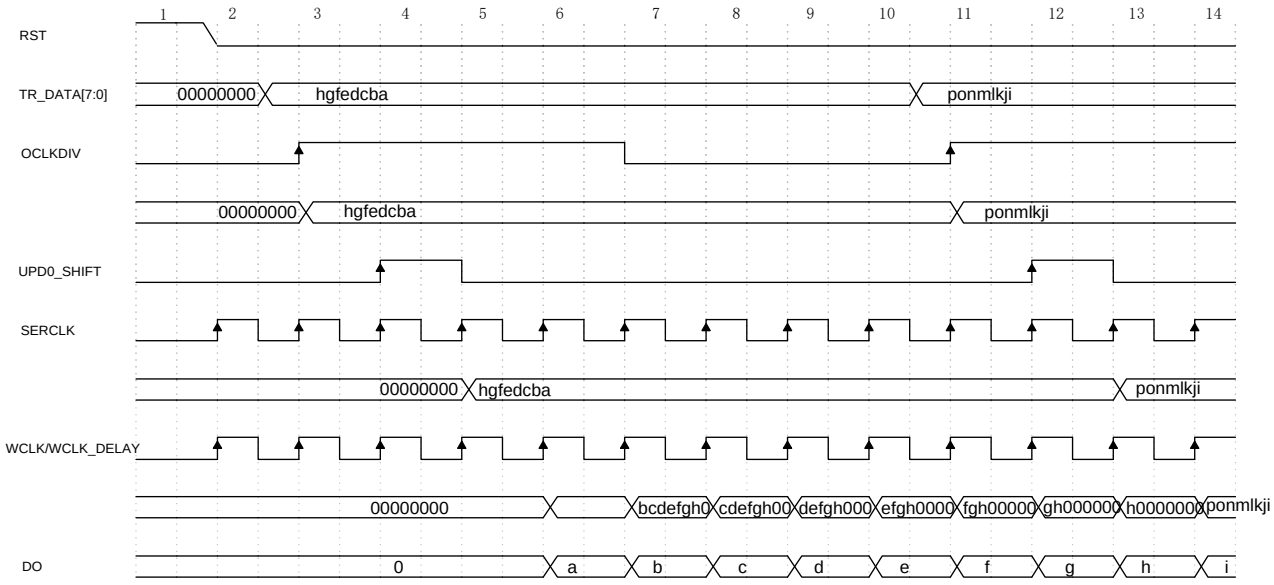
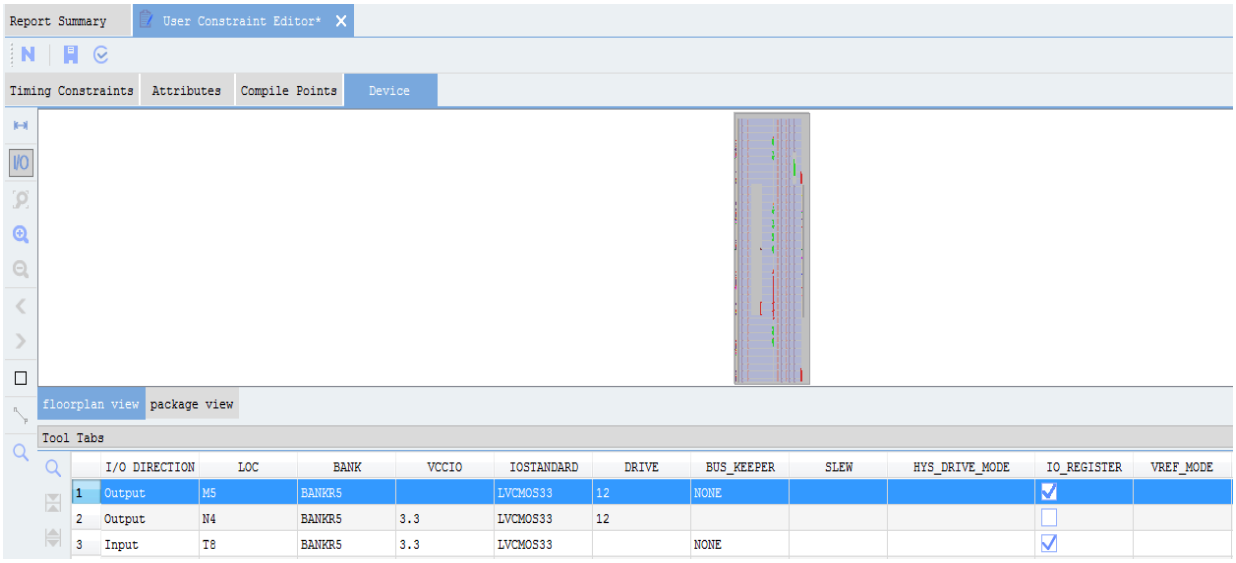


Figure 2-109 TSERDES HMSDR8TO1 Timing Diagram

2.3.4 Input/output Register Setup

To use the input and output registers, check the box under “IO_REGISTER” for the corresponding IO in PDS>UCE>Device>IO Tabs, as shown below.



	I/O DIRECTION	LOC	BANK	VCCIO	IOSTANDARD	DRIVE	BUS_KEEPER	SLEW	HYS_DRIVE_MODE	IO_REGISTER	VREF_MODE
1	Output	M5	BANKR5		LVCMOS33	12	NONE			☑	
2	Output	N4	BANKR5	3.3	LVCMOS33	12				☐	
3	Input	T8	BANKR5	3.3	LVCMOS33		NONE			☑	

Figure 2-110 IO Register Constraint Method

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