Compa Family CPLDs Input/Output Interface (IO) User Guide

(UG030005, V1.3)

(26.08.2023)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.3	26.08.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Full Spelling
OD	Over Drive
UD	Under Drive
IOBS	IO Buffer Single Ended
IOBD	IO Buffer Differential
IOBR	IO Buffer Reference
FDC	FPGA Design Constraint
UCE	User Constraint Editor
HS	High Speed
LP	Low Power
CCS	Configureation Control System
SDR	Single Data Rate
IDDR	Input Double Data Rate
ODDR	Output Double Data Rate
ISERDES	Input SERializer-DESerializer
OSERDES	Output SERializer-DESerializer
GTP	General Technology Primitive

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Chapter 1 Overview of I/O Unit

Compa Family CPLDs devices feature configurable high-performance I/O units with support for various I/O standards and level standards, which can support high-speed data transmission in conjunction with ISERDES/OSERDES.

Each I/O unit of the Compa Family CPLDs devices contains one IO Buffer, 1 IO Logic, and 1 delay module. The delay module can be statically configured to either input delay or output delay, but input and output delays cannot be used simultaneously. Its structure is shown in Figure 1-1.

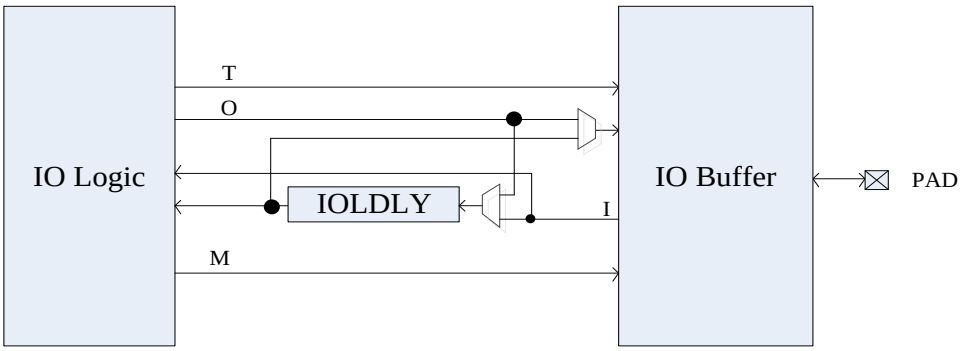


Figure 1-1 I/O Structure Schematic

Chapter 2 Detailed Introduction to I/O Unit

2.1 Compa Family CPLDs Devices I/O Bank Description

2.1.1 I/O Bank Arrangement

The I/Os of the Compa Family CPLDs devices are distributed by Bank. Banks are arranged in the 4 sides of the device in different numbers, as shown in Table 2-1 for different devices.

Table 2-1 Arrangement of Bank Resources for Compa Family CPLDs Devices

I/O Bank Resources	PGC1KL	PGC1KG	PGC2K	PGC4K	PGC7K
I/O Banks on the left	1	3	3	3	3
I/O Banks on the right	1	1	1	1	1
I/O Banks on the upper side	1	1	1	1	1
I/O Banks on the lower side	1	1	1	1	1
Total Number of I/O Banks	4	6	6	6	6

PGC1KL has 4 Banks, with one Bank on each of the 4 sides: top, bottom, left, and right. As shown in Figure 2-1.

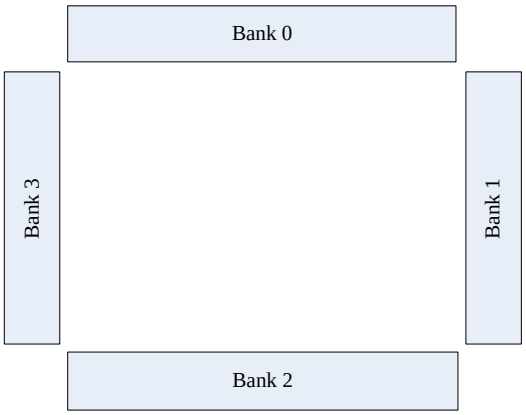


Figure 2-1 Top-view of PGC1KL Bank Distribution

PGC1KG, PGC2K, PGC4K, and PGC7K each have 6 Banks, with their distributions as shown in Figure 2-2.

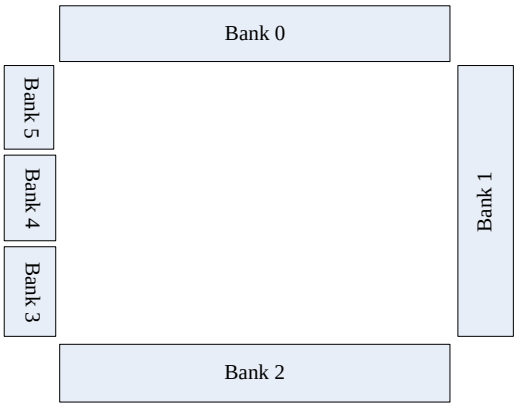


Figure 2-2 Top-view of PGC2K/PGC4K/PGC7K Bank Distribution

2.1.2 I/O Bank voltage

Each Bank is powered by an independent Bank power supply VCCIO, which supports 1.2V, 1.5V, 1.8V, 2.5V and 3.3V. I/Os in each Bank share a common VCCIO; different Banks can have different VCCIO voltages.

For the Compa CPLDs devices, the I/O standards used within the Bank is limited; the voltage of the output standards must match VCCIO. However, due to specialised circuits built into the Compa Family CPLDs devices, input standards have certain compatibility with different VCCIO voltages. See the table below for details of mixed voltage input combination mode within the same Bank:

Table 2-2 List of LVCMOS and LVTTL Mixed Voltage Input Combinations

VCCIO(V)	**Input (V)**					
	1.0	**1.2**	**1.5**	**1.8**	**2.5**	**3.3**
1.2		√	√[2]			
1.5		√[1]	√	√[2]	√[2]	√[2]
1.8		√[1]	√[1]	√	√[2]	√[2]
2.5	√[1]	√[1]	√[1]	√[1]	√	√[2]
3.3	√[1]	√[1]	√[1]	√[1]	√[1]	√

Note:

1. When the input level is below the Bank's VCCIO voltage, it is termed Under-Drive, abbreviated as UD;
2. When the input level is above the Bank's VCCIO voltage, it is termed Over-Drive, abbreviated as OD.

Table 2-3 List of Differential Input Mixed Voltage Input Combinations

VCCIO(V)	**LVDS/LVPECL33/MLVDS25/BLVDS25/ LVCMOS25D**
2.5	√
3.3	√

For any I/O standard used within a Bank, its VCCIO level must adhere to limitations, which will be checked by the PDS software.

If a Bank does not require a set VCCIO, then VCCIO can be connected to a valid power supply voltage.

2.2 IO Buffer

Compa Family CPLDs devices all feature configurable high-performance I/O drivers and receivers, supporting various single-ended and differential I/O standards. It allows programmatically setting of output drive current, slew rate, and on-die termination resistance.

2.2.1 IO Buffer Structure

Each IO Buffer can be configured with different types of I/O standards. The IO Buffer has 2 golden models.

- IOBS

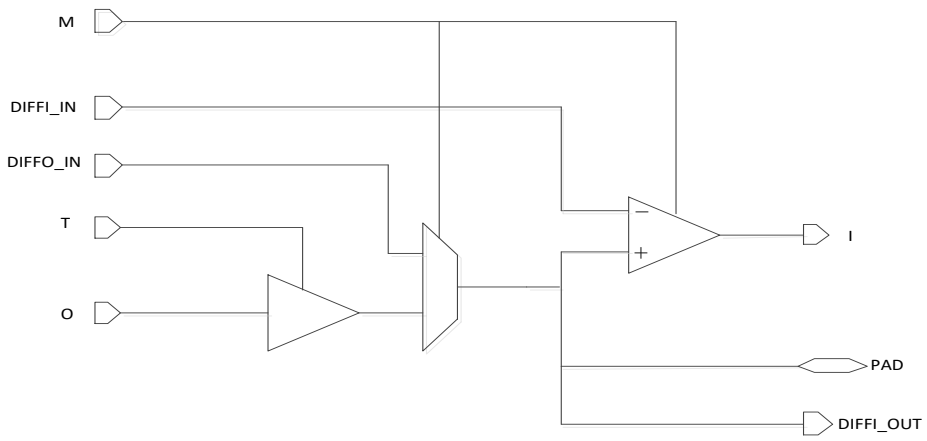


Figure 2-3 IO Buffer Golden Model (IOBS)

IOBS supports all single-ended I/O standards, differential inputs, as well as dynamic switching between high-speed and low-speed MIPI data transfers.

- IOBD

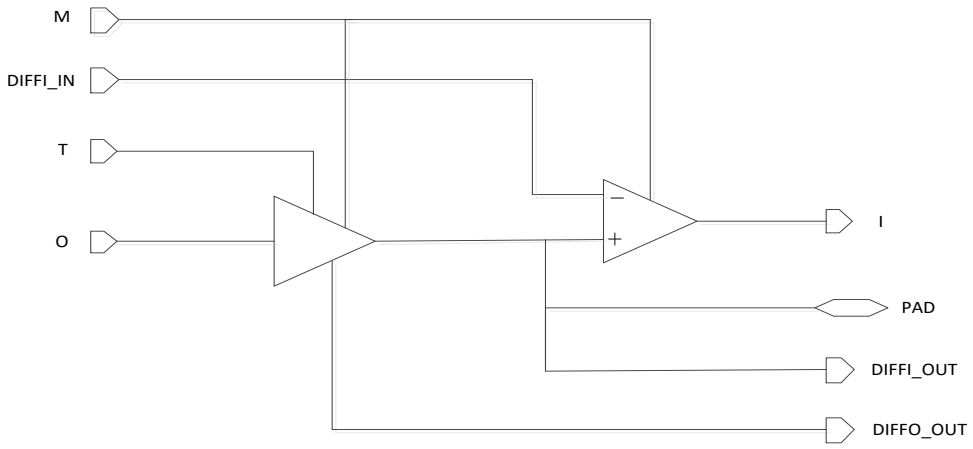


Figure 2-4 IO Buffer Golden Model (IOBD)

In addition to the functions of IOBS, IOBD also supports true differential outputs. The IOBD is only located on the top side of the device (bank0).

2.2.2 Termination Matching Resistors

Termination matching resistors are commonly used to meet signal integrity requirements when using high-speed I/O standards, so as to ensure signal integrity.

The Compa Family CPLDs devices offer internal differential termination resistors of 100Ω, supporting LVDS and MIPI. Internal differential termination matching resistors are only located on the lower side of the device (Bank2).

Internal differential termination matching resistors can be dynamically activated and deactivated, used for switching MIPI between HS (High Speed) and LP (Low Power) input modes. When the standard is selected as MIPI and the IO Buffer type is input, dynamic signal M=1 activates the internal differential termination matching resistor; M=0 deactivates it.

The internal differential termination matching resistors can be configured through I/O constraints. When the attribute DIFF_IN_TERM_MODE of the I/O pin is set to [ON], the internal differential termination matching resistor is enabled. Use the following command to set constraints in the FDC file:

define_attribute {p:*port_name*} {PAP_IO_DIFF_IN_TERM_MODE} {*ON*}

2.2.3 Supported I/O Standards

The IO Buffer of the Compa Family CPLDs devices supports a wide range of single-ended I/O standards, and all I/Os can be used to form differential pairs, which can support many differential signal standards. This flexibility allows users to select the most appropriate I/O standard for each pin to meet the needs of interface and signal integrity.

The I/O standards supported by the Compa Family CPLDs devices are shown in the table below.

Table 2-4 I/O Standards Supported by Compa Family CPLDs

Buffer Type	**I/O Standard**	**Top**	**Bottom**	**Left**	**Right**
Input	LVTTL33	√	√	√	√
	LVCMOS33	√	√	√	√
	LVCMOS25	√	√	√	√
	LVCMOS18	√	√	√	√
	LVCMOS15	√	√	√	√
	LVCMOS12	√	√	√	√
	PCI33		√		
	LVDS	√	√	√	√
	LVPECL33	√	√	√	√
	MLVDS25	√	√	√	√
	BLVDS25	√	√	√	√
	LVTTL33D	√	√	√	√
	LVCMOS33D	√	√	√	√
	LVCMOS25D	√	√	√	√
	MIPI[1]	√	√	√	√
Output	LVTTL33	√	√	√	√
	LVCMOS33	√	√	√	√
	LVCMOS25	√	√	√	√
	LVCMOS18	√	√	√	√
	LVCMOS15	√	√	√	√
	LVCMOS12	√	√	√	√
	PCI33		√		
	LVDS	√			
	LVPECL33[3]	√	√	√	√
	MLVDS25[3]	√	√	√	√
	BLVDS25[3]	√	√	√	√
	LVTTL33D[5]	√	√	√	√
	LVCMOS33D[5]	√	√	√	√
	LVCMOS25D[5]	√	√	√	√
	MIPI[2]	√			
	LVDS25E[3]	√	√	√	√

Buffer Type	I/O Standard	Top	Bottom	Left	Right
Bi-Directional	LVTTL33	√	√	√	√
	LVCMOS33	√	√	√	√
	LVCMOS25	√	√	√	√
	LVCMOS18	√	√	√	√
	LVCMOS15	√	√	√	√
	LVCMOS12	√	√	√	√
	PCI33		√		
	LVCMOS33D	√	√	√	√
	LVCMOS25D	√	√	√	√
	MIPI[4]	√	√	√	√

Note:

1. Unidirectional input HS-MIPI is implemented using a differential input buffer.
2. Unidirectional output HS-MIPI is implemented using a differential output buffer.
3. Differential output levels are simulated using a single-ended driver with external resistors.
4. Unidirectional HS-MIPI, bidirectional LP-MIPI.
5. Differential output is simulated with two single-ended drivers having complementary outputs, with LVCMOS signal levels; no external resistors are needed.

PCI33 (Peripheral Component Interface): This standard supports PCI bus applications, requires a 3.3V VCCIO for output, and does not need a reference voltage or termination voltage V_{TT}.

LVTTL33 (Low-Voltage TTL): A 3.3V standard defined by JESD, requires a 3.3V VCCIO for output, and does not need a reference voltage or termination voltage.

LVCMOS (Low-Voltage CMOS): A low-voltage CMOS standard, with an application voltage from 1.2V to 3.3V. No reference voltage or termination voltage required.

LVDS (Low Voltage Differential Signal): A differential standard where a data bit is transmitted through two signal lines, thus inherently immune to noise compared with single-ended I/O standards. The voltage swing between two signal lines is about 350mV. No reference voltage or termination voltage required. LVDS inputs require matching resistors, which can be discrete resistors on the PCB or differential termination matching resistors in the device enabled through the DIFF_IN_TERM_MODE attribute. Only Bank0 of the CPLDs devices supports true differential output.

SLVS is an adjustable low voltage signal, used for MIPI D-PHY input interfaces.

LVPECL33 (Low Voltage Positive Emitter-Coupled Logic): It is commonly used for on-board clock distribution networks.

MLVD25 (Multipoint Low Voltage Differential Signaling): It is used for optimizing multipoint interconnected applications, which refer to interconnected applications where multiple drivers or receivers share a single physical link, and are used in situations requiring bidirectional multipoint driven differential signal input and output. The I/O itself does not support such output standard; it

requires the complementary output principle of LVCMOS and external resistors to implement this standard.

BLVDS25 (Bus Low Voltage Differential Signaling): An output standard similar to the MLVDS25 standard, also used in situations requiring bidirectional multipoint driven differential signal input and output. The difference between the two is that MLVDS25 is an industrial standard, and has a larger differential amplitude than BLVDS25, requiring a higher current driving capability. The I/O itself does not support BLVDS25; it requires the complementary output principle of LVCMOS and external resistors to implement this standard.

I/O Standards can be constrained through the following statement in the FDC file or operated on the PDS's UCE interface.

define_attribute {p:*port_name*} {PAP_IO_STANDARD} { *LVCMOS33* }

2.2.4 Introduction to IO Buffer Power Supply

The IO Buffer of the Compa Family CPLDs devices is powered by a combination of VCC_{CORE} and VCCIO. Wherein, VCC_{CORE} as the core voltage, is primarily used to power the control logic circuit of the IO Buffer and the majority of the IO Logic circuitry; VCCIO is independently used in each Bank, mainly to power the output drive circuit and input buffer. The characteristic values of IO standards powered by VCCIO will vary with VCCIO voltage.

2.2.5 BUS KEEPER Feature

The main function of the BUS KEEPER circuit is to maintain the current I/O data state before the next I/O data takes effect. Each I/O has an independent BUS KEEPER function, typically with four programmable working modes: PULLUP (weak pull-up), PULLDW (weak pull-down), KPR (keep output) and UNUSED (unused).

BUS KEEPER feature can be edited through the following statement in the FDC file or operated in the PDS's UCE interface.

define_attribute {p:*port_name*} {PAP_IO_*UNUSED*} {TRUE}

2.2.6 Input Hysteresis Feature

Input hysteresis feature is supported by LVTTL33, PCI33, LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, LVCMOS33. The programmable modes for single-ended input hysteresis are: HYS and NOHYS (no hysteresis); differential input hysteresis is at a fixed value.

Input hysteresis feature can be edited through the following statement in the FDC file or operated in the PDS's UCE interface.

define_attribute {p:*port_name*} {PAP_IO_HYS_DRIVE_MODE} {*NOHYS*}

2.2.7 Programmable Output Drive Capability

The Compa Family CPLDs devices support programmable I/O output drive capability, with detailed information as shown in the table below.

Table 2-5 Drive Capability of I/O Output Standards

Buffer Type	**I/O Std**	**Drive Capabilities**	**VCCIO (V)**
Single-Ended	LVTTL33	4,8,12,16	3.3
	LVCMOS33	4,8,12,16	3.3
	LVCMOS25	4,8,12,16	2.5
	LVCMOS18	4,8,12	1.8
	LVCMOS15	4,8	1.5
	LVCMOS12	2,6	1.2
	MIPI	2,6	1.2
	PCI33	4	3.3
Differential	LVDS	2,2.5,3,3.5,4,4.5	2.5,3.3
	LVDS25E	4,8,12,16	2.5
	LVPECL33	8,16	3.3
	MLVDS25	8,12,16	2.5
	BLVDS25	8,12,16	2.5
	LVTTL33D	8,12	3.3
	LVCMOS33D	4,8,12,16	3.3
	LVCMOS25D	4,8,12,16	2.5

The output drive capability of the I/O can be constrained using the following statement in the FDC file, or operated in the PDS's UCE interface.

define_attribute {p:*port_name*} {PAP_IO_DRIVE} {*4*}

2.2.8 Open-Drain Control

Each IO Buffer's single-ended output drive circuit can independently support the Open-Drain function under LVCMOS and LVTTL standards, requiring an external pull-up resistor on the pin.

Open-Drain control includes ON and OFF.Open-Drain control can be constrained using the following statement in the FDC file, or operated on the PDS's UCE interface.

define_attribute {p:*port_name*} {PAP_IO_OPEN_DRAIN} {*OFF*}

2.2.9 Programmable Slew Rate

Based on the requirements to reduce output noise or enhance high-speed output performance, each I/O output driver has a programmable slew rate control setting for controlling the speed of the output slew rate. The slew rate control for each I/O is independent. The available parameters are: "FAST" and "SLOW".

Programmable slew rates can be constrained in the FDC file with the following statement, or constrained within the PDS UCE interface.

define_attribute { p:*port_name* } {PAP_IO_SLEW} {*FAST*}

2.2.10 Pseudo-Differential Output Implementation

In CPLDs I/O circuit design, true differential output can be implemented through the differential output driving circuit for LVDS, so these differential output buffers do not require additional resistors outside the driving circuit. However, LVPECL33, MLVDS, and BLVDS require external resistors to implement differential output.

All pairs of single-ended IO Buffers can support pseudo-differential output at different data rates with external resistors, with specific speeds determined by the capabilities of the single-ended IO Buffers adopted by each output standard.

- Pseudo-Differential Output - LVPECL33

  LVPECL33 output is primarily used for point-to-point applications, with the most common example being clock distribution networks at the board level. The figure below shows a possible implementation of LVPECL33 in a point-to-point application.

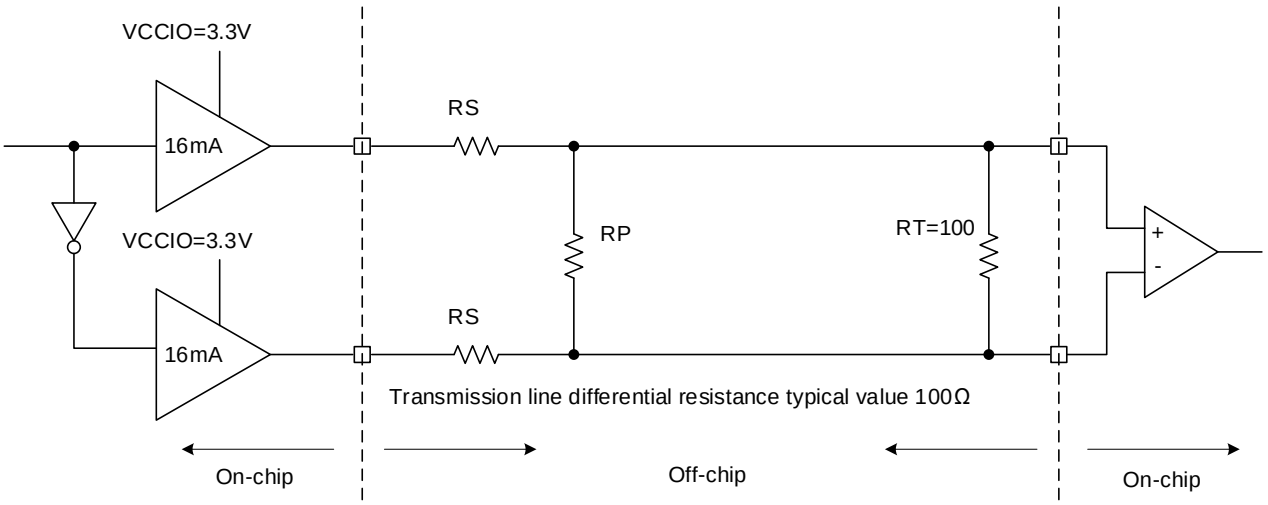


Figure 2-5 LVPECL Point-to-Point Output Example

- Pseudo-differential Output - MLVDS25

MLVDS25 is used in cases where bidirectional multipoint driven differential input and output signals is required. The I/O itself does not support such output standard; it requires the complementary output principle of LVCMOS and external resistors to implement this standard. The differential amplitude of MLVDS25 is larger than that of BLVDS25, and it requires a higher current driving capability. The figure below shows a typical application of BLVDS25 multi-point configuration.

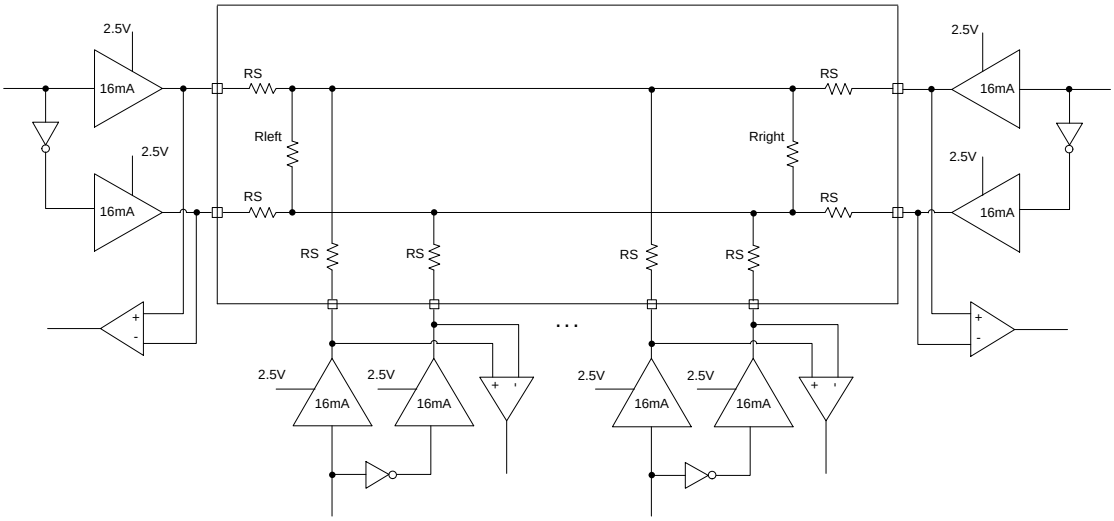


Figure 2-6 MLVDS25/BLVDS25 Point-to-Point Output Example

- Pseudo-differential Output - BLVDS25

BLVDS25 is an output standard similar to the MLVDS25 standard, also used in situations requiring bidirectional multipoint driven differential signal input and output. The difference between the two is that MLVDS25 is an industrial standard, and has a larger differential amplitude than BLVDS25, requiring a higher current driving capability. The implementation method is consistent with MLVDS25; the circuit structure is shown in Figure 2-6.

- Pseudo-differential Output - LVDS25E

  The 2.5V pseudo-differential LVDS25E output is implemented through LVCMOS complementary output; the figure below presents an implementation example of LVDS25E.

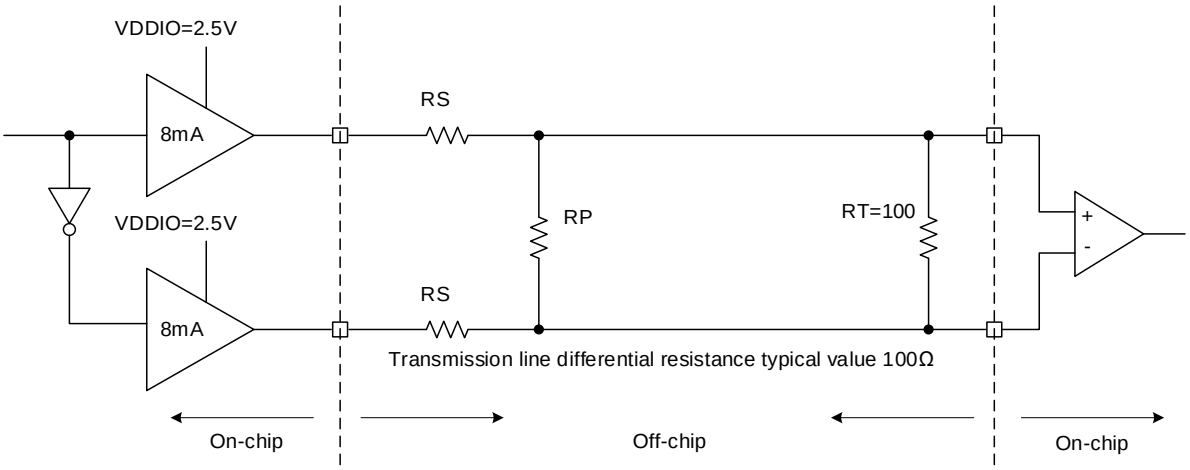


Figure 2-7 LVDS25E Point-to-Point Output Example

2.2.11 MIPI Implementation Method

2.2.11.1 Implement MIPI Input with 4 I/O Units

Unidirectional HS-MIPI input can be implemented with 2 I/O units, using LVCMOS25D and external resistors, and bidirectional LP-MIPI can be implemented with 2 I/O units using LVCMOS12. This structure block diagram is shown in the figure below.

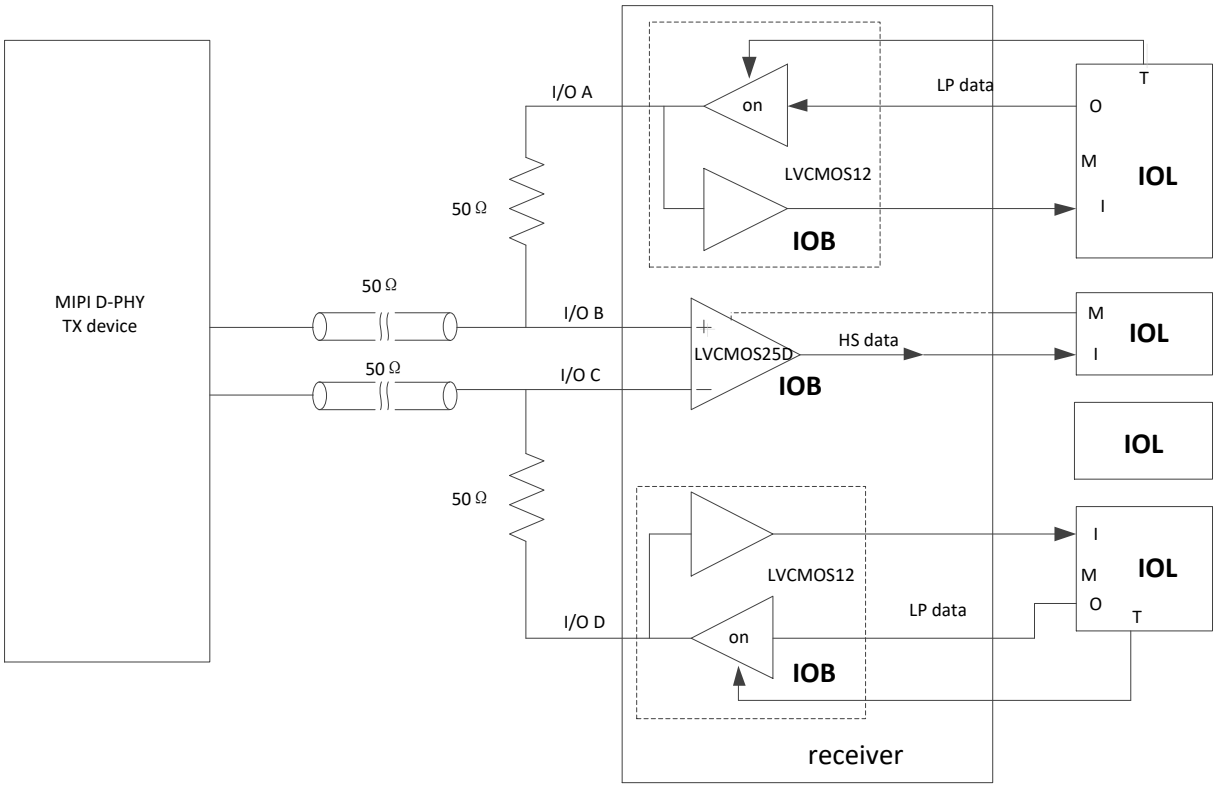


Figure 2-8 MIPI Input with 4 I/O Units (HS/LP)

2.2.11.2 Implement MIPI Input with Two I/O Units

Unidirectional HS-MIPI input can be implemented using MIPI and 2 I/O units; bidirectional LP-MIPI can be implemented using LVCMOS12 with the same pair of I/O units, with HS-MIPI and LP-MIPI sharing a pair of I/O units. This structure block diagram is shown in the figure below.

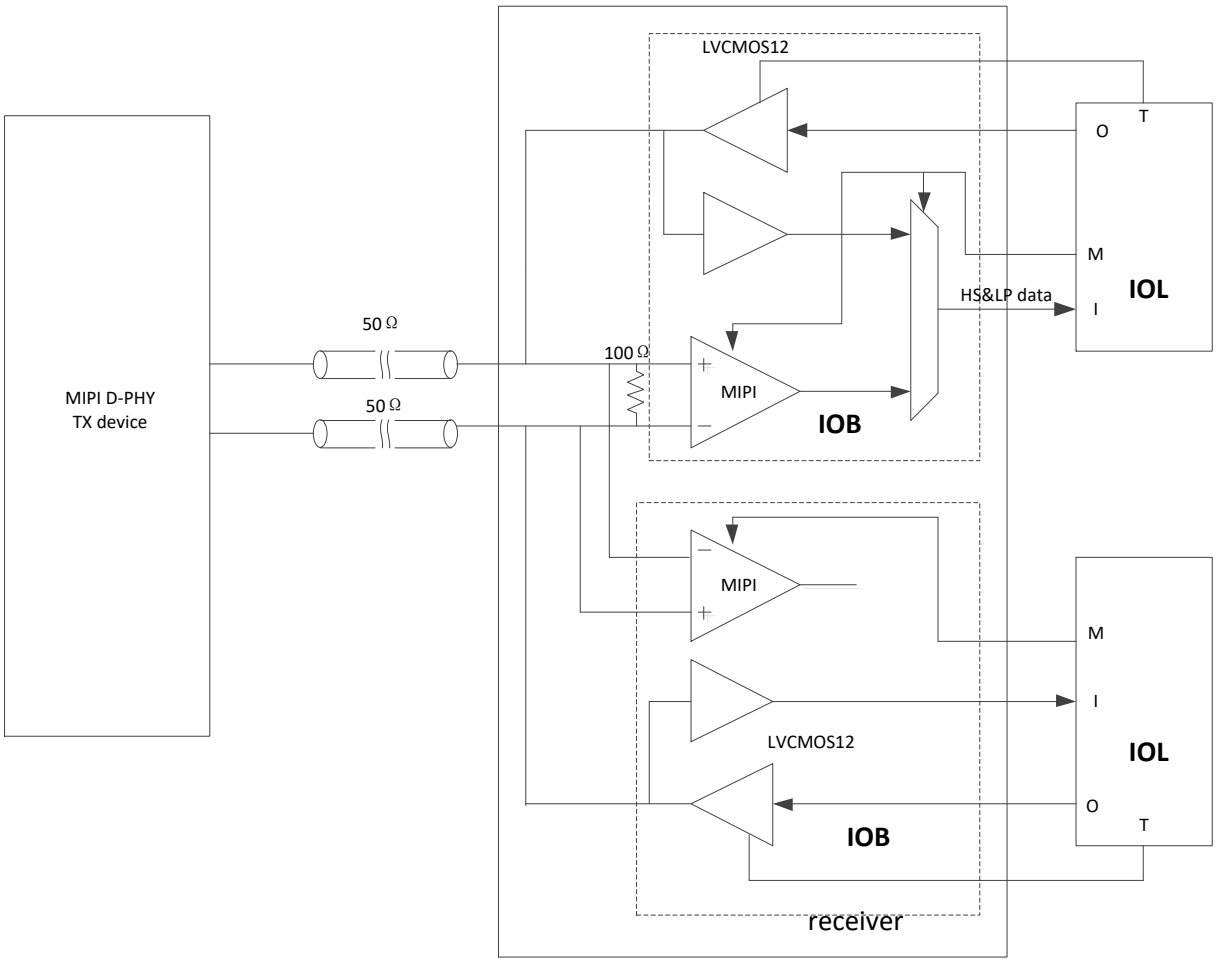


Figure 2-9 MIPI Input with 2 I/O Units (HS/LP)

2.2.11.3 Implement MIPI Output with 4 I/O Units

HS-MIPI output can be implemented with 2 I/O units using LVCMOS25D and external resistors; LP-MIPI output can be implemented using LVCMOS12 and 2 I/O units, as shown in the block diagram below.

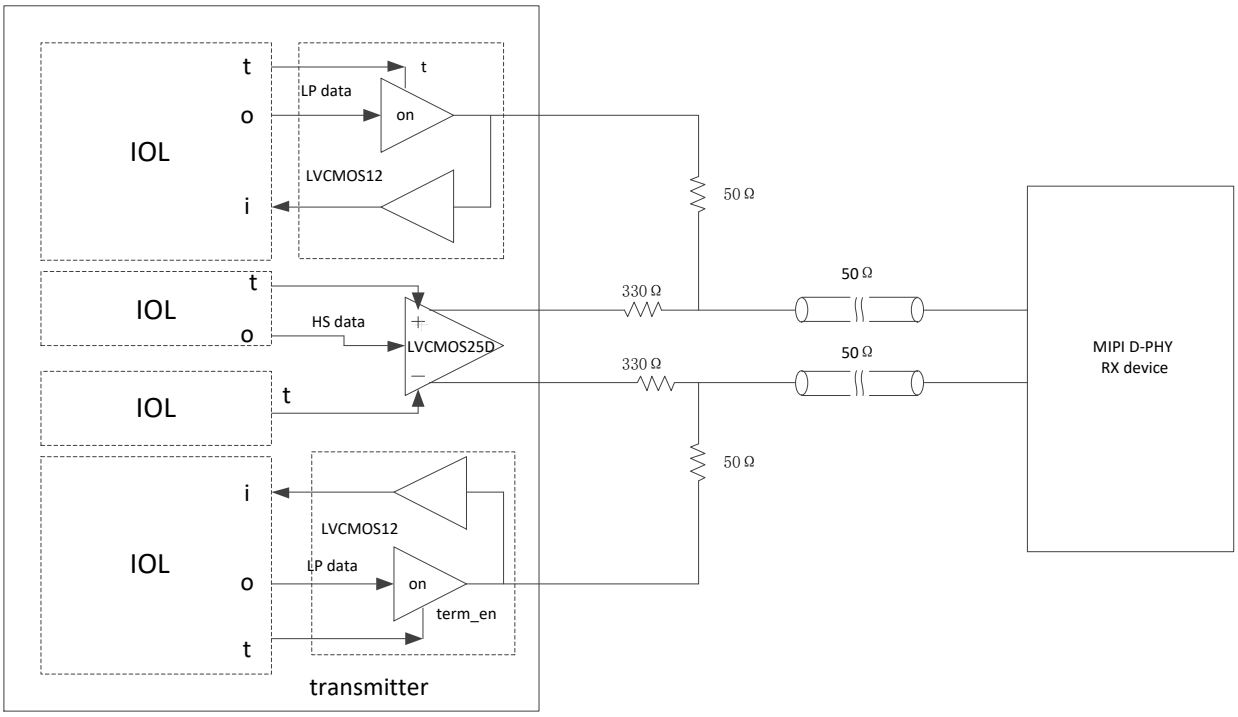


Figure 2-10 MIPI Output with 4 I/O Units (HS/LP)

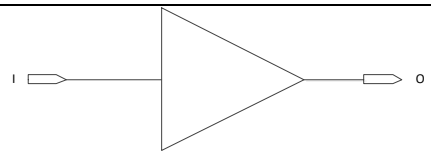
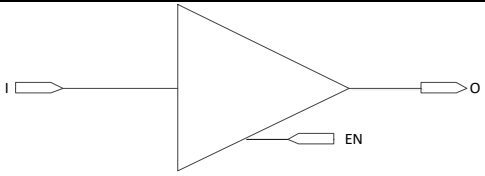
2.2.12 Basic Prototype of GTP for IO Buffer

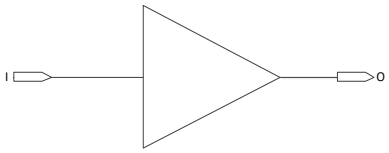
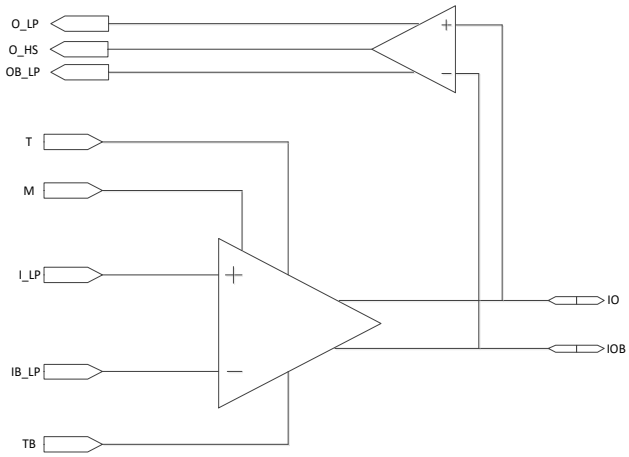
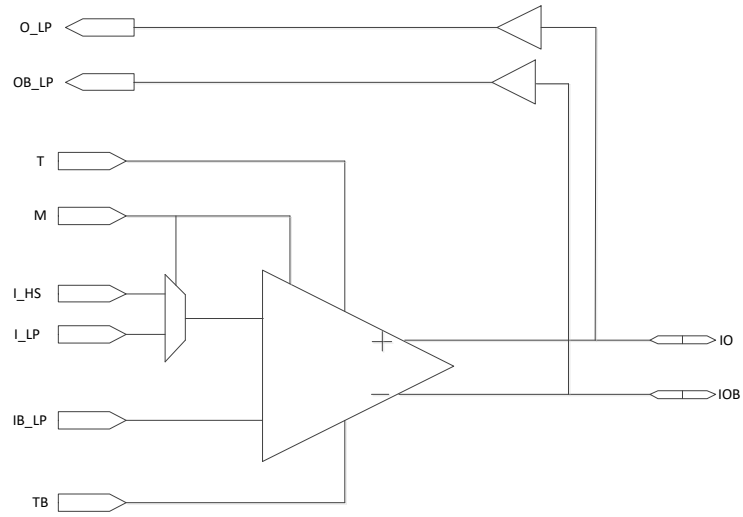
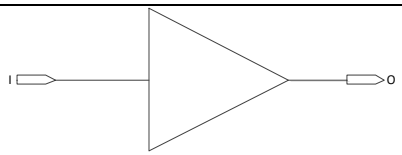
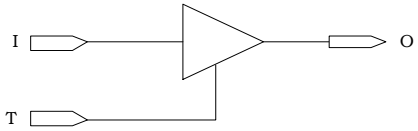
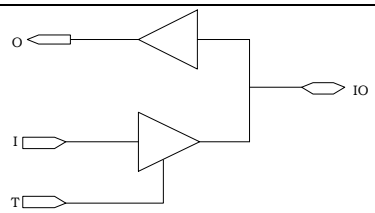
The PDS software library includes GTPs related to IO Buffer to support various I/O standards.

2.2.12.1 Common GTPs for Single-Ended I/O

The following GTPs are the most common in single-ended I/O standards.

Table 2-6 GTP for Single-Ended I/O

GTP Name	GTP Description	GTP Illustration
GTP_INBUF	Single-ended input signals must pass through INBUF	
GTP_INBUFE	Single-ended input buffer with enable control signal	

GTP Name	GTP Description	GTP Illustration
GTP_INBUFG	INBUFG is identical to INBUF, typically used for transmitting single-ended clock signals	
GTP_IOBUF_RX_MIPI	Support MIPI DPHY high-speed (HS) input, as well as single-ended input/output under low-power mode (LP)	
GTP_IOBUF_TX_MIPI	Support MIPI DPHY tri-state output, including input/output under low-power mode (LP) and differential output under high-speed (HS) mode, with both modes switchable according to actual application	
GTP_OUTBUF	Support single-ended I/O signals	
GTP_OUTBUFT	Implement tri-state output	
GTP_IOBUF	Support single-ended bidirectional function	

- GTP_INBUF

Ports are described in the table below.

Table 2-7 GTP_INBUF Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from the input buffer to the fabric

Parameters are described in the table below.

Table 2-8 GTP_INBUF Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-9	Input I/O standard

The optional configuration attributes for the parameter are as indicated in the table below.

Table 2-9 GTP_INBUF Parameter Configuration List

IOSTANDARD
LVTTL33/ PCI33/ LVCMOS33/ LVCMOS25/ LVCMOS18/ LVCMOS15/ LVCMOS12

- GTP_INBUFG

Ports are described in the table below.

Table 2-10 GTP_INBUFG Port Description

Port	Direction	Function Description
I	Input	PAD signal input
O	Output	Buffer output to the fabric

Parameters are described in the table below.

Table 2-11 GTP_INBUFG Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-12	Input IO standard

The list of valid values for parameter configuration is as shown in the table below.

Table 2-12 GTP_INBUFG Valid Parameter Values

IOSTANDARD
LVCMOS33/ LVCMOS25/ LVCMOS18/ LVCMOS15/ LVCMOS12

- GTP_INBUFE

Ports are described in the table below.

Table 2-13 GTP_INBUFE Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from the input buffer to the fabric
EN	Input	Input buffer enable control signal; when set to 0, the input buffer is disabled

Parameters are described in the table below.

Table 2-14 GTP_INBUFE Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-15	Input I/O standard

The list of valid values for parameter configuration is as shown in the table below.

Table 2-15 GTP_INBUFE Valid Parameter Values

IOSTANDARD
LVTTL33/ PCI33/ LVCMOS33/ LVCMOS25/ LVCMOS18/ LVCMOS15/ LVCMOS12

- GTP_OUTBUF

Ports are described in the table below.

Table 2-16 GTP_OUTBUF Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	buffer output

Parameters are described in the table below.

Table 2-17 GTP_OUTBUF Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-18	Input I/O standard
SLEW_RATE	string	"SLOW", "FAST"	Slew rate
DRIVE_STRENGTH	string	"2", "4", "6", "8", "12", "16"	Drive current strength

The list of valid values for parameters is as shown in the table below.

Table 2-18 GTP_OUTBUF Valid Parameter Values

GTP_OUTBUF		
IOSTANDARD	**SLEW_RATE**	**DRIVE_STRENGTH**
LVTTL33	FAST/SLOW	"4", "8", "12", "16"
PCI33	FAST/SLOW	
LVCMOS33	FAST/SLOW	
LVCMOS25	FAST/SLOW	

LVCMOS18	FAST/SLOW	"4", "8", "12"
LVCMOS15	FAST/SLOW	"4", "8",
LVCMOS12	FAST/SLOW	"2", "6"

- GTP_IOBUF_RX_MIPI

Ports are described in the table below.

Table 2-19 GTP_IOBUF_RX_MIPI Port Description

Port	Direction	Function Description
I_LP	Input	The input signal for the single-ended output buffer from "fabric" in LP mode
IB_LP	Input	The input signal for the single-ended output buffer from "fabric" in LP mode
M	Input	Mode selection signal. 1: HS mode, differential input; 0: LP mode, single-ended input. From fabric
T	Input	Single-ended output enable signal; when it is 0, IO serves as output, and when it is 1, IO serves as input
TB	Input	Single-ended output enable signal; when it is 0, IOB serves as output, and when it is 1, IOB serves as input
O_HS	Output	Differential output (HS) to fabric
O_LP	Output	Single-ended output (LP)
OB_LP	Output	Single-ended output (LP)
IO	Bi-Directional	P side differential input (HS mode), or single-ended input and output (LP mode)
IOB	Bi-Directional	N side differential input (HS mode), or single-ended input and output (LP mode)

Parameters are described in the table below.

Table 2-20 GTP_IOBUF_RX_MIPI Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	"MIPI"，"DEFAULT"	Input I/O standard, VCCIO=1.2V
DRIVE_STRENGTH	string	"2"，"6"	Drive current strength
SLEW_RATE	string	"SLOW"，"FAST"	Slew rate
TERM_DIFF	string	"ON"，"OFF"	Internal terminal matching resistor enabled or disabled

- GTP_OUTBUFT

Ports are described in the table below.

Table 2-21 GTP_OUTBUFT Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	buffer output
T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port

Parameters are described in the table below.

Table 2-22 GTP_OUTBUFT Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-23	Input I/O standard
SLEW_RATE	string	"SLOW"，"FAST"	Slew rate
DRIVE_STRENGTH	string	"2", "4", "6", "8", "12", "16"	Drive current strength

The list of valid values for parameters is as shown in the table below.

Table 2-23 GTP_OUTBUFT Valid Parameter Values

GTP_OUTBUFT		
IOSTANDARD	**SLEW_RATE**	**DRIVE_STRENGTH**
LVTTL33	FAST/SLOW	"4", "8", "12", "16"
PCI33	FAST/SLOW	
LVCMOS33	FAST/SLOW	
LVCMOS25	FAST/SLOW	
LVCMOS18	FAST/SLOW	"4", "8", "12"
LVCMOS15	FAST/SLOW	"4", "8"
LVCMOS12	FAST/SLOW	"2", "6"

- GTP_IOBUF_TX_MIPI

Ports are described in the table below.

Table2-24 GTP_IOBUF_TX_MIPI Port Description

Port	Direction	Function Description
I_HS	Input	The input signal for the differential output buffer from IO Logic
I_LP	Input	The input signal for the single-ended output buffer from IO Logic in LP mode
IB_LP	Input	The input signal for the single-ended output buffer from IO Logic in LP mode
M	Input	Mode selection signal. 1: HS mode, differential input; 0: LP mode, single-ended input and output. From IO Logic
T	Input	Differential and single-ended output enable signal
TB	Input	Single-ended output enable signal
O_LP	Output	Single-ended output (LP)
OB_LP	Output	Single-ended output (LP)
IO	Bi-Directional	P-side differential output or input
IOB	Bi-Directional	N-side differential output or input

Parameters are described in the table below.

Table2-25 GTP_IOBUF_TX_MIPI Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	"DEFAULT","MIPI"	Input I/O standard, VCCIO=1.2V
DRIVE_STRENGTH	string	"2"，"6"	Drive current strength

Parameter Name	Parameter Type	Valid Values	Function Description
SLEW_RATE	string	"SLOW"，"FAST"	Slew rate
TERM_DIFF	string	"ON"，"OFF"	Internal terminal matching resistor enabled or disabled

- GTP_IOBUF

  Ports are described in the table below.

Table 2-26 GTP_IOBUF Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from the input buffer to the fabric
T	Input	Tristate enable; when T=1, IO is an input; when T=0, IO is an output
IO	Bi-Directional	PAD

Parameters are described in the table below.

Table 2-27 GTP_IOBUF Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-28	Input IO standard
SLEW_RATE	string	"SLOW", "FAST"	Slew rate
DRIVE_STRENGTH	string	"2", "4", "6", "8", "12", "16"	Drive current strength

The list of valid values for parameters is as shown in the table below.

Table 2-28 GTP_IOBUF Valid Parameter Values

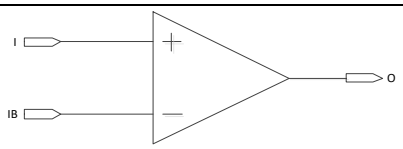
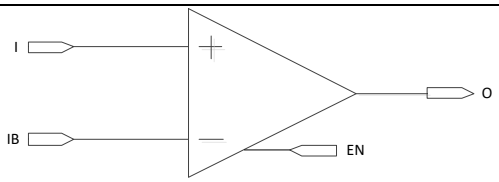
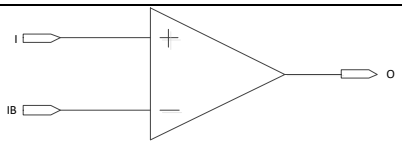
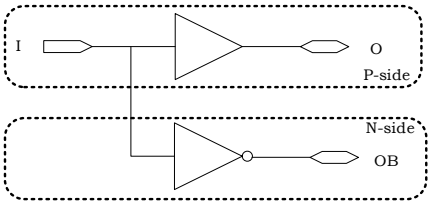
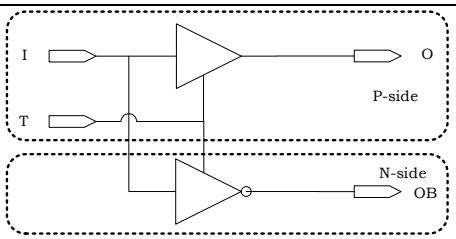
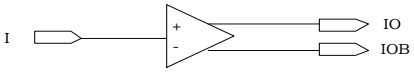
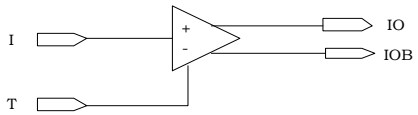
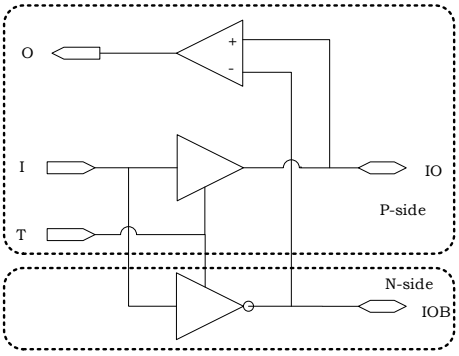
GTP_IOBUF		
IOSTANDARD	**SLEW_RATE**	**DRIVE_STRENGTH**
LVTTL33	FAST/SLOW	"4", "8", "12", "16"
PCI33	FAST/SLOW	
LVCMOS33	FAST/SLOW	
LVCMOS25	FAST/SLOW	
LVCMOS18	FAST/SLOW	"4", "8", "12"
LVCMOS15	FAST/SLOW	"4", "8"
LVCMOS12	FAST/SLOW	"2", "6"

2.2.12.2 Common GTPs for Differential I/O

The table below lists the most commonly used GTPs for differential I/O.

Table 2-29 GTPs for Differential I/O

GTP Name	Description	Illustration

GTP Name	Description	Illustration
GTP_INBUFDS	Supports differential input function. INBUFDS has 2 inputs: I and IB, representing the P-channel and N-channel input pins of the differential pair respectively	
GTP_INBUFEDS	Differential input buffer with enable control signal	
GTP_INBUFGDS	Differential clock input	
GTP_OUTBUFCO	Pseudo-differential output driving function	
GTP_OUTBUFTCO	Supports pseudo-differential output driving function and tri-state enable	
GTP_OUTBUFDS	True differential output function. Supported IO output standards are: "LVDS"	
GTP_OUTBUFTDS	True differential output function. Supported IO output standards are: "LVDS"	
GTP_IOBUFCO	Single-ended input and pseudo-differential output driving function	

- GTP_INBUFDS

  Ports are described in the table below.

Table 2-30 GTP_INBUFDS Port Description

Port	Direction	Function Description
I	Input	P-side differential input
IB	Input	N-side differential input
O	Output	Differential output to fabric

Parameters are described in the table below.

Table 2-31 GTP_INBUFDS Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-32	Input I/O standard
TERM_DIFF	string	"ON", "OFF"	Internal termination matching resistor enabled or disabled during differential input

The list of valid values for parameters is as shown in the table below.

Table 2-32 Valid GTP Parameter Values for Differential Input

IOSTANDARD
LVDS / LVPECL / BLVDS / LVCMOS33D / LVCMOS25D / DEFAULT

- GTP_INBUFEDS

  Ports are described in the table below.

Table 2-33 GTP_INBUFEDS Port Description

Port	Direction	Function Description
I	Input	P-side differential input
IB	Input	N-side differential input
O	Output	Differential output to fabric
EN	Input	Input buffer enable control signal, active high

Parameters are described in the table below.

Table 2-34 GTP_INBUFEDS Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-32	Input I/O standard
TERM_DIFF	string	"ON", "OFF"	Internal termination matching resistor enabled or disabled during differential input

- GTP_INBUFGDS

  Ports are described in the table below.

Table 2-35 GTP_INBUFGDS Port Description

Port	Direction	Function Description
I	Input	P-side differential input
IB	Input	N-side differential input
O	Output	Differential output to fabric

Parameters are described in the table below.

Table 2-36 GTP_INBUFGDS Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-32	Input I/O standard
TERM_DIFF	string	"ON", "OFF"	Internal termination matching resistor enabled or disabled during differential input

- GTP_OUTBUFCO

Ports are described in the table below.

Table 2-37 GTP_OUTBUFCO Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	P-side for pseudo-differential output
OB	Output	N-side for pseudo-differential output

Parameters are described in the table below.

Table 2-38 GTP_OUTBUFCO Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-39	Output I/O standard

The list of valid values for parameters is as shown in the table below.

Table 2-39 Valid GTP Parameter Values for Differential Output

IOSTANDARD
LVPECL / MLVDS / BLVDS / LVCMOS33D / LVCMOS25D / LVDS25E / DEFAULT

- GTP_OUTBUFTCO

Ports are described in the table below.

Table2-40 GTP_OUTBUFTCO Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	P-side for pseudo-differential output
OB	Output	N-side for pseudo-differential output

T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port

Parameters are described in the table below.

Table 2-41 GTP_OUTBUFTCO Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-39	Output I/O standard

- GTP_OUTBUFDS

Ports are described in the table below.

Table 2-42 GTP_OUTBUFDS Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	P-side for true differential output
OB	Output	N-side for true differential output

Parameters are described in the table below.

Table 2-43 GTP_OUTBUFDS Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	"LVDS"	Output I/O standard

- GTP_OUTBUFTDS

Ports are described in the table below.

Table 2-44 GTP_OUTBUFTDS Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	P-side for true differential output
OB	Output	N-side for true differential output
T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port

Parameters are described in the table below.

Table 2-45 GTP_OUTBUFTDS Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	"LVDS"	Output I/O standard

- GTP_IOBUFCO

Ports are described in the table below.

Table 2-46 GTP_IOBUFCO Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from the input buffer to the fabric
T	Input	Tri-state enable; when T=1, IO and IOB act as differential inputs; when T=0, IO and IOB act as pseudo-differential outputs
IO	Bi-Directional	P-side for differential signal
IOB	Bi-Directional	N-side for differential signal

Parameters are described in the table below.

Table 2-47 GTP_IOBUFCO Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-39	I/O Std
TERM_DDR	string	"ON", "OFF"	Internal terminal matching resistor enabled or disabled

2.3 IO Logic

IO Logic manages whether the IO Buffer outputs or receives signals from CPLDs pins. IO Logic includes input registers, output registers, and tri-state registers and supports functions such as IDDR and ODDR.

2.3.1 Input Register

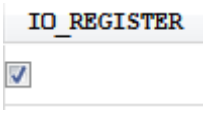
Input registers support the following functions:

- Two types of transmission modes: SDR and DDR, where SDR supports flip-flops and latches
- Synchronous/asynchronous reset/set operations
- Clock gating with asynchronous reset
- Clock polarity select
- Reset/set polarity select
- Dynamic and static clock enable
- Bypass input registers for direct input
- MIPI input (HS and LP)

Input register SDR flip-flop mode can be implemented through Verilog/VHDL code, taking Verilog as an example:

```
always @ (posedge CLK)
Q1 <= D;
```

Also, the "IO_REGISTER" attribute of the input IO shall be selected in [UCE > Device > I/O]:



Timing diagram for input register SDR flip-flop mode:

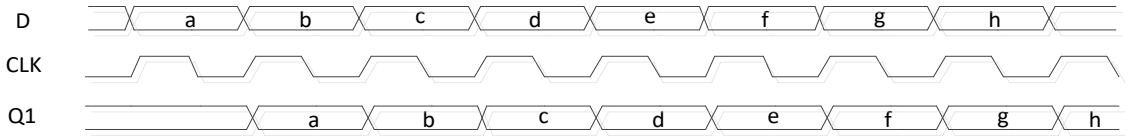


Figure 2-11 Timing Diagram for Input Register SDR Flip-Flop Mode

Input register SDR latch mode can be implemented through Verilog/VHDL code, taking Verilog as an example:

```
always @ (*)
Q1 = D;
```

Also, the "IO_REGISTER" attribute of the IO needs to be selected.

Timing diagram for input register SDR latch mode:

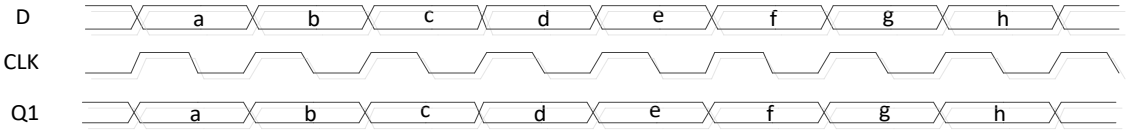


Figure 2-12 Timing Diagram for Input Register SDR Latch Mode

The DDR mode of the input register can be implemented through the dedicated primitive GTP_IDDR provided by the PDS software library, with instantiation as shown below.

```
GTP_IDDR #
(
.GRS_EN        ("TRUE"        ),    //"TRUE","FALSE"
.RS_TYPE       ("ASYNC_SET")
//"SYNC_SET","ASYNC_SET","SYNC_RESET","ASYNC_RESET"
) gtp_iddr_inst (
.D             ( d            ),
.CE            ( ce           ),
.RS            ( rs           ),
.CLK           ( clk          ),
.Q0            ( q0           ),
.Q1            ( q1           )
);
```

The parameters for GTP_IDDR are described in the table below.

Table 2-48 GTP_IDDR Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
GRS_EN	string	"TRUE","FALSE"	Global reset enable; "TRUE" indicates valid
RS_TYPE	string	"SYNC_SET", "ASYNC_SET", "SYNC_RESET", "ASYNC_RESET"	Reset/Set mode select

The signals for GTP_IDDR are described in the table below.

Table 2-49 GTP_IDDR Signal Description

Signal Name	Direction	Width	Function Description
D	Input	1	Input data port
CE	Input	1	Clock enable signal, active high
RS	Input	1	Set/reset signal, active high
CLK	Input	1	System clock
Q0	Output	1	Deserializer data output
Q1	Output	1	Deserializer data output

Timing diagram for input register DDR mode (IDDR):

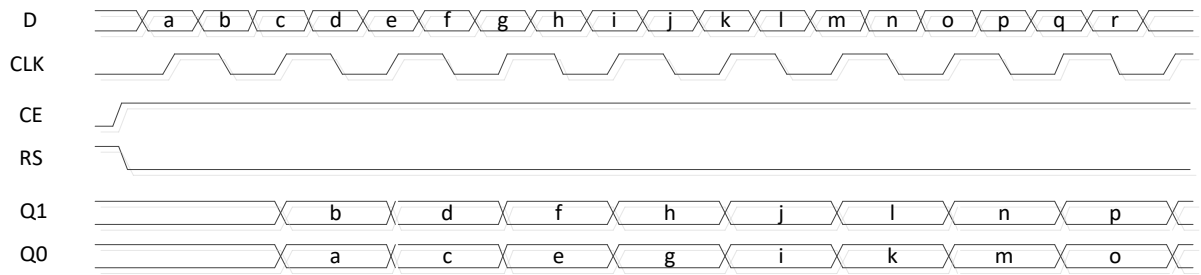


Figure 2-13 GTP_IDDR (IDDR) Timing Diagram

2.3.2 Output Register

Output registers support the following functions:

- SDR and DDR modes
- Synchronous/asynchronous reset/set operations
- Clock gating with asynchronous reset
- Clock polarity select
- Reset/set polarity select
- Dynamic and static clock enable
- Bypass output registers for direct output
- MIPI output (HS and LP)

Output register SDR flip-flop mode can be implemented through Verilog/VHDL code, taking Verilog as an example:

```
always @ (posedge CLK)
  Q <= D0;
```

Also, the "IO_REGISTER" attribute of the output IO needs to be selected.

Timing diagram for output register SDR flip-flop mode:

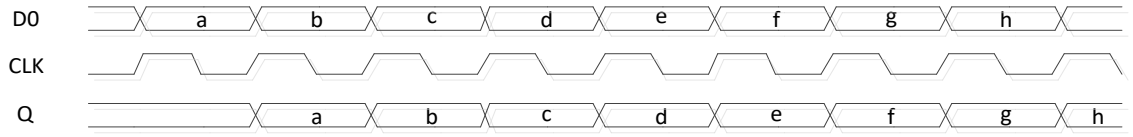


Figure 2-14 Timing Diagram for Output Register SDR Flip-Flop Mode

The DDR mode of the output register can be implemented through the dedicated primitive GTP_ODDR provided by the PDS software library, with instantiation as shown below.

```
GTP_ODDR #
(
      .GRS_EN       ("TRUE"          ),   //"TRUE","FALSE"
      .RS_TYPE      ("ASYNC_SET")
 //"SYNC_SET","ASYNC_SET","SYNC_RESET","ASYNC_RESET"
) gtp_oddr_inst (
.D0               ( d0               ),
.D1               ( d1               ),
.CE               ( ce               ),
.RS               ( rs               ),
.CLK              ( clk              ),
.Q                ( q                )
);
```

The parameters for GTP_ODDR are described in the table below.

Table 2-50 GTP_ODDR Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
GRS_EN	string	"TRUE","FALSE"	Global reset enable; "TRUE" indicates valid
RS_TYPE	string	"SYNC_SET", "ASYNC_SET", "SYNC_RESET", "ASYNC_RESET"	Reset/Set mode select

The signals for GTP_ODDR are described in the table below.

Table 2-51 GTP_ODDR Signal Description

Signal Name	Direction	Width	Function Description
D0	Input	1	Input data port
D1	Input	1	Input data port
CE	Input	1	Clock enable signal, active high
RS	Input	1	Set/reset signal, active high
CLK	Input	1	System clock
Q	Output	1	Serial data output

Timing diagram for output register DDR mode (ODDR):

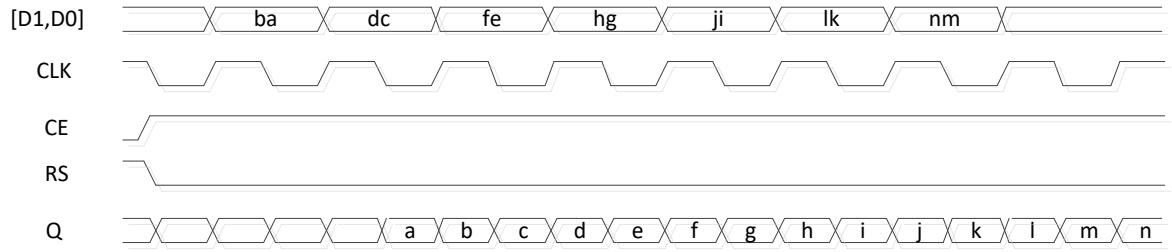


Figure 2-15 GTP_ODDR (ODDR) Timing Diagram

2.3.3 Tri-State Register

Tri-State registers support the following functions:

- SDR and DDR modes
- Synchronous/asynchronous reset/set operations
- Clock gating with asynchronous reset
- Clock polarity select
- Reset/set polarity select
- Dynamic and static clock enable
- Bypass output registers for direct output
- Pseudo-differential

The tri-state register SDR flip-flop mode can be implemented when instantiating GTP_OUTBUFT, GTP_OUTBUFTCO, or GTP_OUTBUFTDS, with the "IO_REGISTER" attribute selected for the corresponding I/O. Timing diagram for the tri-state register SDR flip-flop mode:

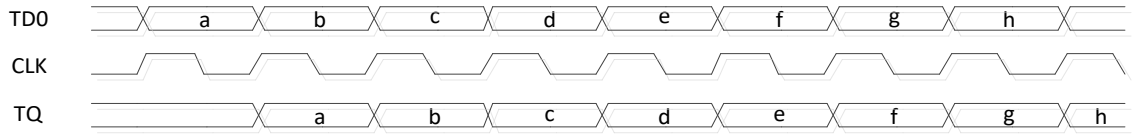


Figure 2-16 Timing Diagram for the Tri-State Register SDR Flip-Flop Mode

The tri-state register DDR mode can be implemented by invoking GTP_ODDR; PDS software will map D1 and D0 to TD1 and TD0 respectively, and map Q to TD in the underlying circuit based on the actual situation. Timing diagram for the tri-state register DDR mode:

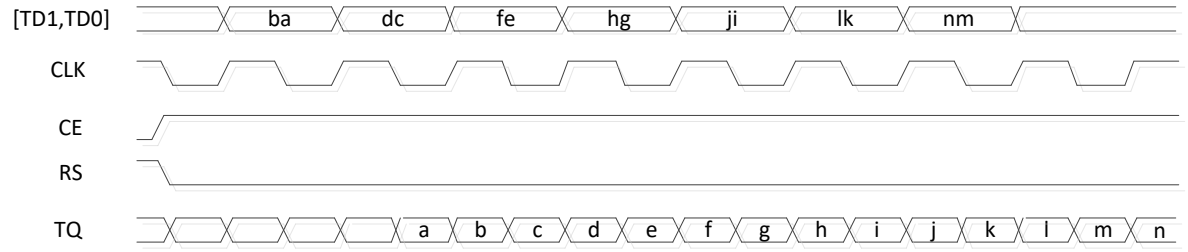


Figure 2-17 Timing Diagram for the Tri-State Register DDR Mode

2.3.4 I/O Input/Output Delay Module

Each I/O unit of the Compa Family CPLDs devices includes 1 I/O input/output delay module. There are two types of I/O input/output delay modules: IOLDLY and IOLDLYS. IOLDLY supports both dynamic and static input/output delay control and is located only in the I/O units on the bottom side (bank2) of the device; IOLDLYS only supports static delay configuration, located on the left side, right side, and top side of the device. The I/O input/output delay supports 32 steps of adjustment (0-31), each step being 100ps, thus the maximum delay provided can be 3100ps.

The PDS software library provides specialized primitives to facilitate users in using the I/O input/output delay modules, allowing users to instantiate the GTP_IODELAY_E1 prototype module within the source code (Verilog/VHDL) to implement input/output delay control function. The Verilog instantiation template is as follows.

```
GTP_IODELAY_E1 #
(
.DELAY_STEP_VALUE ( 5`h0                ),    // 5`h0 ~ 5`h1F
.DELAY_STEP_SEL     ("PARAMETER")     //"PARAMETER", "PORT"
) gtp_iodelay_e1_inst (
.DI                      ( di              ),
.DELAY_STEP          ( delay_step      ),
.DO                      ( do              )
);
```

The functional block diagram of GTP_IODELAY_E1 is shown in the figure below.

Figure 2-18 GTP_IODELAY_E1 Functional Block Diagram

The parameters for GTP_IODELAY_E1 are described in the table below.

Table 2-52 GTP_IODELAY_E1 Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
DELAY_UNIT	string	"110ps", "58ps"	Used to select the size of the delay step; the Compa product only supports "110ps"
DELAY_STEP_VALUE	integer	5'h0 ~ 5'h1F	Static delay control
DELAY_STEP_SEL	string	"PARAMETER" "PORT"	Selection of the delay control signal source: "PARAMETER" indicates static configuration, with delay passed through DELAY_STEP_VALUE "PORT" indicates dynamic configuration, with delay passed through DELAY_STEP

The signals for GTP_IODELAY_E1 are described in the table below.

Table 2-53 GTP_IODELAY_E1 Signal Description

Signal Name	Direction	Width	Function Description
DI	Input	1	Data input bus
DELAY_STEP	Input	5	Dynamic delay control
DO	Output	1	Data output bus

The distribution of IOLDLY units varies between devices.

Table 2-54 Outlines the distribution of IOLDLY units in Compa Family CPLDs devices.

Table 2-54 IOLDLY Unit Distribution in Compa Family CPLDs Devices

Device Name	Banks That Support Both Dynamic and Static Input Delays (IOLDLY)
PGC1K	Bank2
PGC2K	Bank2
PGC4K	Bank2
PGC7K	Bank2

Chapter 3 Implementation of High-Speed Data Transmission

High-speed data transmission can be implemented by the I/O units of Compa Family CPLDs devices used in conjunction with ISERDES/OSERDES. As a receiver, ISERDES supports the following functions:

IDES4(1:4)

IDES7(1:7)

IDES8(1:8)

Word alignment

As a transmitter, OSERDES supports the following functions:

OSER4(4:1)

OSER7(7:1)

OSER8(8:1)

3.1 High-Speed Data Reception Interface

3.1.1 Structure

The I/O units of Compa Family CPLDs devices are arranged in groups of 4, divided into A, B, C, and D. These 4 I/O units together with 1 ISERDES form a high-speed data reception interface. The connection block diagram of I/O units with ISERDES is shown in the figure below. PADA in the diagram corresponds to the odd pair differential pin P side in the packaging user guide, PADB corresponds to the odd pair differential pin N side, PADC corresponds to the even pair differential pin P side, and PADD corresponds to the even pair differential pin N side.

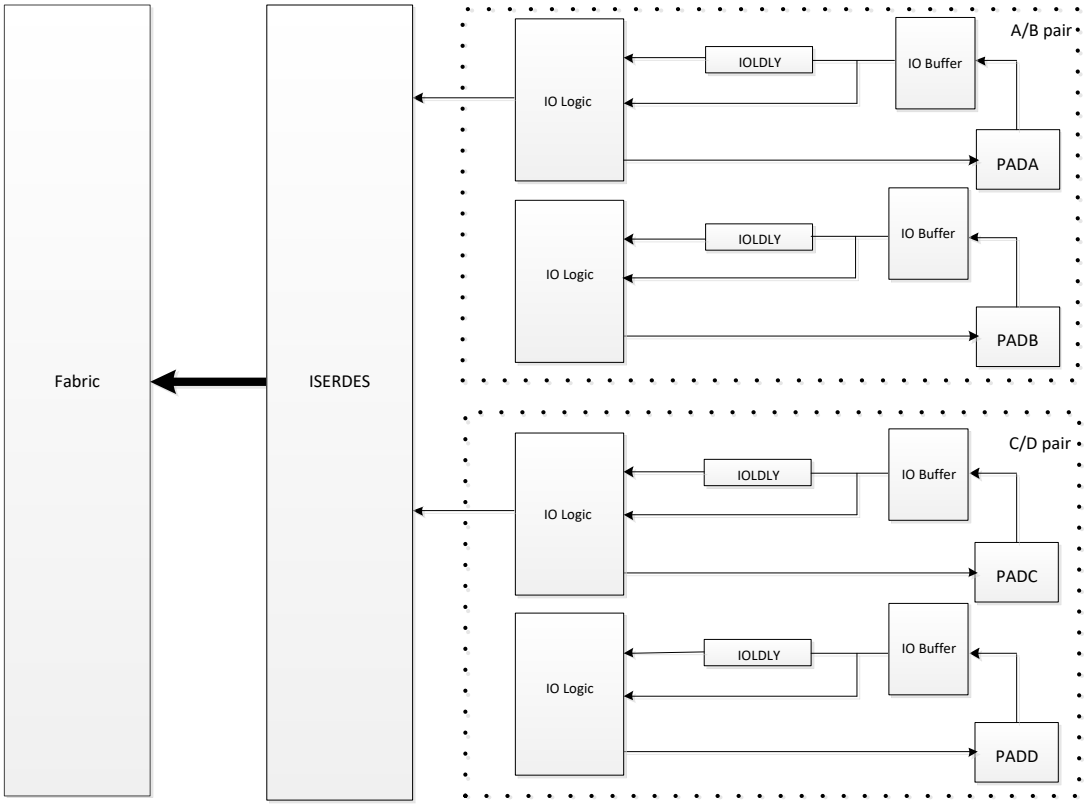


Figure 3-1 Connection Block Diagram of I/O Units with ISERDES

3.1.2 ISERDES

The PDS software library provides dedicated primitives for the convenience of users utilizing the ISERDES unit, allowing users to instantiate the GTP_ISERDES_E1 prototype module in the source code (Verilog/VHDL). Taking Verilog instantiation as an example:

```
GTP_ISERDES_E1 #
(
.ISERDES_MODE        ("IDES4"),    //"IDES4","IDES8","IDES7"
.GRS_EN              ("TRUE" )     //"TRUE","FALSE"
) gtp_iserdes_e1_inst    (
.DI                  ( di        ),
.ICLK                ( iclk      ),
.RCLK                ( rclk      ),
.ALIGNWD             ( alignwd),
.RST                 ( rst       ),
.DO                  ( do        )
);
```

The parameters for GTP_ISERDES_E1 are described in the table below.

Table 3-1 GTP_ISERDES_E1 Parameter Description

Parameter Name	Parameter Type	Valid Values	Function Description
GRS_EN	string	"TRUE","FALSE"	Global reset enable; "TRUE" indicates valid
ISERDES_MODE	string	"IDES4","IDES8", "IDES7"	Serial data deserialization mode

The signals for GTP_ISERDES_E1 are described in the table below.

Table 3-2 GTP_ISERDES_E1 Signal Description

Signal Name	Direction	Width	Function Description
DO	Output	8	In "IDES4" mode, DO [7:4] is the deserialized data for DIA, and DO [3:0] is the deserialized data for DIC In "IDES8" mode, DO [7:0] is the deserialized data for DIA In "IDES7" mode, DO [6:0] is the deserialized data for DIA
DI	Input	1	Serial input data of PADA
ICLK	Input	1	Serial data input clock of PADA
RCLK	Input	1	The deserialization clock for PADA from CLKDIVOUT of GTP_IOCLKDIV_E1
ALIGNWD	Input	1	PADA word alignment request signal, active high
RST	Input	1	PADA reset signal, active high

1 ISERDES can be implemented as 2 IDES4 or 1 IDES7 or 1 IDES8. When ISERDES is configured as IDES4, only I/O units A and C can be connected to ISERDES; when ISERDES is configured as IDES7 or IDES8, only I/O unit A can be connected. Depending on the application requirements, the functions of the 4 I/O units are as shown in the following table.

Table 3-3 Receiver I/O Functions

ISERDES Mode	I/O Unit A	I/O Unit B	I/O Unit C	I/O Unit D
IDES4	√		√	
IDES8	√			
IDES7	√			

Only the bottom Banks in CPLDs devices support ISERDES, and the distribution of ISERDES in different devices is illustrated in the table below.

Table 3-4 ISERDES Distribution for Different Devices

Device Name	Bank Supporting ISERDES
PGC1K	Bank2
PGC2K	Bank2
PGC4K	Bank2
PGC7K	Bank2

GTP_ISERDES_E1 is typically used in conjunction with GTP_INBUF, GTP_INBUFG, GTP_INBUFDS, and GTP_INBUFGDS. The following diagram illustrates the connection method of GTP_ISERDES_E1 with GTP_INBUFDS as an example.

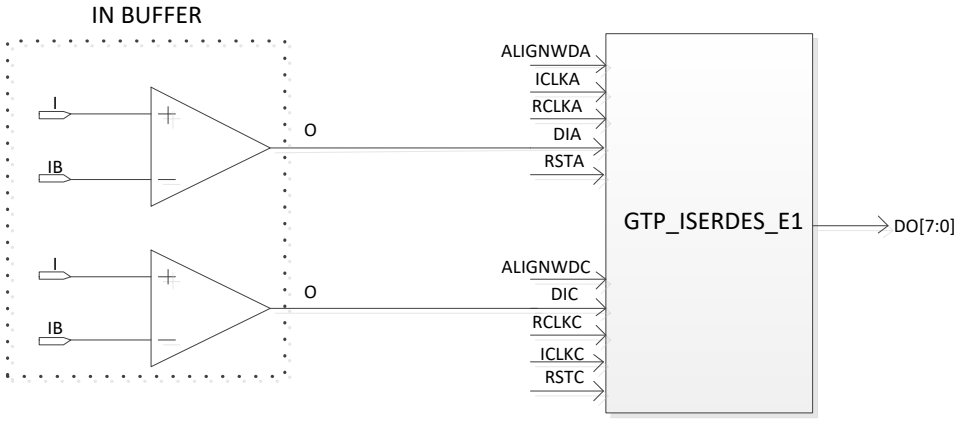


Figure 3-2 Common Connection Methods for GTP_ISERDES_E1

The following describes the different working modes of ISERDES, taking A/B pair as an example.

- IDES4

  When ISERDES is configured as IDES4, its function is as shown below.

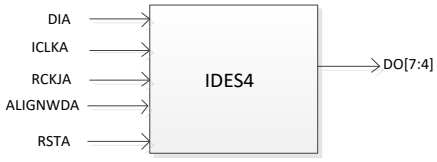


Figure 3-3 Block Diagram of IDES4

In IDES4 mode, while adjusting word boundaries, each ALIGNWDA request must remain high for at least 2 ICLKA cycles, with a minimum interval of 1 RCLKA cycle between 2 consecutive ALIGNWDA requests; ALIGNWDA and ICLKA can be asynchronous; after every 2 ALIGNWDA requests, the output data shifts by 2 bits; between 2 ALIGNWDA requests, there is an intermediate state for adjusting word boundaries, during which the output data is invalid. Once ICLKA captures the second ALIGNWDA request, the output data becomes valid after at most 4 more RCLKA cycles. The timing diagram for IDES4 is shown below.

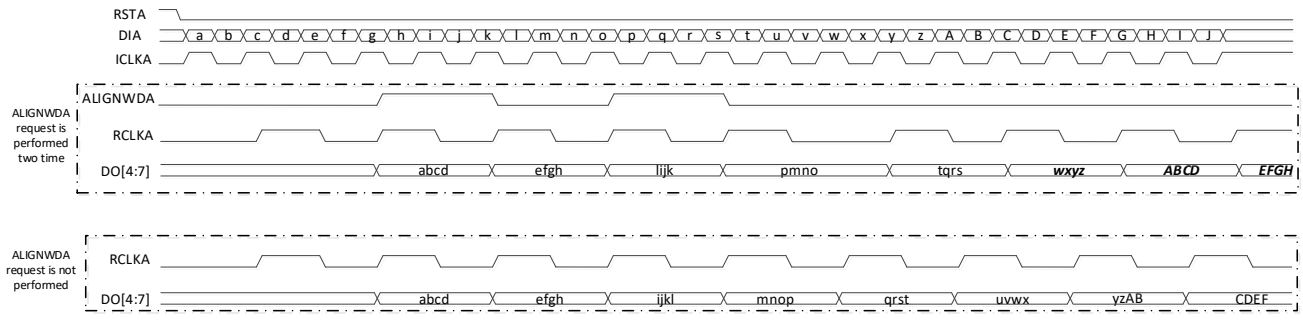


Figure 3-4 IDES4 Timing Diagram

- IDES7

When ISERDES is configured as IDES7, its function is as shown below.

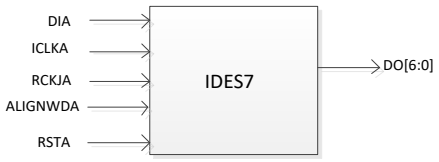


Figure 3-5 Functional Diagram of IDES7

In IDES7 mode, while adjusting word boundaries, the ALIGNWDA signal must remain high for at least 2 ICLKA cycles; ALIGNWDA and ICLKA can be asynchronous; to traverse all byte orders, up to 7 ALIGNWDA request signals are needed, with each request moving the data right by two bits. The timing diagram for IDES7 is shown in the figure below.

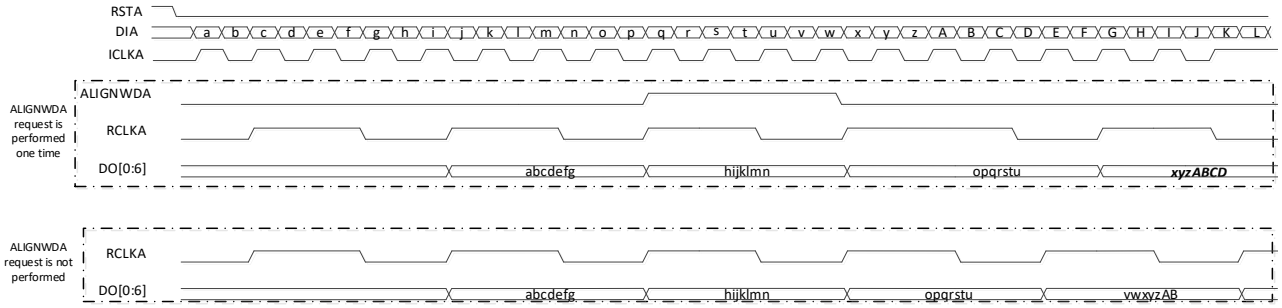


Figure 3-6 IDES7 Timing Diagram

- IDES8

When ISERDES is configured as IDES8, its function is as shown below.

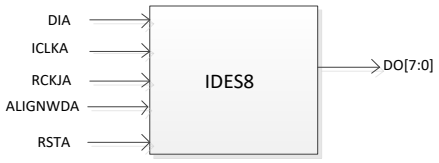


Figure 3-7 IDES8 Function Diagram

In IDES8 mode, when adjusting word boundaries, each ALIGNWDA request must remain high for at least 2 ICLKA cycles, with a minimum interval of 1 RCLKA cycle between 2 consecutive ALIGNWDA requests; ALIGNWDA and ICLKA can be asynchronous; after every 2 ALIGNWDA requests, the output data shifts by 2 bits; between 2 ALIGNWDA requests, there is an intermediate state for adjusting word boundaries, during which the output data is invalid. Once ICLKA captures the second ALIGNWDA request, the output data becomes valid

after at most 4 more RCLKA cycles. The timing diagram for IDES8 is shown in the figure below.

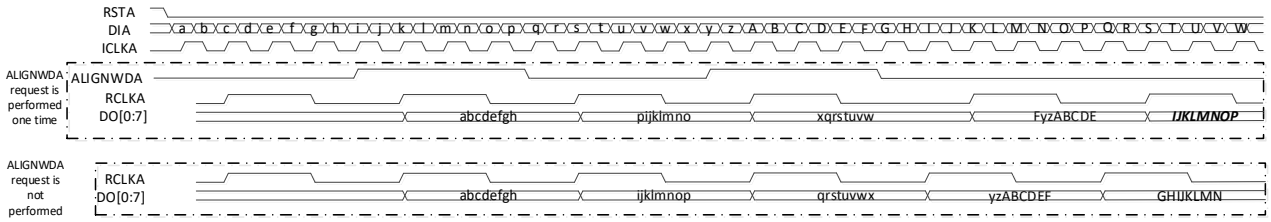


Figure 3-8 IDES8 Timing Diagram

3.2 High-Speed Data Transmission Interface

3.2.1 Structure

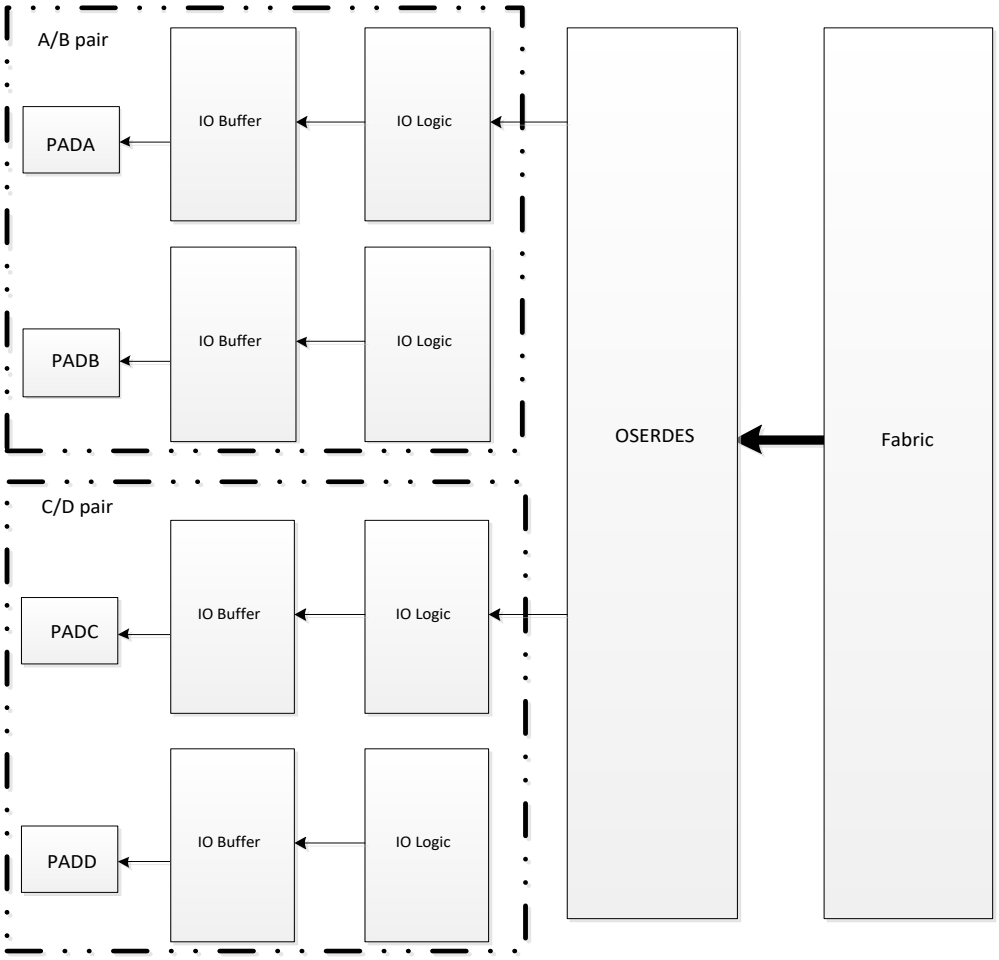


Figure 3-9 Connection Block Diagram of I/O Units with OSERDES

3.2.2 OSERDES

The PDS software library provides dedicated primitives for the convenience of users utilizing the OSERDES unit, allowing users to instantiate the GTP_OSERDES_E1 prototype module in the source code (Verilog/VHDL). Taking Verilog instantiation as an example:

```
GTP_OSERDES _E1#
(
.OSERDES_MODE     ("OSER4"),    //"OSER4","OSER8","OSER7"
.GRS_EN                ("TRUE" )     //"TRUE","FALSE"
) gtp_oserdes_e1_inst (
.DI                        ( di          ),
.OCLK                     ( oclk       ),
.RCLK                     ( rclk      ),
.RST                      ( rst         ),
.DO                       ( do          )
);
```

The parameters for GTP_OSERDES_E1 are described in the table below.

Table 3-5 GTP_OSERDES_E1 Parameter Description

Parameter Name	**Parameter Type**	**Valid Values**	**Function Description**
GRS_EN	string	"TRUE","FALSE"	Global reset enable; "TRUE" indicates valid
OSERDES_MODE	string	"OSER4","OSER8", "OSER7"	Parallel data serialization mode

The signals for GTP_OSERDES_E1 are described in the table below.

Table 3-6 GTP_OSERDES_E1 Signal Description

Signal Name	**Direction**	**Width**	**Function Description**
DI	Input	8	Parallel input data In "OSER4" mode, DI[3:0] are valid In "OSER8" mode, DI[7:0] are fully valid In "OSER7" mode, DI[6:0] are valid
DO	Output	1	In "OSER4" mode, DOA is the serial data for DI[3:0] In "OSER8" mode, DOA is the serial data for DI[7:0] In "OSER7" mode, DOA is the serial data for DI[6:0]
OCLK	Input	1	Serial data output clock of PADA
RCLK	Input	1	Parallel data input clock of PADA
RST	Input	1	PADA reset signal, active high

1 OSERDES can be implemented as 2 OSER4s, 1 OSER7, or 1 OSER8. When OSERDES is configured as OSER4, only A and C of the four I/O units can be connected to OSERDES; when OSERDES is configured as OSER7 or OSER8, only A can be connected. Depending on the application requirements, the functions of the 4 I/O units are as shown in the following table.

Table 3-7 Transmitter I/O Functions

OSERDES Mode	**I/O Unit A**	**I/O Unit B**	**I/O Unit C**	**I/O Unit D**
OSER4	√		√	
OSER8	√			
OSER7	√			

Only the top Banks in CPLDs device support OSERDES, and the distribution of OSERDES in different devices is shown in the table below.

Table 3-8 OSERDES Distribution for Different Devices

Device Name	**Bank Supporting OSERDES**
PGC1K	Bank0
PGC2K	Bank0
PGC4K	Bank0
PGC7K	Bank0

GTP_OSERDES_E1 is typically used in conjunction with GTP_OUTBUF, GTP_OUTBUFDS, GTP_OUTBUFCO, GTP_OUTBUFTCO, GTP_OUTBUFTDS, and GTP_OUTBUFT. The diagram below takes GTP_OUTBUFDS as an example to illustrate the connection relationship with GTP_OSERDES_E1.

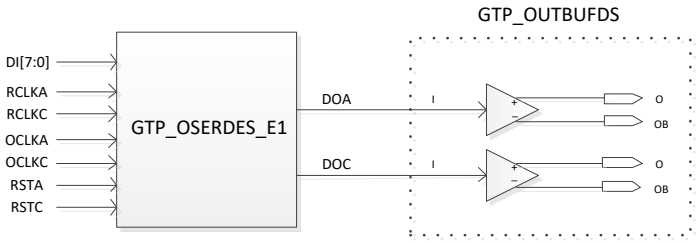


Figure 3-10 Common Connection Method of GTP_OSERDES_E1

The following describes the different working modes of OSERDES, taking A/B pair as an example.

- OSER4

  When OSERDES is configured as OSER4 mode, its functional diagram is as shown below.

Figure 3-11 OSER4 Functional Diagram

OSER4 Timing Diagram is as shown in the following figure.

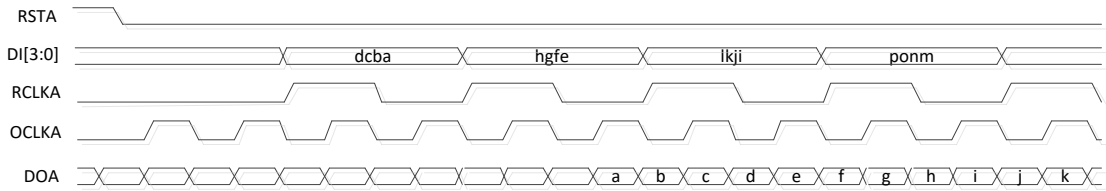


Figure 3-12 OSER4 Timing Diagram

- OSER7

  When OSERDES is configured as OSER7 mode, its functional diagram is as shown below.

Figure 3-13 OSER7 Functional Block Diagram

OSER7 Timing Diagram is shown in the figure below.

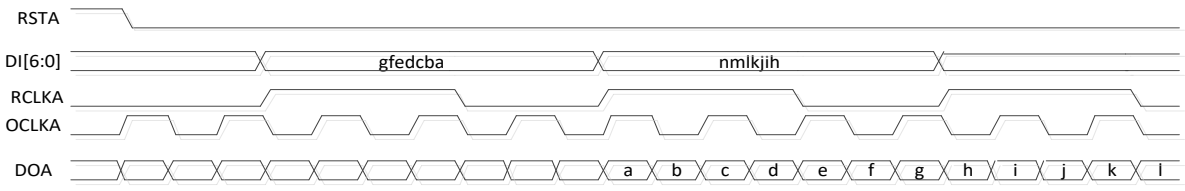


Figure 3-14 OSER7 Timing Diagram

- OSER8

When OSERDES is configured as OSER8 mode, its functional diagram is as shown below.

Figure 3-15 OSER8 Functional Block Diagram

OSER8 Timing Diagram is shown in the figure below.

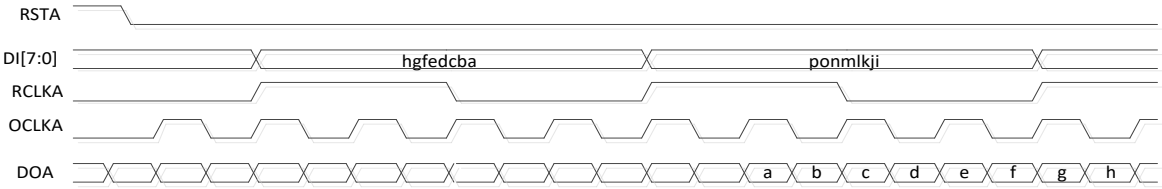


Figure 3-16 OSER8 Timing Diagram

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