Logos Family FPGAs Input/Output Interface (IO) User Guide

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.8	29.07.2022	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
OD	Over Drive
UD	Under Drive

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Chapter 1 Overview of I/O Unit

The Logos Family programmable logic devices feature configurable high-performance I/O drivers and receivers and support various standard interfaces.

The I/O units of Logos Family products mainly consist of IO BUFFER and IO LOGIC, typically distributed in pairs, with the structural diagram as follows:

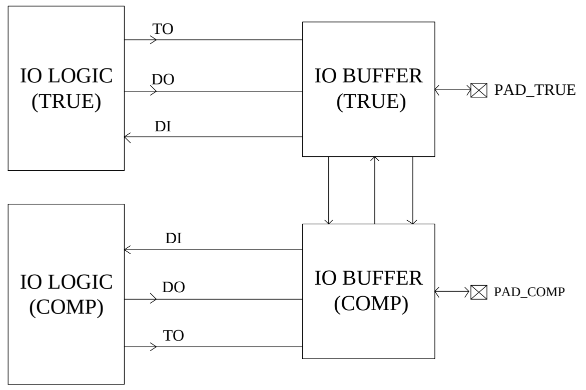


Figure 1-1 I/O Structural Diagram

Each IO BUFFER is directly connected to an IO LOGIC, which includes data input and output, as well as the tri-state control signal of the IO BUFFER. IO LOGIC can be configured as either ISERDES or OSERDES.

The single-ended I/O standards supported by the Logos Family products include LVCMOS, LVTTL, SSTL, and HSTL.

The differential I/O standards supported by the Logos Family products include LVDS, Sub-LVDS, Mini-LVDS, SLVS, RSDS, PPDS, BLVDS, MLVDS, TMDS, and LVPECL.

The I/O unit of Logos Family products features electrostatic discharge protection to prevent device pins from electrostatic damage.

Chapter 2 Detailed Introduction to I/O Unit

2.1 Logos Family I/O BANK

2.1.1 I/O BANK Arrangement

The I/O unit of Logos Family products is arranged by BANK.

PGL22G has 6 BANKs, arranged as shown in the following diagram.

Figure 2-1 Top View of PGL22G I/O BANK Arrangement

BANKL1, BANKL2, BANKR1, and BANKR2 support DDR interfaces.

PGL12G has 4 BANKs, arranged as shown in the following diagram.

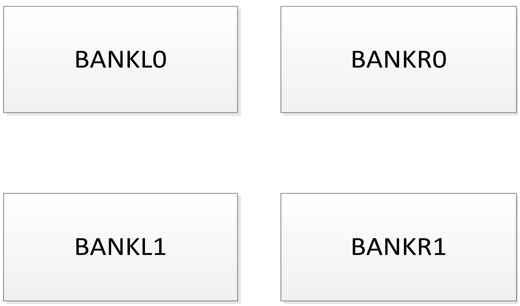


Figure 2-2 Top View of PGL12G I/O BANK Arrangement

PGL25G, PGL50G, and PGL50H are divided into 4 BANKs on the top, bottom, left, and right respectively, as shown in the following diagram.

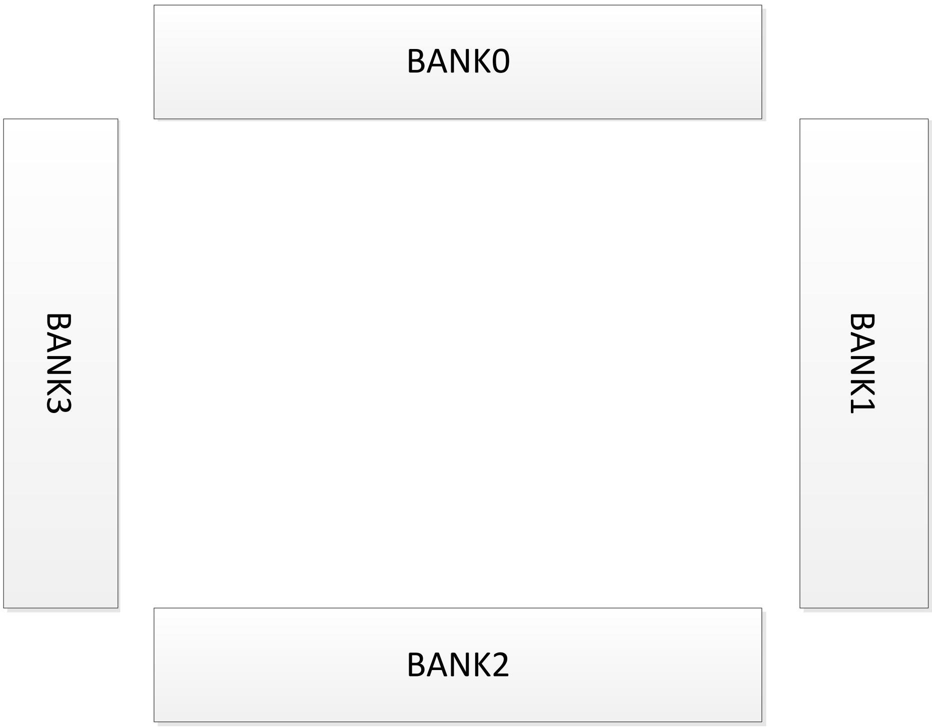


Figure 2-3 Top View of PGL25G, PGL50G, and PGL50H I/O BANK Arrangement

PGL100H is divided into 6 BANKs on the top, bottom, left, and right, as shown in the following diagram.

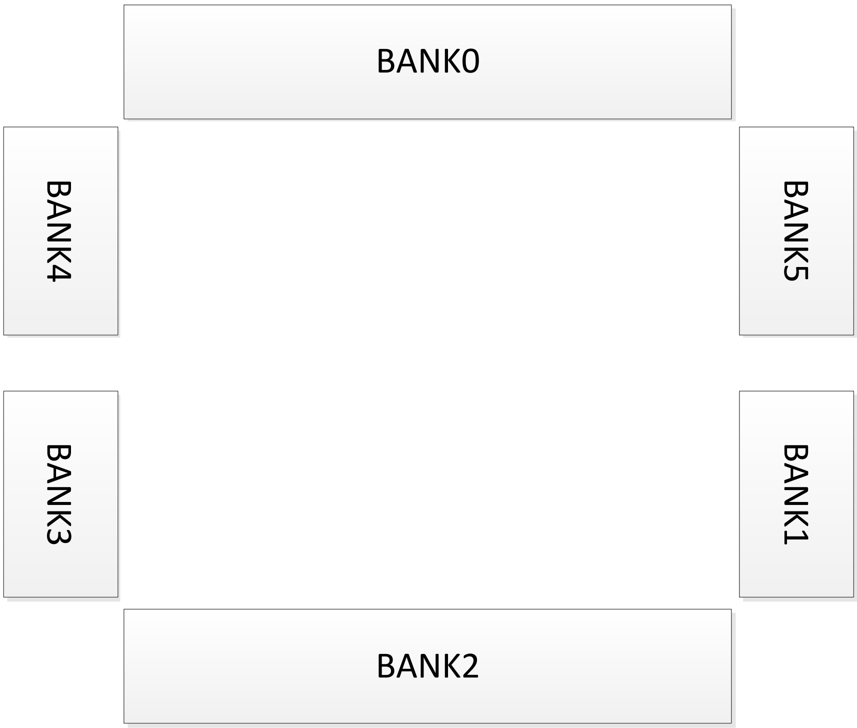


Figure 2-4 Top View of PGL100H Arrangement

For the PGL12G and PGL22G download banks, a voltage of 3.3V is recommended.

2.1.2 I/O BANK Voltage

For the Logos Family products, the I/O standards used within the BANK is limited; the voltage of the output standards must match VCCIO. Logos products have built-in dedicated circuits that allow input standards to be compatible with different VCCIOs to a certain extent. For the input-output combination modes for mixed voltage LVCMOS standard within the BANK, see the following table:

Table 2-1 Input-Output Combination Modes for Mixed-Voltage LVCMOS Standard Within BANK

VCCIO (V)	**Input (V)**					**Output (V)**				
	1.2	**1.5**	**1.8**	**2.5**	**3.3**	**1.2**	**1.5**	**1.8**	**2.5**	**3.3**
1.2	√					√				
1.5	√	√					√			
1.8	√	√	√					√		
2.5	√	√	√	√					√	
3.3	√	√	√	√	√					√

For any I/O standard used within a BANK, its VCCIO level must adhere to limitations, which will be checked by the Pango Design Suite software.

2.2 IO BUFFER

Logos Family products all feature configurable high-performance I/O drivers and receivers and support a variety of I/O standards. It allows programmatically setting of output drive current, slew rate, and on-die termination resistance.

2.2.1 IO BUFFER Structure

Each IO BUFFER includes input, output, and trifv-state I/O drivers. These drivers can be configured to various types of I/O standards. There are three golden models of IO BUFFER.

- IOBSHR (IOBS)

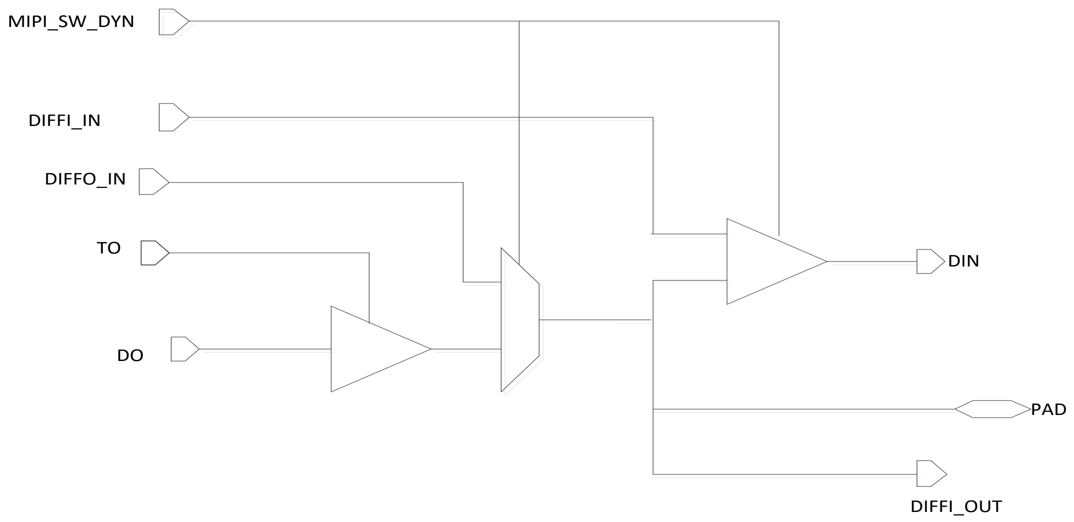


Figure 2-5 IO BUFFER Golden Model (IOBSHR)

IOBSHR supports all single-ended I/O standards, differential inputs, as well as dynamic switching between high-speed and low-speed MIPI data transfers.

- IOBDHR (IOBD)

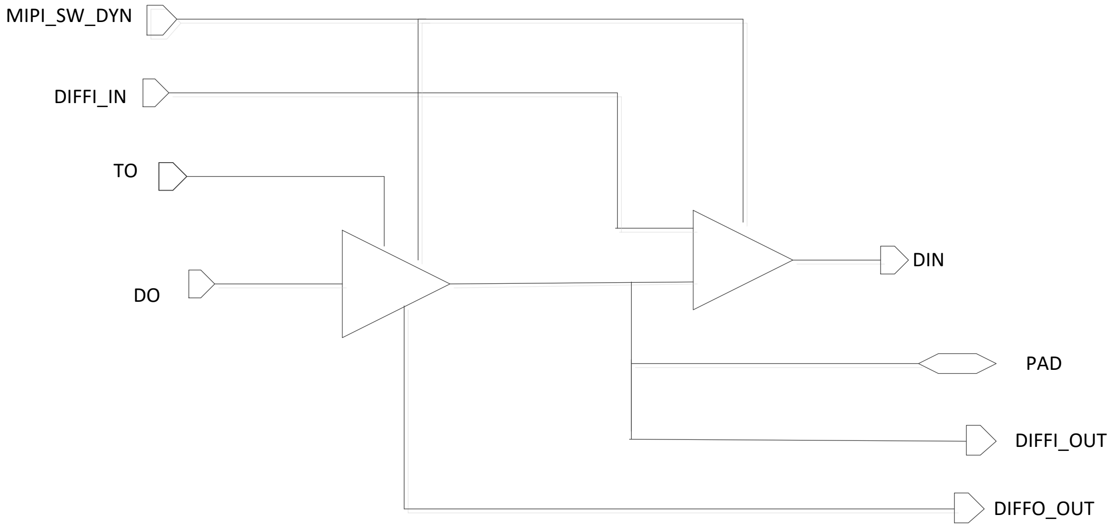


Figure 2-6 IO BUFFER Golden Model (IOBDHR)

In addition to the functions of IOBSHR, IOBDHR also supports true differential outputs.

- IOBRHR (IOBR)

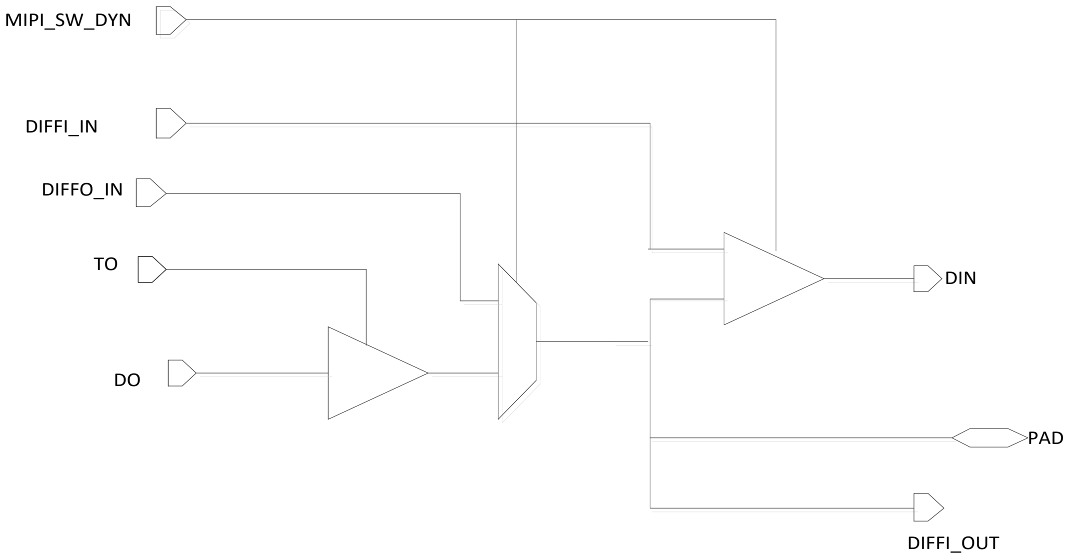


Figure 2-7 IO BUFFER Golden Model (IOBRHR)

In addition to the functions of IOBSHR, IOBRHR also supports DDR external reference voltage input.

Differential I/O is implemented using two IO BUFFERs. One IOBD and one IOBS or IOBR forms an IOB pair. The PAD corresponding to IOBD serves as TRUE, and the PAD to IOBS and IOBR serves as COMP; TRUE and COMP are combined together to transmit the differential output signal.

2.2.2 Termination Matching Resistors

Termination matching resistors are commonly used to meet signal integrity requirements when using high-speed I/O standards. Termination matching resistors should be placed as close to the receiver as possible to minimize interference with signal integrity.

For Logos Family FPGAs, terminal resistors are provided for differential interfaces (such as LVDS) and single-ended interfaces (such as SSTL). If terminal resistors are configured within the IO BUFFER, external terminal resistors are not needed.

- Termination Matching of Differential Signal:

Differential inputs use 100Ω parallel resistors. The following diagram shows the structure of external terminal resistors.

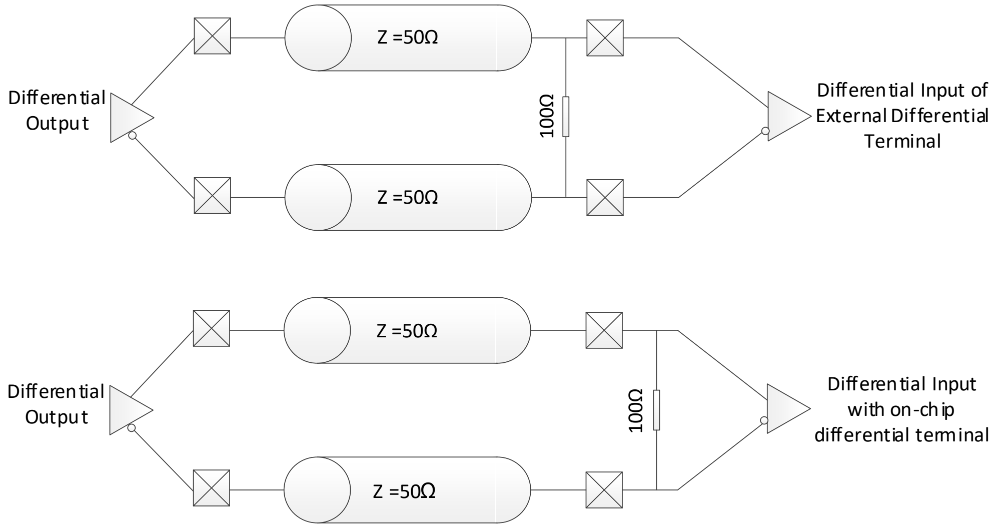


Figure 2-8 Matching Resistors for External Differential Signals on the Chip

Logos Family FPGAs offer optional on-chip differential terminations that can eliminate the need for 100Ω external terminal resistors. This type of on-chip differential terminal resistor is fully compatible with LVDS standards without any adjustment.

Optional on-chip differential terminations can be configured through I/O constraints. The diagram below presents different implementation methods using on-chip differential terminations or external terminal resistors at the differential receiver end.

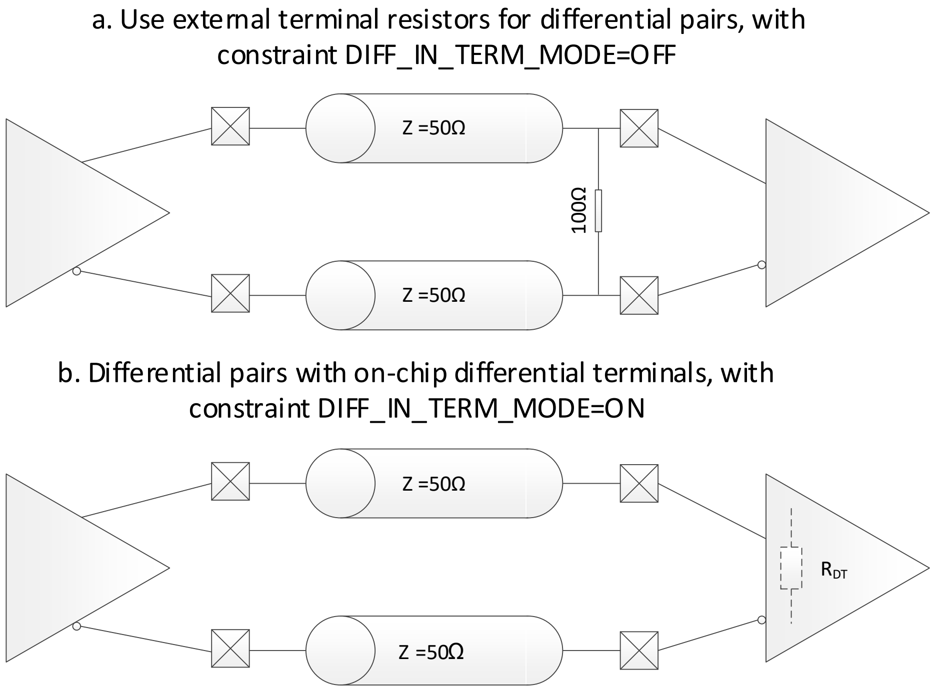


Figure 2-9 Termination Resistors Selection Method at the Differential Input End

When the attribute DIFF_IN_TERM_MODE of the I/O pin is set to "ON", the on-chip differential termination matching resistor is enabled. Use the following command to set constraints in the FDC file:

define_attribute {p:*port_name*} {PAP_IO_DIFF_IN_TERM_MODE} {*ON*}

➢ Termination Matching of Single-Ended Signal:

SSTL and HSTL interfaces are supported for termination matching of single-ended signal. For high-speed single-ended signals, such as memory interfaces, Logos Family FPGAs offer optional on-die termination features to eliminate the need for complex external on-board terminals.

The figure below shows how on-die termination replaces external terminal resistors.

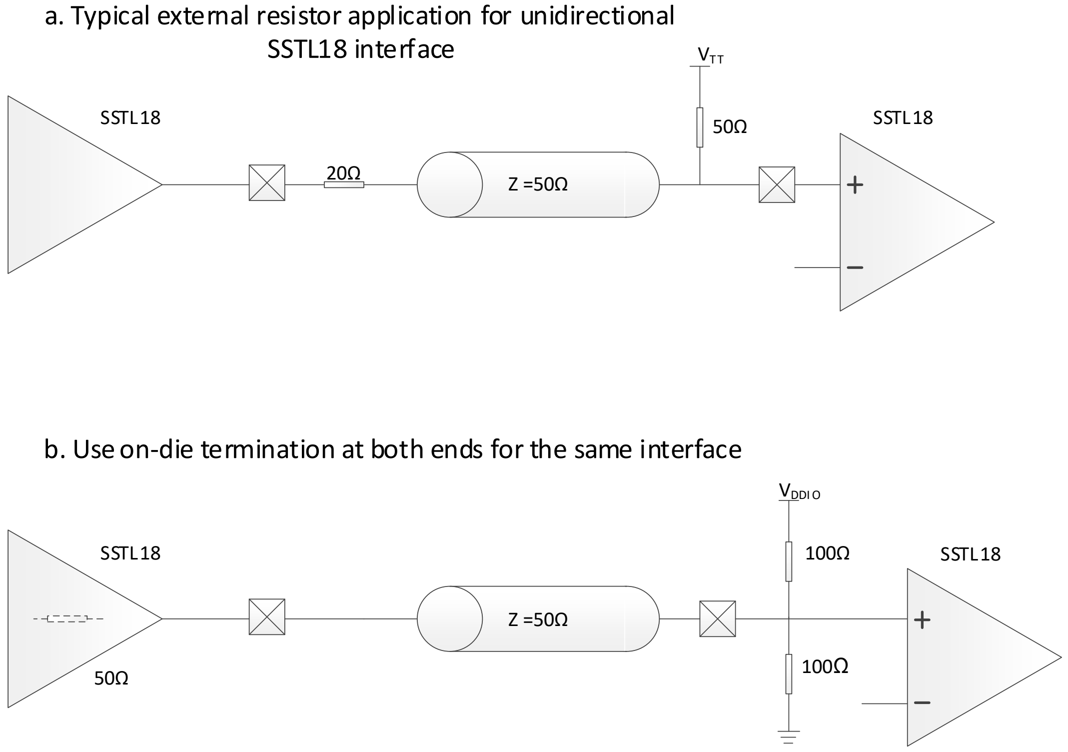


Figure 2-10 Application of SSTL18 Interface with On-Chip Termination

In practical applications, the SSTL18 interface is used for the address and control signals of DDR2 SDRAM interface, which requires a serial connection of a 50Ω matching resistor when VTT=VCCIO/2.

In the FDC file, on-die termination can be enabled through the I/O constraint as follows:

define_attribute { p:*port_name* } {PAP_IO_DDR_TERM_MODE} {*ON*}

In which, the parameter "ON" is selected to enable on-die termination; otherwise, choose "OFF".

2.2.3 Supported I/O Standards

The IO BUFFER of the Logos Family programmable logic devices supports a wide range of single-ended I/O standards, and all I/Os can be used to form differential pairs, which can support many differential standards. This flexibility allows users to select the most appropriate I/O standard for each pin to meet the needs of interface and signal integrity. These I/Os are allocated in several independent BANKs, each with a common output voltage (VCCIO) and a common reference voltage (VREF).

Each I/O standard has its specific electrical characteristics: including current, voltage, IO Buffering, and termination technology. The Logos Family programmable logic devices are precisely in line with this trend, supporting an ever-expanding range of I/O standards, and can adapt flexibly and rapidly to market demands. By configuring the IO BUFFER drivers, multiple I/O standards can be supported by the I/O. The single-ended I/O standards supported by the Logos Family are shown in the table below:

Table 2-2 Single-Ended I/O Standards Supported by the Logos Family

Single-Ended I/O Standard	**VCCIO**			**VREF**	**Supported by all BANKs**
	Output (V)	**Input (V)**	**Bi-Directional (V)**		
LVTTL33	3.3	3.3	3.3	/	Yes
LVCMOS33	3.3	3.3/2.5/1.8/1.5/1.2	3.3	/	Yes
LVCMOS25	2.5	2.5/1.8	2.5	/	Yes
LVCMOS18	1.8	1.8/1.5	1.8	/	Yes
LVCMOS15	1.5	1.5/1.2	1.5	/	Yes
LVCMOS12	1.2	1.2	1.2	/	Yes
SSTL25_I	2.5	2.5	2.5	1.25V	Yes
SSTL25_II	2.5	2.5	2.5	1.25V	Yes
SSTL18_I	1.8	1.8	1.8	0.90V	Yes
SSTL18_II	1.8	1.8	1.8	0.90V	Yes
SSTL15_I	1.5	1.5/1.2	1.5	0.75V	Yes
SSTL15_II	1.5	1.5/1.2	1.5	0.75V	Yes
HSTL18_I	1.8	1.8/1.5	1.8	0.90V	Yes
HSTL18_II	1.8	1.8/1.5	1.8	0.90V	Yes
HSTL15_I	1.5	1.5/1.2	1.5	0.75V	Yes

LVTTL (Low-Voltage TTL): A 3.3V standard defined by JESD, requires a 3.3V VCCIO for output, without the need for reference voltage and termination voltage.

LVCMOS (Low-Voltage CMOS): A low-voltage CMOS standard, with an application voltage from 1.2V to 3.3V. No reference voltage or termination voltage required.

SSTL25 (Stub Series Terminated Logic for 2.5V): A common memory bus standard defined by HITACHI and IBM (JESD8-8), requiring a 1.25V reference voltage, a 2.5V VCCIO, and a 1.25V termination voltage.

SSTL18 (Stub Series Terminated Logic for 1.8V): A 1.8V memory bus standard defined by JESD79-2C, requiring a 0.90V reference voltage, a 1.8V VCCIO, and a 0.90V termination voltage.

SSTL18 is used for high-speed SDRAM interfaces.

SSTL15 (Stub Series Terminated Logic for 1.5V): A 1.5V memory bus standard defined by JESD79-3, requiring a 0.75V reference voltage, a 1.5V VCCIO, and a 0.75V termination voltage. SSTL15 is used for high-speed SDRAM interfaces.

SSTL135 (Stub Series Terminated Logic for 1.35V): A 1.35V memory bus standard defined by JESD79-3-1, requiring a 0.675V reference voltage, a 1.35V VCCIO, and a 0.675V termination voltage. SSTL135 is used for DDR3L SDRAM memory interfaces.

HSTL18 (High-Speed Transceiver Logic for 1.8V): A high-speed bus standard defined by IBM, requiring a 0.90V reference voltage, a 1.8V VCCIO, and a 0.90V termination voltage.

HSTL15 (High-Speed Transceiver Logic for 1.5V): A high-speed bus standard defined by IBM, requiring a 0.75V reference voltage, a 1.5V VCCIO, and a 0.75V termination voltage.

HSUL12 (High-Speed Unterminated Logic for 1.2V): A high-speed bus standard defined by JESD8-22B, requiring a 0.6V reference voltage, a 1.2V VCCIO, and a 0.6V termination voltage. HSUL12 is used to improve bus power consumption during high-speed data transmission.

Logos Family products feature two types of differential outputs: true differential and pseudo-differential:

True differential outputs are supported by dedicated circuitry and offer higher performance, including LVDS, Mini-LVDS, Sub-LVDS, TMDS, and SLVS.

Pseudo-differential outputs are achieved with the help of external resistors based on the LVCMOS output standard, consisting of single-end driven COMP PAD and TRUE PAD, that is, a complementary output mode. Pseudo-differential output mode is used to drive complementary SSTL, MLVDS, and BLVDS I/O standards.

The differential I/O standards supported by the Logos Family are shown in the following table:

Table 2-3 Differential I/O Standards Supported by the Logos Family

Differential I/O Standard	**VCCIO**		**Remarks**	**Supported by all BANKs**
	Output (V)	**Input (V)**		
LVDS25	2.5	2.5	All BANKs support LVDS true differential inputs	Note 1
LVDS33	3.3	3.3	All BANKs support LVDS true differential inputs	Note 1
Sub-LVDS	2.5	2.5/3.3		Note 1
RSDS	2.5	2.5/3.3	Outputs are implemented through pseudo-differential mode	Yes
Mini-LVDS	2.5	2.5/3.3		Note 1
PPDS	2.5	2.5/3.3	Outputs are implemented through pseudo-differential mode	Yes
SLVS	1.2	1.2		Note 1

Differential I/O Standard	VCCIO		Remarks	Supported by all BANKs
	Output (V)	Input (V)		
TMDS	3.3	3.3	Open drain connection	Note 1
MLVDS	2.5	2.5	Outputs are implemented through pseudo-differential mode	Yes
BLVDS	2.5	2.5	Bidirectional multi-point driven input and output differential signals Outputs are supported by pseudo-differential mode with the help of peripheral resistors. Inputs are connected in differential mode	Yes
LVPECL	3.3	3.3	Outputs are implemented through pseudo-differential mode	Yes
SSTL25D_I	2.5	2.5	Outputs are implemented through pseudo-differential mode	Yes
SSTL25D_II	2.5	2.5	Outputs are implemented through pseudo-differential mode	Yes
SSTL18D_I	1.8	1.8	Outputs are implemented through pseudo-differential mode	Yes
SSTL18D_II	1.8	1.8	Outputs are implemented through pseudo-differential mode	Yes
SSTL15D_I	1.5	1.5	Outputs are implemented through pseudo-differential mode	Yes
SSTL15D_II	1.5	1.5	Outputs are implemented through pseudo-differential mode	Yes
HSTL18D_I	1.8	1.8	Outputs are implemented through pseudo-differential mode	Yes
HSTL18D_II	1.8	1.8	Outputs are implemented through pseudo-differential mode	Yes
HSTL15D_I	1.5	1.5	Outputs are implemented through pseudo-differential mode	Yes

Note : See Tables 16, 17, and 18of "DS02001_Logos Family FPGAs Device Data Sheet"

LVDS (Low Voltage Differential Signal): A differential standard where a data bit is transmitted through two signal lines, thus inherently immune to noise compared with single-ended I/O standards. The voltage swing between the two signal lines is about 350mV. No reference voltage or termination voltage required. LVDS inputs require matching resistors, which can be discrete resistors on the PCB or enabled matching resistors on the chip through the

DIFF_IN_TERM_MODE attribute.

Mini-LVDS is developed based on the LVDS interface standard and is typically used in the flat panel display sector as an interface between the timing control module and the LCD. It has a smaller swing, generates very low electromagnetic interference, and can provide high bandwidth for display drivers.

Sub-LVDS is used for CMOS sensor interfaces.

RSDS (Reduced Swing Differential Signaling): An intra-panel bus interface standard commonly used in the display sector. It defines the transmission/reception characteristics and protocol for interfaces between chips. RSDS inputs require parallel terminal resistors, which can be discrete resistors on the PCB or enabled matching resistors on the chip through the DIFF_IN_TERM_MODE attribute.

PPDS (Point-to-Point Differential Signaling): The standard for internal display interfaces for next-generation LCD. PPDS inputs require parallel terminal resistors, which can be discrete resistors on the PCB or enabled matching resistors on the chip through the DIFF_IN_TERM_MODE attribute.

SLVS is an adjustable low-voltage signal, used for MIPI D-PHY interfaces.

TMDS (Transition Minimized Differential Signaling): An overmoduled differential signaling, also known as minimized transmission differential signaling, used for DVI and HDMI interfaces.

LVPECL (Low Voltage Positive Emitter-Coupled Logic): It is commonly used for on-board clock distribution networks.

MLVDS (Multipoint Low Voltage Differential Signaling): It is used for optimizing multipoint interconnected applications, which refer to interconnected applications where multiple drivers or receivers share a single physical link, and are used in situations requiring bidirectional multipoint driven differential signal input and output. The IO itself does not support such output standard; it requires the complementary output principle of LVCMOS and external chip resistors to implement this standard.

BLVDS (Bus Low Voltage Differential Signaling): An output standard similar to the MLVDS standard proposed by National Semiconductor, also used in situations requiring bidirectional multipoint driven differential signal input and output. The difference between the two is that MLVDS is an industrial standard, and has a larger differential amplitude than BLVDS, requiring a higher current driving capability. The I/O itself does not support BLVDS; it requires the complementary output principle of LVCMOS and external chip resistors to implement this standard.

Differential outputs such as SSTL25D, SSTL18D, SSTL15D, HSTL18D, and HSTL15D are implemented through pseudo-differential modes.

Different I/O standards have different timings, which will be analyzed by the Pango Design Suite software, with the result included in a timing analysis report.

I/O Standards can be constrained through the following statement in the FDC file or operated on the PDS's UCE interface.

define_attribute {p:*port_name*} {PAP_IO_STANDARD} { *LVCMOS33* }

2.2.4 I/O Supply Voltage Introduction

According to actual user designs, the IO BUFFER is powered by a mix of three main FPGA power sources: VCC, VCCAUX, and VCCIO. For detailed voltage values, refer to the "DS02001_Logos Family FPGAs Device Data Sheet".

- VCC

VCC is the core voltage of the FPGA chip, mainly used to power the control logic circuit of the IO BUFFER and the majority of the IO LOGIC circuit. When outputting data from the core, control signals pass through the IO LOGIC and IO BUFFER control logic, converting the data signal from VCC powered to higher supply voltage powered; when inputting data to the core, control signals pass through the IO BUFFER control logic and IO LOGIC, converting the data signal from high supply voltage powered to VCC powered.

- VCCAUX

VCCAUX is the auxiliary power voltage, primarily used to power differential output driving circuits, differential input circuits, and input circuits with reference voltages in SSTL and HSTL standards.

- VCCIO

VCCIO voltage is independently supplied in each BANK, mainly for single-ended output driving circuits and ratio input circuits. Therefore, the characteristic values of IO standards powered by VCCIO will vary with VCCIO power voltage.

- GND

Although within the I/O circuits, for placement planning and signal partitioning, different supply voltages correspond to different ground connections, such as VCCIO to VSSIO, VCCAUX to VSS, VCC to VSS, etc. However, at the chip's top level, all these I/O grounds are connected to a common GND during the packaging process.

2.2.5 Hot Plugging Support supported

The hot plugging feature ensures that the chip will not be damaged due to excessive leakage current.

The implementation of the hot plugging feature and its characteristic parameters are related to the power-up process within the I/O, specific mixed input modes, and the state of the CLAMP switch.

All four sides of Logos Family FPGAs chips support the hot plugging feature.

2.2.6 BUS KEEPER Feature

The main function of the BUS KEEPER circuit is to maintain the current I/O data state before the next I/O data takes effect. Each I/O has an independent BUS KEEPER function, typically with four programmable modes: PULLUP, PULLDW, KPR, and UNUSED.

BUS KEEPER feature can be edited through the following statement in the FDC file or operated in the PDS's UCE interface.

"define_attribute {p:*port_name*} {PAP_IO_*UNUSED*} {TRUE}"

2.2.7 Input Hysteresis Feature

LVCMOS33/LVTTL33/LVCMOS25/LVCMOS18 input standards support input hysteresis features, with two programmable hysteresis amounts available: large and small. The programmable modes include: SMHYS_I (Type 1 small hysteresis), SMHYS_II (Type 2 small hysteresis), LGHYS (large hysteresis), and NOHYS (no hysteresis).

Input hysteresis feature can be edited through the following statement in the FDC file or operated in the PDS's UCE interface.

"define_attribute {p:port_name} {PAP_IO_HYS_DRIVE_MODE} {NOHYS}"

2.2.8 Input Buffer Types

Each input pad has two types of input buffers to meet the requirements of different input standards. The first type is the ratio receiver buffer with a power voltage of VCCIO; the second type is the input buffer with a power voltage of VCCAUX, which can implement input standards with reference voltage-determined thresholds and differential input standards.

Table 2-4 Input Buffer Types

<table>
<tr><th colspan="2"></th><th>Power</th><th>Single-Ended</th><th>Dual Port</th><th>Supported Standard</th><th>Remarks</th></tr>
<tr><td rowspan="2">Input Buffer</td><td>Single-Ended</td><td>VCCIO</td><td>√</td><td></td><td>LVTTL33/LVCMOS</td><td>UD supported</td></tr>
<tr><td>Differential</td><td>VCCAUX</td><td></td><td>√</td><td>SSTL/HSTL15/18/25
,
LVDS (input)</td><td>SSTL and HSTL standards require reference voltage</td></tr>
</table>

						and matching resistor support

2.2.9 Buffer Voltage Reference (VREF)

I/O standards with reference voltages, such as SSTL and HSTL, require a reference voltage to set thresholds. This reference voltage can be generated in two methods. The first method is through input from a specific I/O pin; the second method is through an internal reference voltage generation circuit within the I/O circuit.

In the first method, each BANK has a specific user I/O that can be programmed to serve as the input for VREF. In the second method, the reference voltage is provided to all I/Os in the entire BANK through the I/O internal reference voltage generation circuit to support the I/O standards that require a reference voltage. Each BANK corresponds to an internal reference voltage generation circuit, where the output of the reference voltage can be set to four states through constraints: OFF, 45% of VCCIO, 50% of VCCIO, and 55% of VCCIO, with the effective values being OFF, 0.45, 0.5, and 0.55 respectively. Use the following statement to set constraints in the FDC file, or operate in the PDS's UCE interface.

"define_attribute {p:*port_name*} {PAP_IO_VREF_MODE_VALUE} {*0.5*}"

The two methods of generating VREF reference voltage need to be selected and set through programming to provide a reference voltage input to the I/O. However, it should be noted that once this specific I/O is selected as the reference voltage input pin in the first method, it cannot be used as a user I/O to support I/O standards that require a reference voltage until the pin is released. The figure below is a schematic diagram of the circuit connection.

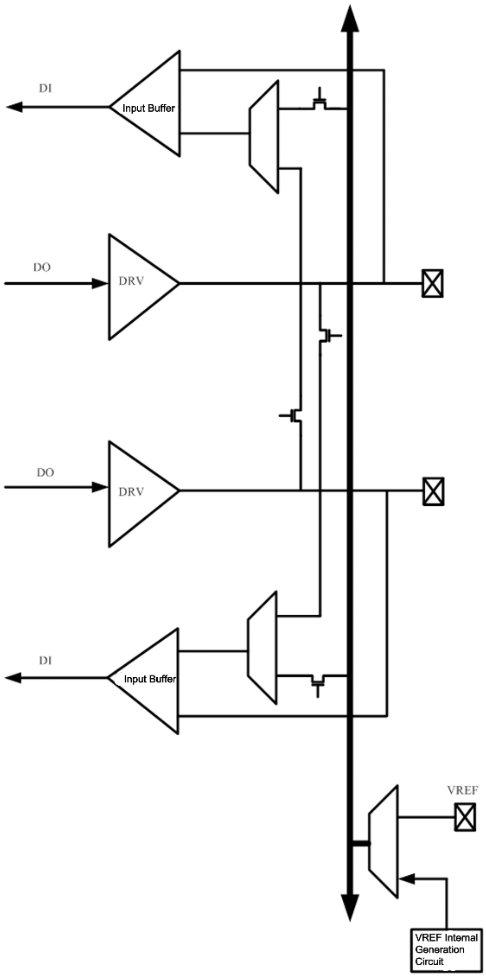


Figure 2-11 Schematic Diagram of VREF Connection

The table below lists the reference voltage values for some of the IO standards.

Table 2-5 Reference Voltages for Some IO Standards

I/O Standard	VREF(V)
SSTL25_I	1.25
SSTL25_II	1.25
SSTL18_I	0.9
SSTL18_II	0.9
SSTL15_I	0.75
SSTL15_II	0.75
HSTL18_I	0.9
HSTL18_II	0.9
HSTL15_I	0.75

2.2.10 Programmable Output Drive Capability

The programmable characteristics of single-ended output drive capability are primarily based on the LVCMOS and LVTTL standards. The drive capability specifications listed in the table below are based on conditions where the output high level is 400mV below the VCCIO supply voltage or the output low level is 400mV above ground.

Table 2-6 Drive Capability of LVCMOS and LVTTL Output Standards

VCCIO	Output Drive Current (mA)						
	2	4	6	8	12	16	24
1.2V	√		√				
1.5V		√		√	√		
1.8V		√		√	√	√	
2.5V		√		√	√	√	
3.3V		√		√	√	√	√

The output drive capability for SSTL and HSTL standards is influenced by the circuit balance requirements during application. The performance and signal integrity of the I/O interface shall be comprehensively considered, which requires matching with buffer resistors. The table below lists the output drive capability for SSTL standards.

Table 2-7 List of Drive Capability for SSTL Output Buffer

IO Standard	Application Interfaces	Buffer Output Connected to the Near-End PCB	Buffer Output Low Level	Buffer Drive Capability and Output Impedance
SSTL25_I	DDR1	Direct connection or addition of series resistors depending on the application	0.56V from rail	8.1mA (69ohm)
SSTL25_II	DDR1	Direct connection or addition of series resistors depending on the application	0.36V from rail	16.2mA(22ohm)
SSTL18_I	DDR2	Direct Connection	0.40V from rail	6.7mA (60ohm)
SSTL18_II	DDR2	DIMM	0.28V from rail	13.4mA(21ohm)
SSTL15_I	DDR3	Direct Connection	0.2* VCCIO from rail	7.5mA(40ohm)
SSTL15_II	DDR3	Incorporate a 22-ohm resistor	0.2* VCCIO from rail	8.8mA(34ohm)

The table below lists the output drive capability for HSTL standards.

Table 2-8 Drive Capability of HSTL Output Buffers

IO Standard	Application Interfaces	Buffer Drive Capability
HSTL18_I		8mA
HSTL18_II	QDR II	16mA
HSTL15_I		8mA

The output drive current of LVDS can be programmably set to meet different output common-mode voltage VCM, and output high and low levels VOH and VOL requirements. It can be set to support different types of differential output standards, as shown in the table below.

Table 2-9 Differential Signal Current Drive Capability

Differential Output	**Output Drive Current (mA)**													
	1.0	**1.5**	**2.0**	**2.5**	**3.0**	**3.5**	**4.5**	**6.5**	**7.5**	**8.0**	**9.0**	**9.5**	**10**	**11**
LVDS25		√	√	√	√	√	√	√						
Sub-LVDS	√	√	√											
Mini-LVDS				√	√	√	√	√	√	√	√			
SLVS		√	√	√										
TMDS											√	√	√	√

The output drive capability of the I/O can be constrained using the following statement in the FDC file, or operated in the PDS's UCE interface.

"define_attribute {p:port_name} {PAP_IO_DRIVE} {4}"

2.2.11 Open-Drain Control

Each IO BUFFER's single-ended output driving circuit can independently support Open-Drainfunction. That is, during Open-Drain output, the output driving circuit only includes the current sunk and does not provide current sourced.

Open-Drain control includes ON and OFF.Open-Drain control can be constrainedusing the following statement in the FDC file, or operated on the PDS's UCE interface.

"define_attribute {p:port_name} {PAP_IO_OPEN_DRAIN} {OFF}"

2.2.12 Tri-State Control Output

In the I/O output path, each single-ended output driving circuit has an independent tri-state control circuit. Additionally, a multiplexed I/O generates a flag signal IO_STATE for controlling the port state of all I/Os during the configuration process. For PGL12G and PGL22G, when IO_STATUS_C=0, it indicates that the I/O is in a tri-state during configuration; when IO_STATUS_C=1, it indicates that the I/O is in a pull-up state during configuration. The tri-state control of the differential driving circuit uses the tri-state control of the single-ended output driver of the TRUE pad.

Note: For PGL25G, PGL50G, PGL50H, and PGL100H, when IO_STATUS_C=0, it indicates that the I/O is in a pull-up state during configuration; when IO_STATUS_C=1, it indicates that the I/O is in a tri-state during configuration.

2.2.13 Programmable Slew Rate

Based on the requirements to reduce output noise or enhance high-speed output performance, each I/O output driver has a programmable slew rate control setting for controlling the speed of the output slew rate. The slew rate control for each I/O is independent. The available parameters are: "FAST" and "SLOW".

Programmable slew rate can be constrained using the following statement in the FDC file, or constrained in the PDS's UCE interface.

"define_attribute { p:*port_name* } {PAP_IO_SLEW} {*FAST*}"

2.2.14 Pseudo-Differential Output Implementation

The outputs of LVPECL, MLVDS, BLVDS, PPDS, and RSDS can supported differential output by connecting external resistors. In our I/O circuit design, true differential output can be implemented through the differential output driving circuit for LVDS and others, so these differential output buffers do not require additional resistors outside the driving circuit.

All pairs of single-ended IO BUFFERs can support pseudo-differential output at different data rates with external resistors, with specific speeds determined by the capabilities of the single-ended IO BUFFERs adopted by each output standard.

- Pseudo-Differential Output - LVPECL33

LVPECL output is primarily used for point-to-point applications, with the most common example being clock distribution networks at the board level. The figure below shows a possible implementation of LVPECL in a point-to-point application. R0, R1, and RT values should be selected based on circuit design and verification., The reference values are provided to ensure the output levels meet the standard requirements, with specific values determined according to the actual chip test results finally provided by the product engineers.

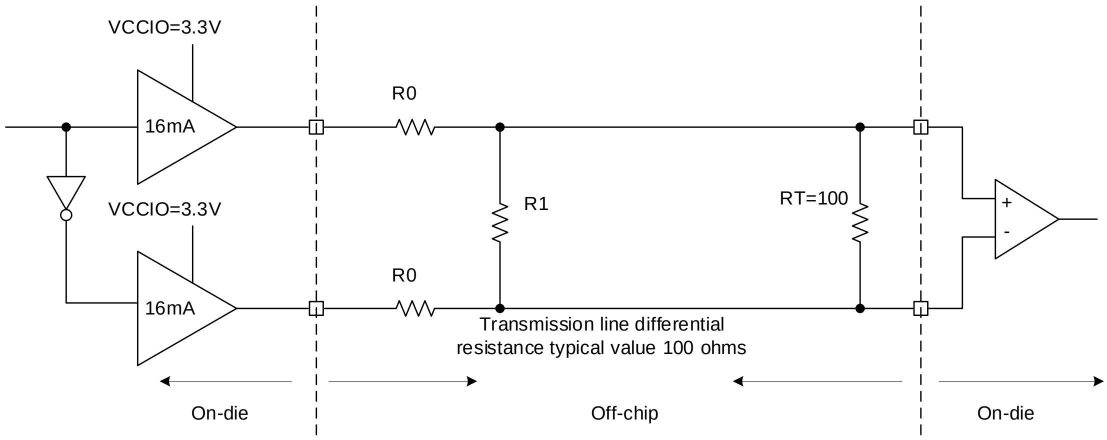


Figure 2-12 LVPECL Point-to-Point Output Example

➢ Pseudo-Differential Output - MLVDS

MLVDS is used in cases where bidirectional multipoint driven differential input and output signals is required. The I/O itself does not support such output standard; it requires the complementary output principle of LVCMOS and external chip resistors to implement this standard. The differential amplitude of MLVDS is larger than that of BLVDS, and it requires a higher current driving capability. The figure below shows a typical application of MLVDS multi-point configuration. R0 and R1 values should be based on circuit design and verification., The reference values are provided to ensure the output levels meet the standard requirements, with specific values determined according to the actual chip test results finally provided by the product engineers.

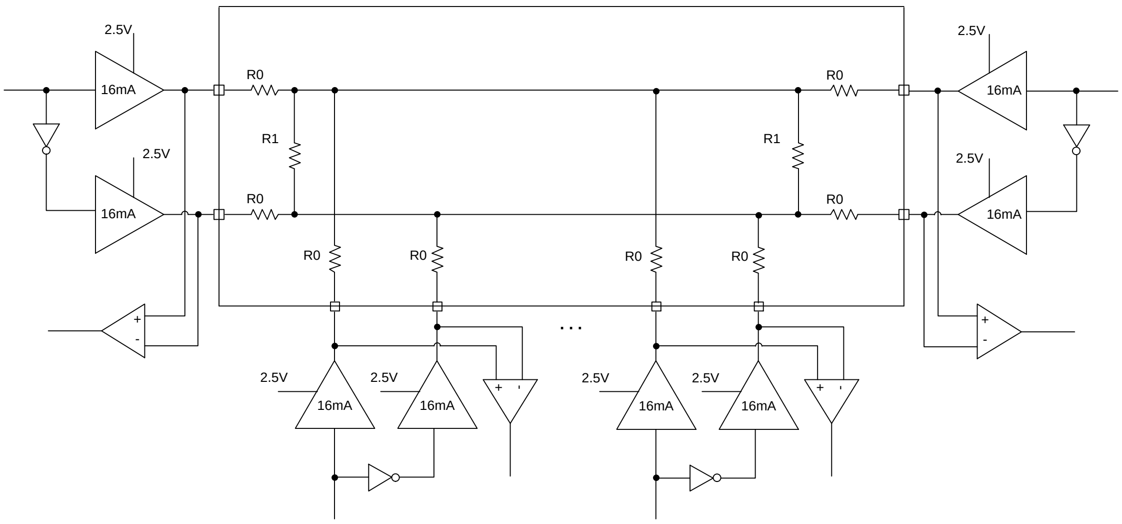


Figure 2-13 MLVDS Point-to-Point Output Example

➢ Pseudo-Differential Output - BLVDS

BLVDS is an output standard similar to the MLVDS standard proposed by National Semiconductor, also used in situations requiring bidirectional multipoint driven differential signal input and output. The difference between the two is that MLVDS is an industrial standard, and has a larger differential amplitude than BLVDS, requiring a higher current driving capability. The I/O itself does not support BLVDS; it requires the complementary output principle of LVCMOS and external chip resistors to implement this standard. The figure below shows a typical application of BLVDS multi-point configuration. R0 and R1 values should be based on circuit design and verification., The reference values are provided to ensure the output levels meet the standard requirements, with specific values determined according to the actual chip test results finally provided by the product engineers.

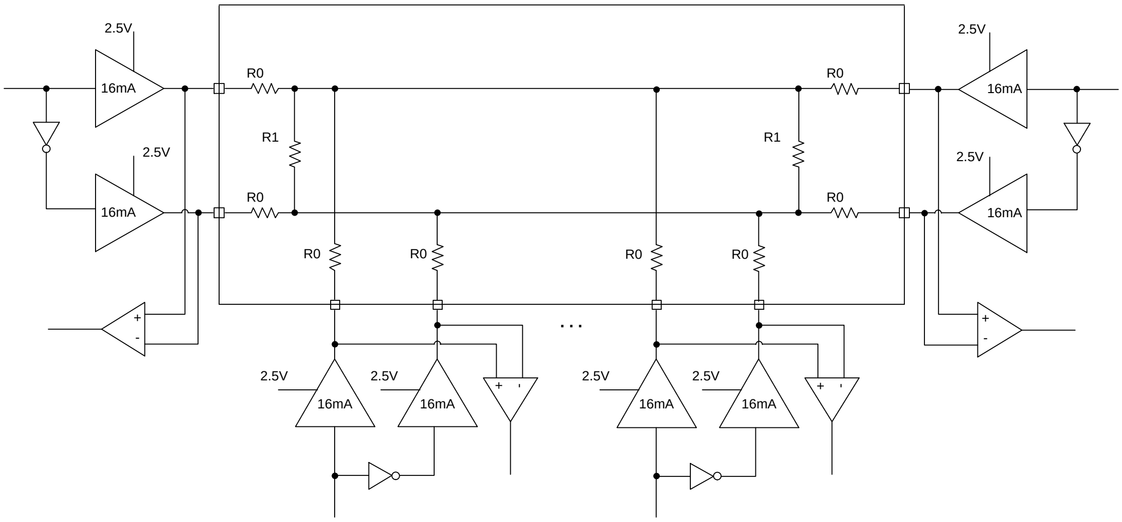


Figure 2-14 BLVDS Point-to-Point Output Example

- Pseudo-Differential Output - RSDS

RSDS (Reduced Swing Differential Switching) is commonly used in the display field. The figure below provides an example of RSDS implementation. R0, R1, and RT values should be based on circuit design and verification., The reference values are provided to ensure the output levels meet the standard requirements, with specific values determined according to the actual chip test results finally provided by the product engineers.

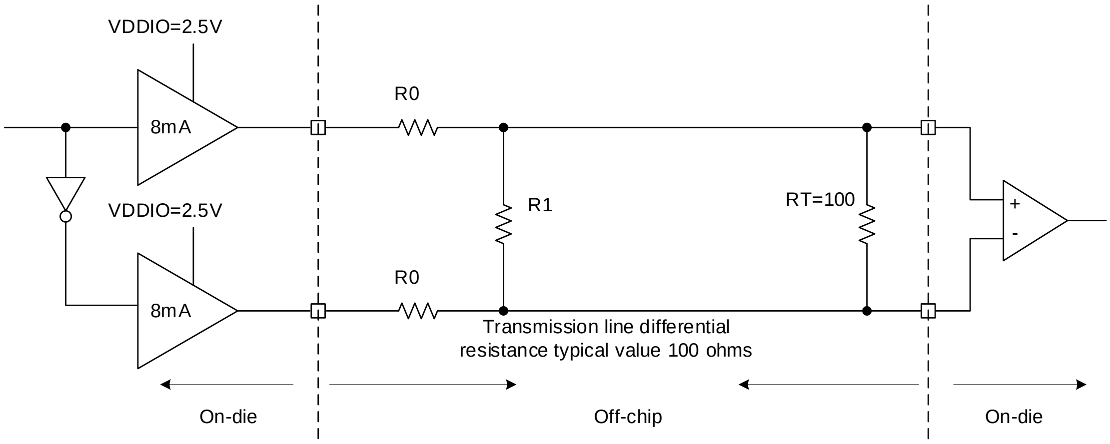


Figure 2-15 RSDS Point-to-Point Output Example

2.2.15 MIPI Implementation Method

Within the Logos Family, PGL12G, PGL25G, PGL50G, PGL50H, and PGL100H use MIPI 2-wire input, and all use MIPI 2-wire output.

1. Implement MIPI Input with Two I/O Units

HS-MIPI input and LP-MIPI input can also be implemented with SLVS and 2 I/O units, as shown in the block diagram below.

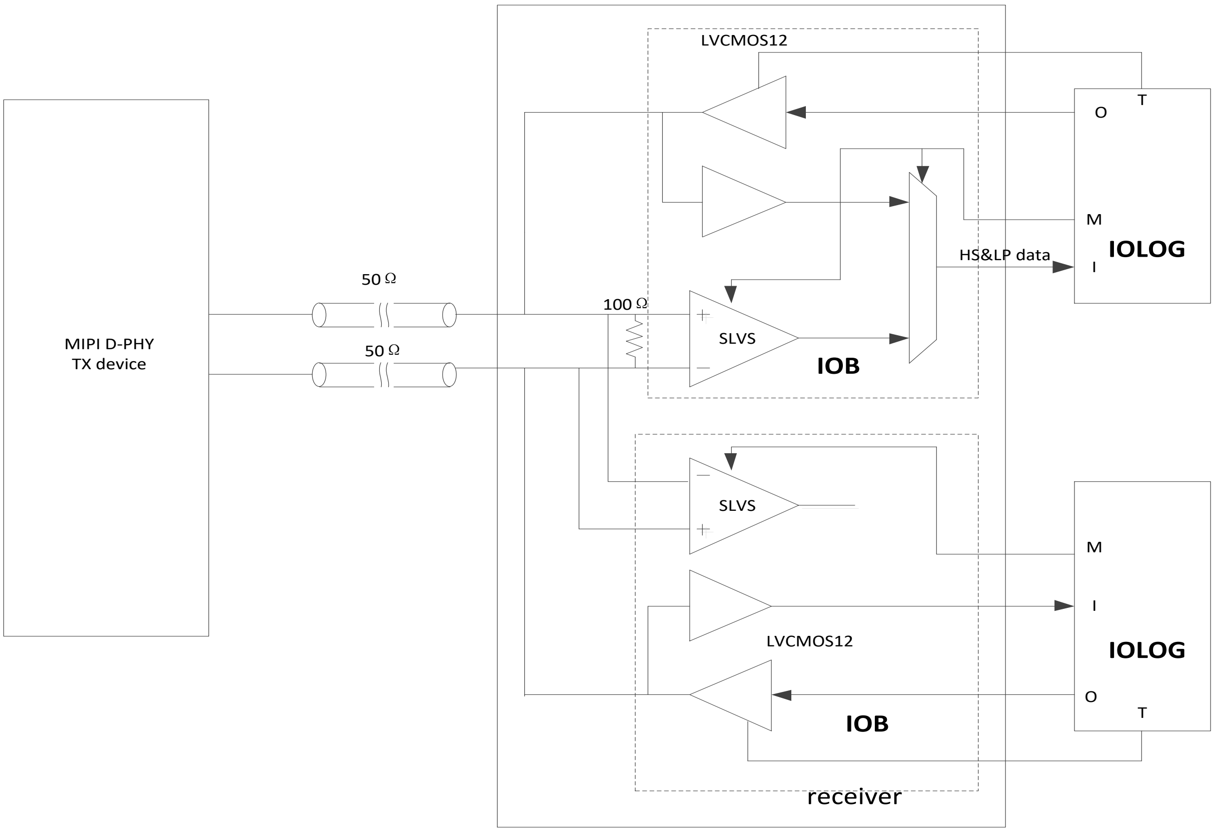


Figure 2-16 MIPI Input Implemented with SLV (HS/LP)

2. Implement MIPI Output with Two I/O Units

HS-MIPI output and LP-MIPI output can also be implemented with SLVS and 2 I/O units, as shown in the block diagram below.

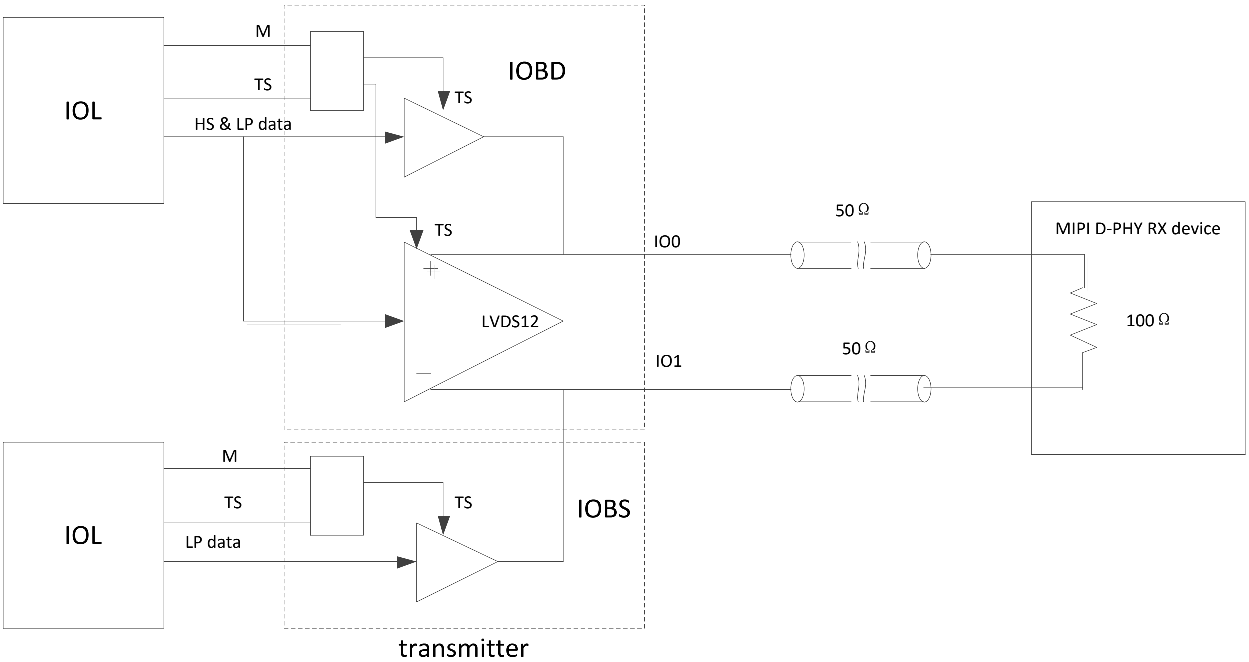


Figure 2-17 MIPI Output Implemented with SLV (HS/LP)

2.2.16 I/O Power-up and Configuration

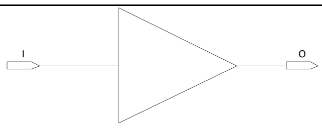
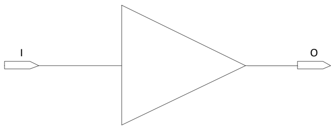
The basic requirement for the normal operation of Logos Family products is that the core voltage VCC (1.1V or 1.2V), auxiliary voltage VCCAUX (3.3V), and the BANK I/O voltage VCCIO where the programming pins are located must be supplied normally. The chip has a built-in dedicated circuit to monitor these power supplies, and the chip initialization begins only when all these power voltages are at normal levels.

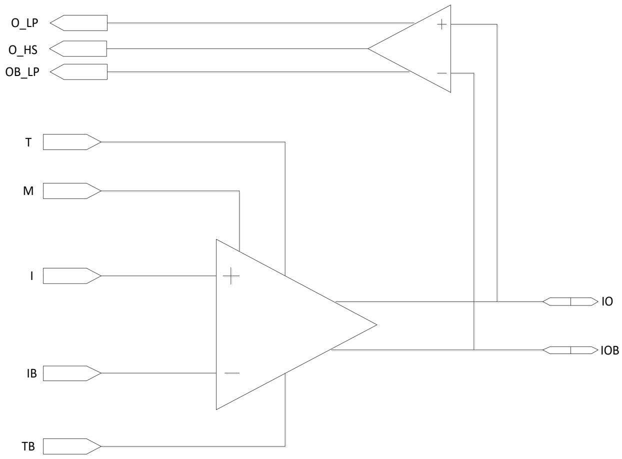
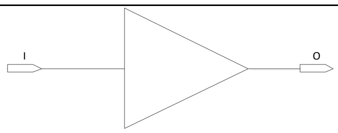
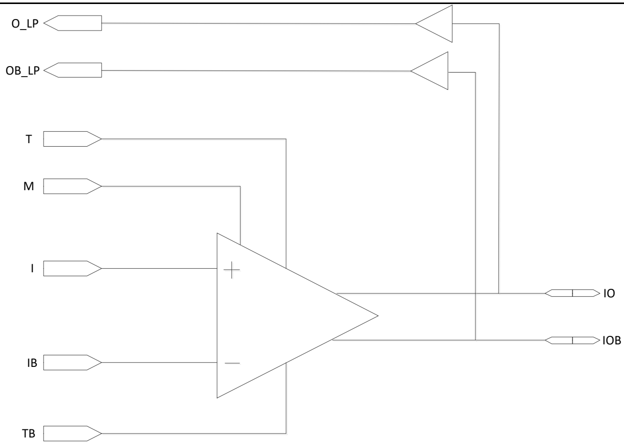
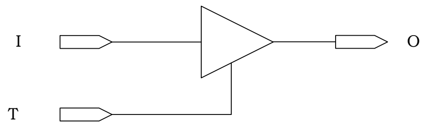
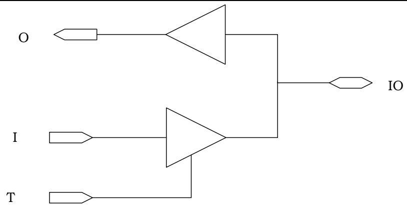
Upon normal power supply voltages, memory initialization and configuration begins in the FPGA. At this point, a global reset is triggered in the FPGA, setting all IO BUFFERs to their default state. After initialization, INIT_FLAG_N indicates high level. The chip then samples the input of the M [2:0] pins to determine the programming mode, and configuration data is loaded into the FPGA according to the corresponding mode. During FPGA configuration, the status of the user I/O is as described in Section 2.2.12. Upon download completion, the reset is released, the CFG_DONE pin is driven high, the I/O pins used in the design are activated, and the state of unused I/O pins is determined by the bitstream, which can be set in the Pango Design Suite software interface.

2.2.17 Basic Prototype of GTP for IO BUFFER

The software library of Pango Design Suite includes related GTPs (General Technology Primitives) to support various I/O standards. The following are the most common basic prototypes of GTPs in single-ended I/O standards.

Table 2-10 GTPs for Single-Ended I/Os

GTP Name	GTP Description	GTP Illustration
GTP_INBUF	Single-ended input signals must pass through INBUF, supporting IOBD, IOBS, and IOBR	
GTP_INBUFG	INBUFG is the same as INBUF. When the input signal enters the FPGA from the clock pin, the PDS software will automatically use INBUFG.	

GTP Name	GTP Description	GTP Illustration
GTP_IOBUF_RX_MIPI	MIPI DPHY high-speed (HS) input, as well as single-ended input/output under low power mode (LP), supporting IOBR and IOBS	
GTP_OUTBUF	Single-ended input signal	
GTP_IOBUF_TX_MIPI	MIPI DPHY tri-state output, including input/output in low-power mode (LP) and differential output in high-speed (HS) mode, with both modes being switchable according to practical application.	
GTP_OUTBUFT	Used for tri-state output or bidirectional I/O	
GTP_IOBUF	Single-ended input/output	

- GTP_INBUF

Ports are described as follows:

Table 2-11 GTP_INBUF Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from input buffer to the chip

Parameters are described as follows:

Table 2-12 GTP_INBUF Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-13	Input IO standard
TERM_DDR	string	See Table 2-13	When inputting HSTL, SSTL standards, the built-in terminal resistor can be enabled or disabled

The optional configuration attributes for the parameters are as follows:

Table 2-13 Parameter Configuration List

GTP_INBUF	
IOSTANDARD	**TERM_DDR**
LVTTL33	None
LVCMOS33	
LVCMOS25	
LVCMOS18	
LVCMOS15	
LVCMOS12	
SSTL25_I	OFF/ON
SSTL25_II	OFF/ON
SSTL18_I	OFF/ON
SSTL18_II	OFF/ON
SSTL15_I	OFF/ON
SSTL15_II	OFF/ON
HSTL18_I	OFF/ON
HSTL18_II	OFF/ON
HSTL15_I	OFF/ON
SSTL15_I	ON
SSTL15_II	ON
HSTL15_I	ON

➢ GTP_INBUFG

Ports are described as follows:

Table 2-14 GTP_INBUFG Port Description

Port	Direction	Function Description
I	Input	PAD signal input
O	Output	Output from buffer to the chip

Parameters are described as follows:

Table 2-15 GTP_INBUFG Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-16	Input IO standard
TERM_DDR	string	See Table 2-16	When inputting HSTL, SSTL standards, the built-in terminal resistor can be enabled or disabled

The valid parameter values are listed as follows:

Table 2-16 Valid Parameter Values

GTP_INBUFG	
IOSTANDARD	**TERM_DDR**
LVCMOS33	None
LVCMOS25	
LVCMOS18	
LVCMOS15	
LVCMOS12	
SSTL25_I	OFF/ON
SSTL25_II	OFF/ON
SSTL18_I	OFF/ON
SSTL18_II	OFF/ON
SSTL15_I	OFF/ON
SSTL15_II	OFF/ON
HSTL18_I	OFF/ON
HSTL18_II	OFF/ON
HSTL15_I	OFF/ON
SSTL15_I	ON
SSTL15_II	ON
HSTL15_I	ON

- GTP_IOBUF_RX_MIPI

Ports are described as follows:

Table 2-17 GTP_IOBUF_MIPI Port Description

Port	Direction	Function Description
I	Input	The input signal for the single-ended output buffer from "fabric" in LP mode
IB	Input	The input signal for the single-ended output buffer from "fabric" in LP mode
M	Input	Mode selection signal. 1: HS mode, differential input; 0: LP mode, single-ended input. From fabric
T	Input	Single-ended output enable signal; when it is 0, IO serves as output, and when it is 1, IO serves as input
TB	Input	Single-ended output enable signal; when it is 0, IOB serves as output, and when it is 1, IOB serves as input
O_HS	Output	Differential output (HS) to fabric
O_LP	Output	Single-ended output (LP)

Port	Direction	Function Description
OB_LP	Output	Single-ended output (LP)
IO	Bi-Directional	P side differential input (HS mode), or single-ended input and output (LP mode)
IOB	Bi-Directional	N side differential input (HS mode), or single-ended input and output (LP mode)

Parameters are described as follows:

Table 2-18 GTP_IOBUF_MIPI Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	" DEFAULT "	Input I/O standard, V_{CCIO}=1.2V
DRIVE_STRENGTH	string	"2", "6"	Drive current strength
TERM_DIFF	string	"ON", "OFF"	Internal terminal matching resistor enabled or disabled

- GTP_OUTBUF

Ports are described as follows:

Table 2-19 GTP_OUTBUF Port Description

Port	Direction	Function Description
I	IN	Single-ended signal input
O	OUT	buffer output

Parameters are described as follows:

Table 2-20 GTP_OUTBUF Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-21	Input IO standard
DRIVE_STRENGTH	string	See Table 2-21	Drive current strength

The valid parameter values are listed as follows:

Table 2-21 Valid Parameter Values

GTP_OUTBUF		
IOSTANDARD	**SLEW_RATE**	**DRIVE_STRENGTH**
LVTTL33	FAST/SLOW	"4", "6", "12", "16", "24"
LVCMOS33	FAST/SLOW	
LVCMOS25	FAST/SLOW	"4", "8", "12", "16"
LVCMOS18	FAST/SLOW	
LVCMOS15	FAST/SLOW	"4", "8", "12"
LVCMOS12	FAST/SLOW	"2", "6"
SSTL25_I	FAST/SLOW	None
SSTL25_II	FAST/SLOW	
SSTL18_I	FAST/SLOW	

GTP_OUTBUF		
IOSTANDARD	**SLEW_RATE**	**DRIVE_STRENGTH**
SSTL18_II	FAST/SLOW	
SSTL15_I	FAST/SLOW	
SSTL15_II	FAST/SLOW	
HSTL18_I	FAST/SLOW	
HSTL18_II	FAST/SLOW	
HSTL15_I	FAST/SLOW	
SSTL15_I	FAST/SLOW	
SSTL15_II	FAST/SLOW	
HSTL15_I	FAST/SLOW	

- GTP_IOBUF_TX_MIPI

Ports are described as follows:

Table 2-22 GTP_OUTBUF_MIPI Port Description

Port	Direction	Function Description
I	Input	Input signals of differential output buffer (HS) and single-ended output buffer (LP), from IO Logic
IB	Input	The input signal for the single-ended output buffer in LP mode, from IO Logic
M	Input	Mode selection signal. 1: HS mode, differential input; 0: LP mode, single-ended input and output. From IO Logic
T	Input	Differential and single-ended output enable signal
TB	Input	Single-ended output enable signal
O_LP	Output	Single-ended output (LP)
OB_LP	Output	Single-ended output (LP)
IO	Bi-Directional	P-side differential output or input
IOB	Bi-Directional	N-side differential output or input

Parameters are described as follows:

Table 2-23 GTP_OUTBUF_MIPI Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	" DEFAULT "	Input I/O standard, V_{CCIO}=1.2V
DRIVE_STRENGTH	string	"2", "6"	Drive current strength
SLEW_RATE	string	"SLOW", "FAST"	Slew rate
TERM_DIFF	string	"ON", "OFF"	Internal terminal matching resistor enabled or disabled

- GTP_OUTBUFT

Ports are described as follows:

Table 2-24 GTP_OUTBUFT Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	buffer output
T	Input	Enable signal; 1: Active

Parameters are described as follows:

Table 2-25 GTP_OUTBUFT Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-26	Input IO standard
SLEW_RATE	string	"SLOW", "FAST"	Slew rate
DRIVE_STRENGTH	string	See Table 2-26	Drive current strength

The valid parameter values are listed as follows:

Table 2-26 Valid Parameter Values

<table>
<tr><th colspan="3">GTP_OUTBUFT</th></tr>
<tr><th>IOSTANDARD</th><th>SLEW_RATE</th><th>DRIVE_STRENGTH</th></tr>
<tr><td>LVTTL33</td><td>FAST/SLOW</td><td rowspan="3">"4", "6", "12", "16", "24"</td></tr>
<tr><td>PCI33</td><td>FAST/SLOW</td></tr>
<tr><td>LVCMOS33</td><td>FAST/SLOW</td></tr>
<tr><td>LVCMOS25</td><td>FAST/SLOW</td><td rowspan="2">"4", "8", "12", "16"</td></tr>
<tr><td>LVCMOS18</td><td>FAST/SLOW</td></tr>
<tr><td>LVCMOS15</td><td>FAST/SLOW</td><td>"4", "8", "12",</td></tr>
<tr><td>LVCMOS12</td><td>FAST/SLOW</td><td>"2", "6",</td></tr>
<tr><td>SSTL25_I</td><td>FAST/SLOW</td><td rowspan="12">None</td></tr>
<tr><td>SSTL25_II</td><td>FAST/SLOW</td></tr>
<tr><td>SSTL18_I</td><td>FAST/SLOW</td></tr>
<tr><td>SSTL18_II</td><td>FAST/SLOW</td></tr>
<tr><td>SSTL15_I</td><td>FAST/SLOW</td></tr>
<tr><td>SSTL15_II</td><td>FAST/SLOW</td></tr>
<tr><td>HSTL18_I</td><td>FAST/SLOW</td></tr>
<tr><td>HSTL18_II</td><td>FAST/SLOW</td></tr>
<tr><td>HSTL15_I</td><td>FAST/SLOW</td></tr>
<tr><td>SSTL15_I</td><td>FAST/SLOW</td></tr>
<tr><td>SSTL15_II</td><td>FAST/SLOW</td></tr>
<tr><td>HSTL15_I</td><td>FAST/SLOW</td></tr>
</table>

- GTP_IOBUF

Ports are described as follows:

Table 2-27 GTP_IOBUF Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from input buffer to the chip
T	Input	Enable output buffer
IO	Input/Output	PAD

Parameters are described as follows:

Table 2-28 GTP_IOBUF Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-29	Input IO standard
TERM_DDR	string	"ON", "OFF"	When inputting HSTL, SSTL standards, the built-in terminal resistor can be enabled or disabled
SLEW_RATE	string	"SLOW", "FAST"	Slew rate
DRIVE_STRENGTH	string	"2", "4", "6", "8", "12", "16", "24"	Drive current strength

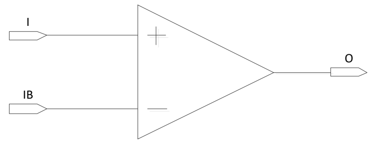
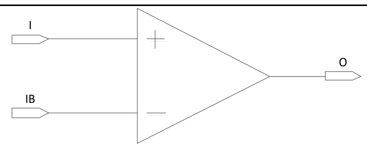
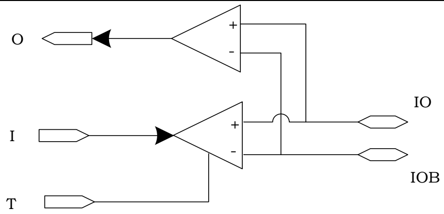
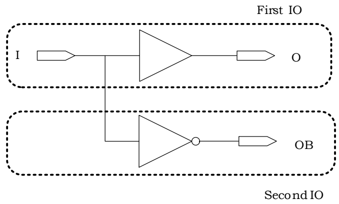
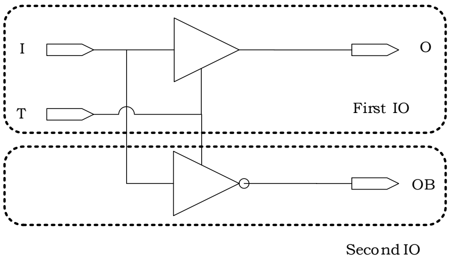
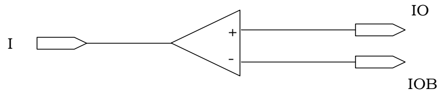
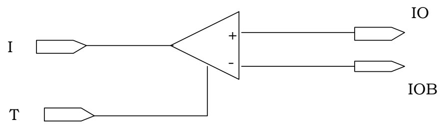
The valid parameter values are listed as follows:

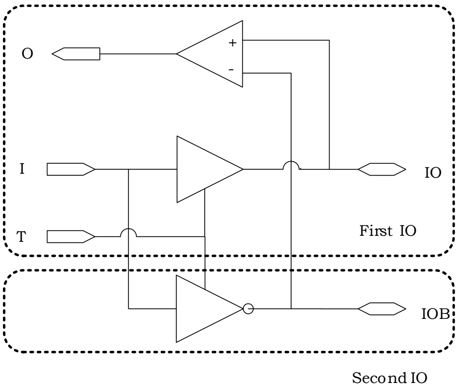
Table 2-29 Valid Parameter Values

<table>
<tr><th colspan="4">GTP_IOBUF</th></tr>
<tr><th>IOSTANDARD</th><th>SLEW_RATE</th><th>TERM_DDR</th><th>DRIVE_STRENGTH</th></tr>
<tr><td>LVTTL33</td><td rowspan="20">FAST/SLOW</td><td rowspan="7">None</td><td rowspan="3">"4", "6", "12", "16", "24"</td></tr>
<tr><td>PCI33</td></tr>
<tr><td>LVCMOS33</td></tr>
<tr><td>LVCMOS25</td><td rowspan="2">"4", "8", "12", "16"</td></tr>
<tr><td>LVCMOS18</td></tr>
<tr><td>LVCMOS15</td><td>"4", "8", "12",</td></tr>
<tr><td>LVCMOS12</td><td>"2", "6",</td></tr>
<tr><td>SSTL25_I</td><td>OFF/ON</td><td rowspan="13">None</td></tr>
<tr><td>SSTL25_II</td><td>OFF/ON</td></tr>
<tr><td>SSTL18_I</td><td>OFF/ON</td></tr>
<tr><td>SSTL18_II</td><td>OFF/ON</td></tr>
<tr><td>SSTL15_I</td><td>OFF/ON</td></tr>
<tr><td>SSTL15_II</td><td>OFF/ON</td></tr>
<tr><td>HSTL18_I</td><td>OFF/ON</td></tr>
<tr><td>HSTL18_II</td><td>OFF/ON</td></tr>
<tr><td>HSTL15_I</td><td>OFF/ON</td></tr>
<tr><td>SSTL15_I</td><td>ON</td></tr>
<tr><td>SSTL15_II</td><td>ON</td></tr>
<tr><td>HSTL15_I</td><td>ON</td></tr>
</table>

The table below lists the most commonly used GTPs for differential I/O.

Table 2-30 Differential I/O GTPs

GTP Name	Description	Illustration
GTP_INBUFDS	Differential input driving function. INBUFDS has two inputs: I and IB, representing the P-channel and N-channel input pins of the differential pair respectively	
GTP_INBUFGDS	Differential clock input supported	
GTP_IOBUFDS	True differential input and output supported	
GTP_OUTBUFCO	Pseudo-differential output driving function supported	
GTP_OUTBUFTCO	Pseudo-differential output driving function and tri-state output supported	
GTP_OUTBUFDS	True differential output function. supported Supported IO input standards are: "LVDS", "MINI-LVDS", "SUB-LVDS", and "TMDS"	
GTP_OUTBUFTDS	True differential output function supported. Supported IO input standards are: "LVDS", "MINI-LVDS", "SUB-LVDS","TMDS"	

GTP Name	Description	Illustration
GTP_IOBUFCO	Single-ended input and pseudo-differential output driving function	

➢ GTP_INBUFDS

Ports are described as follows:

Table 2-31 GTP_INBUFDS Port Description

Port	Direction	Function Description
I	Input	Noninverting differential input
IB	Input	Inverting differential input
O	Output	Differential output to the chip

Parameters are described as follows:

Table 2-32 GTP_INBUFDS Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-33	Input IO standard
TERM_DIFF	string	See Table 2-33	When in differential input, the built-in terminal resistor is enabled or disabled

The valid parameter values are listed as follows:

Table 2-33 Valid Parameter Values

GTP_INBUFDS	
IOSTANDARD	**TERM_DIFF**
LVDS25	OFF/ON
MINI-LVDS	OFF/ON
LVPECL	OFF/ON
SUB-LVDS	OFF/ON
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON
HSTL18D_I	OFF/ON
HSTL18D_II	OFF/ON
HSTL15D_I	OFF/ON
SSTL25D_I	OFF/ON
RSDS	OFF/ON
PPDS	OFF/ON
TMDS	OFF/ON
SSTL25D_II	OFF/ON
BLVDS	OFF/ON
SSTL15D_I	ON
SSTL15D_II	ON
HSTL15D_I	ON

- GTP_INBUFGDS

Ports are described as follows:

Table 2-34 GTP_INBUFGDS Port Description

Port	Direction	Function Description
I	Input	Noninverting differential input
IB	Input	Inverting differential input
O	Output	Differential output to the chip

Parameters are described as follows:

Table 2-35 GTP_INBUFGDS Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	See Table 2-36	Input IO standard
TERM_DIFF	string	See Table 2-36	When in differential input, the built-in terminal resistor is enabled or disabled

The valid parameter values are listed as follows:

Table 2-36 Valid Parameter Values

GTP_INBUFGDS	
IOSTANDARD	**TERM_DIFF**
LVDS	OFF/ON
MINI-LVDS	OFF/ON
LVPECL33	OFF/ON
SUB-LVDS	OFF/ON
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON
HSTL18D_I	OFF/ON
HSTL18D_II	OFF/ON
HSTL15D_I	OFF/ON
SSTL25D_I	OFF/ON
RSDS	OFF/ON
PPDS	OFF/ON
TMDS	OFF/ON
SSTL25D_II	OFF/ON
BLVDS	OFF/ON
SSTL15D_I	ON
SSTL15D_II	ON
HSTL15D_I	ON

- GTP_IOBUFDS

Ports are described as follows:

Table 2-37 GTP_IOBUFDS Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from input buffer to the chip
T	Input	Enable signal
IO	Input/Output	IO's PAD

Port	Direction	Function Description
IOB	Input/Output	IO's PAD, opposite to the IO value

Parameters are described as follows:

Table 2-38 GTP_IOBUFDS Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	"LVDS","MINI-LVDS","SUB-LVDS", "TMDS"	Input IO standard
TERM_DIFF	string	"ON", "OFF"	When using standard inputs such as LVDS, the built-in differential terminal resistor is enabled or disabled

- GTP_OUTBUFCO

Ports are described as follows:

Table 2-39 GTP_OUTBUFCO Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	The first IO's PAD
OB	Output	The second IO's PAD, opposite to the first IO's value

Parameters are described as follows:

Table 2-40 GTP_OUTBUFCO Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	"SSTL18D_I", "SSTL18D_II", "SSTL15D_I", "SSTL15D_II", "HSTL15D_I", "SSTL25D_I", "SSTL25D_II", "SSTL15D_I_CAL", "SSTL15D_II_CAL", "HSTL15D_I_CAL", "LVPECL", "RSDS", "PPDS", "BLVDS"	Input IO standard

- GTP_OUTBUFTCO

Ports are described as follows:

Table 2-41 GTP_OUTBUFTCO Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	The first IO's PAD
OB	Output	The second IO's PAD, opposite to the first IO's value
T	Input	Enable

Parameters are described as follows:

Table 2-42 GTP_OUTBUFTCO Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	"SSTL18D_I", "SSTL18D_II", "SSTL15D_I", "SSTL15D_II", "HSTL15D_I", "SSTL25D_I", "SSTL25D_II", "SSTL15D", "HSTL15D", "LVPECL", "RSDS", "PPDS", "BLVDS"	Input IO standard

- GTP_OUTBUFDS

Ports are described as follows:

Table 2-43 GTP_OUTBUFDS Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	The first IO's PAD
OB	Output	The second IO's PAD, opposite to the first IO's value

Parameters are described as follows:

Table 2-44 GTP_OUTBUFDS Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	"LVDS","MINI-LVDS","SUB-LVDS","TMDS"	Input IO standard

- GTP_OUTBUFTDS

Ports are described as follows:

Table 2-45 GTP_OUTBUFTDS Port Description

Port	Direction	Function Description
I	IN	Single-ended signal input
O	OUT	The first IO's PAD
OB	OUT	The second IO's PAD, opposite to the first IO's value
T	IN	Enable signal

Parameters are described as follows:

Table 2-46 GTP_OUTBUFTDS Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	"LVDS","MINI-LVDS", "SUB-LVDS","TMDS"	Input IO standard

- GTP_IOBUFCO

Ports are described as follows:

Table 2-47 GTP_IOBUFCO Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from input buffer to the chip
T	Input	Enable output buffer
IO	Input/Output	The first IO's PAD
IOB	Input/Output	The second IO's PAD, opposite to the first IO's value

Parameters are described as follows:

Table 2-48 GTP_IOBUFCO Parameter Description

Parameter Name	Type	Valid Values	Function Description
IOSTANDARD	string	"SSTL18D_I", "SSTL18D_II", "SSTL15D_I", "SSTL15D_II", "HSTL15D_I", "SSTL25D_I", "SSTL25D_II", "SSTL15D_I", "SSTL15D_II", "HSTL15D", "LVPECL", "RSDS", "PPDS", "BLVDS"	Input IO standard
TERM_DDR	string	"ON", "OFF"	When inputting HSTL, SSTL standards, the built-in terminal resistor can be enabled or disabled

2.3 IO LOGIC

This section mainly describes the IO LOGIC of the Logos Family products.

The IO LOGIC module is located between the IO BUFFER and the core Fabric of FPGA. IO LOGIC manages the signals the IO BUFFER outputs to or receives from the FPGA pins. In differential I/O standard applications, two IO LOGICs (TRUE and COMP) and two IO BUFFERs (TRUE and COMP) form a differential pair.

IO LOGIC supports various high-speed interfaces, in addition to direct data input/output and I/O register input/output, it also supports the following functions:

- For high-speed interfaces, it supports 1:2; 1:4; 1:7; 1:8 input Deserializers.
- For high-speed interfaces, it supports 2:1; 4:1; 7:1; 8:1 output Serializers.
- Built-in IO delay function, which can dynamically/statically adjust input/output delay.
- Built-in input FIFO, mainly used for clock domain conversion from external non-continuous DQS (for DDR memory interface) to internal continuous clock and compensating for the phase difference between the sampling clock and internal clock in some special Generic DDR applications.

2.3.1 IO DELAY Unit

Each I/O PAD contains an IO DELAY unit that can be used for providing an input or output delay of 15 steps * 25ps = 375ps; it can provide a DELAY mode that is either statically configured or dynamically adjusted. IO DELAY is commonly used to adjust the sampling window or to fine-tune the output timing, improving SSO (simultaneous switching output).

The structure of the IO DELAY unit is shown in the following diagram.

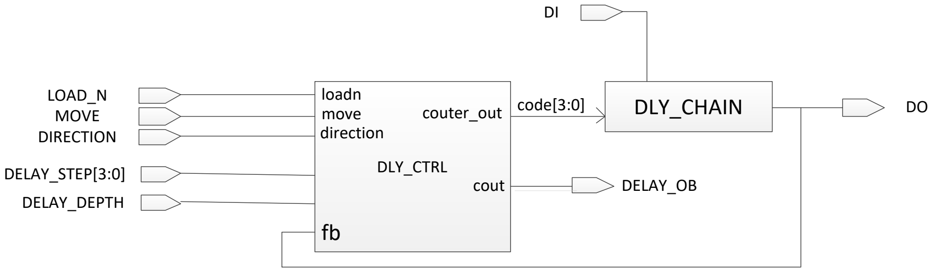


Figure 2-18 IODELAY Unit

As Figure 2-18 shown, when LOAD_N=0, DLY_CTRL adopts a static delay configuration of DELAY_STEP; when LOAD_N=1, DLY_CTRL uses a dynamic delay adjustment mode, with the dynamic delay vector being transmitted by MOVE and DIRECTION.

Dynamic delay adjustment is achieved through the combined action of MOVE, DIRECTION, and LOAD_N.

When LOAD_N=1, and SC_IODLY_DEGL=0, if DIRECTION is 0 and code[3:0] is less than 15, then the output code increases by 1 for each falling edge of MOVE; if code[3:0] is greater than 15, the cout goes high, the adjustment overflows, and the output code remains unchanged; if DIRECTION is 1, the output code decreases by 1 for each falling edge of MOVE, and when the output code reduces to 0, cout goes high, and adjustment overflows.

To eliminate glitches in the output of the IO DELAY unit, a SC_IODLY_DEGL signal has been added to the module, as shown in the figure below.

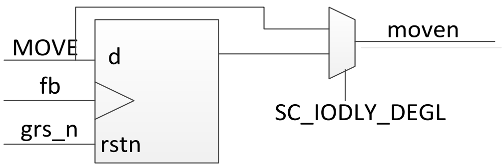


Figure 2-19 SC_IODLY_DEGEL Structure

At the input end, MOVE and DI are in separate asynchronous clock domains, while the timing of code during dynamic adjustment is consistent with MOVE. When SC_IODLY_DEGL=0, code and DI are asynchronous, and will cause glitches after passing through the IO DELAY unit. When SC_IODLY_DEGL=1, the active moven is pulled into the fb clock domain, which is the DI clock domain, synchronizing code with DI and eliminating the glitches in the output of the IO DELAY unit.

DLY_CHAIN is a delay unit that provides a delay of 15 steps * 25ps= 375ps plus intrinsic delay (matched to DQSL intrinsic delay), with code[3:0] selecting the delay step.

The PDS software library provides dedicated primitives for the IO DELAY unit, allowing users to instantiate the GTP_IODELAY prototype module in the source code Verilog/VHDL. Taking Verilog instantiation as an example:

```
GTP_IODELAY #(
.DELAY_STEP    (4'd0         ) ,
.DELAY_DEPTH (4              )
)u_GTP_IODELAY
(
.DI                 (DI           ),
.DO                 (DO           ),
.LOAD_N          (LOAD_N     ),
.MOVE             (MOVE        ),
.DIRECTION     (DIRECTION),
.DELAY_OB       (DELAY_OB )
);
```

The parameter and signal descriptions for the IO DELAY prototype module are as follows:

Table 2-49 GTP_IODELAY Parameter Description

Parameter	Description
DELAY_STEP[3:0]	Step number setting, 0-15 corresponds to a delay of 1-16 steps, used for static adjustment.
DELAY_DEPTH	DELAY depth setting. A setting of 4 indicates 2^4.

Table 2-50 GTP_IODELAY Port Description

Port Signal	Direction	Description
DI	Input	Input data
DO	Output	Output data
DIRECTION	Input	Set to 0 to dynamically increase the delay step, set to 1 to dynamically decrease the delay step
MOVE	Input	The falling edge triggers dynamic fine-tuning, increasing or decreasing one step depending on the DIRECTION.
LOAD_N	Input	Active-low, resets the delay step to the DELAY_STEP value.
DELAY_OB	Output	Overflow indicator. It goes high when internal delay step is 127 with DIRECTION reset; it goes high when delay step is 0 with DIRECTION set.

The reuse of programmable output delay units and programmable input delay units can be achieved through configuration bit control.

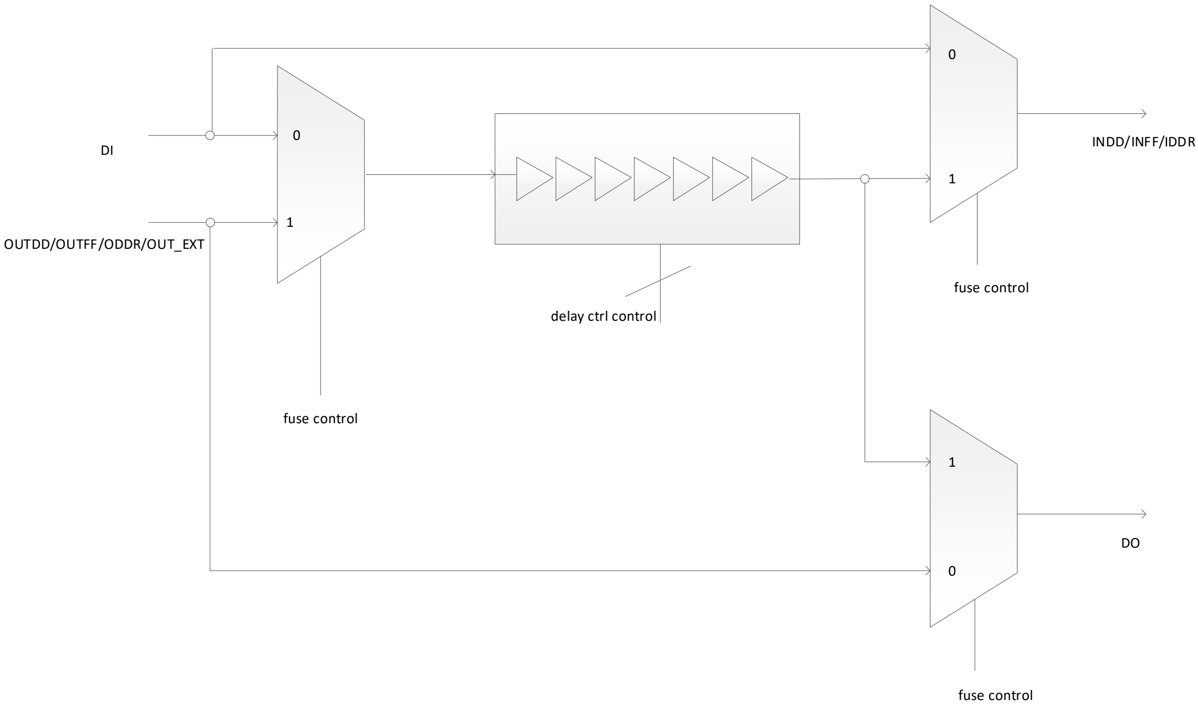


Figure 2-20 IO DELAY Reuse

2.3.2 Register Unit

The functions of input and output registers of the IO LOGIC are shown below.

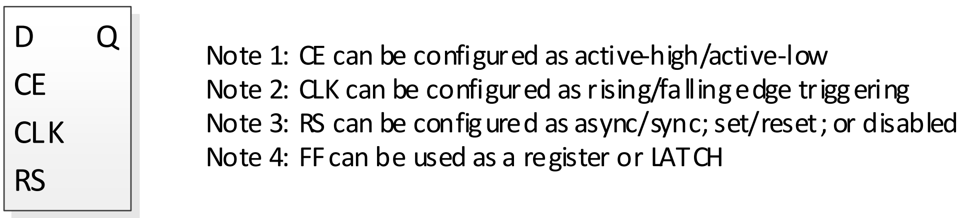


Figure 2-21 IO LOGIC Register Functions

The structure of input and output registers of IO LOGIC is shown in the following diagram.

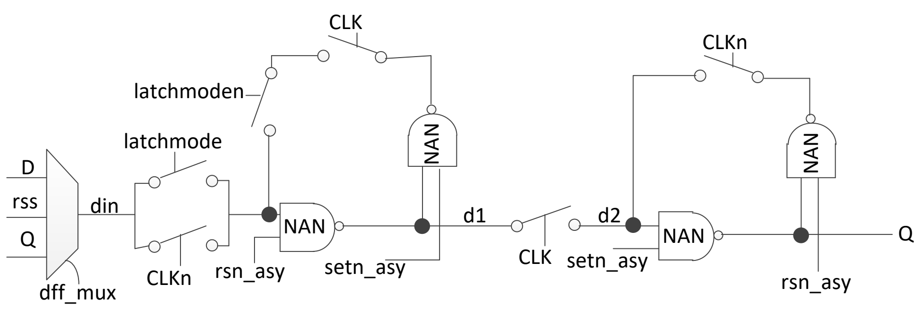


Figure 2-22 IO LOGIC Register Structure

When dff_mux is configured as synchronous, with CE active and RS inactive, select D; when configured as either synchronous or asynchronous, with RS active, select rss, with rss being 1 when RS is configured to "set", and rss being 0 when RS is configured to "reset"; when configured as synchronous, with CE inactive and RS inactive, select Q. When configured as asynchronous, D is selected by default.

In Figure 2-22, latchmode is 1, when configured as LATCH mode; it is 0 controlled by asynchronous RS when configured as FF mode; it is 1 when RS is active.

In Figure 2-22, the CLK comes from CLK_SYS_I (input register) or CLK_SYS_O (output register).

rsn_asy and setn_asy are asynchronous, active-low reset and set signals. Where RS is configured as asynchronous reset, rsn_asy has input, and setn_asy has no input. When RS is configured as asynchronous set, rsn_asy has no input, and setn_asy has input. When RS is configured as synchronous, neither rsn_asy and setn_asy have input.

The input and output registers can be selected by checking the box under "IO_REGISTER" for the corresponding IO in PDS>UCE>Device>I/O Tabs, as shown in the following diagram.

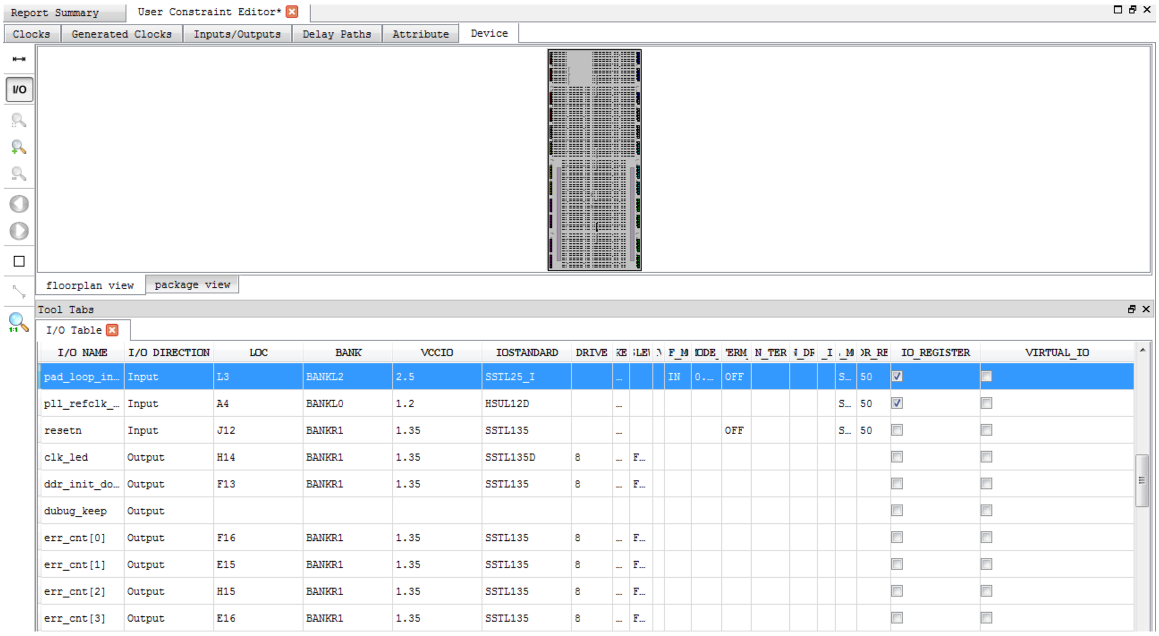


Figure 2-23 IO Register Constraint Method

2.3.3 Input and Output Logic Units

The IO LOGIC of Logos Family products includes input logic and output logic units, which can flexibly support various application interfaces. In addition to the commonly used direct input/output and input/output registers, the IO LOGIC has data input-output rate conversion capabilities to support DDR memory interfaces.

The input logic unit can support four types of rate conversion modes: 1:2, 1:4, 1:7, and 1:8

The output logic unit can support four types of rate conversion modes: 2:1, 4:1, 7:1, and 8:1

1) Input Logic Units

The input logic unit primarily consists of two parts: IFIFO and GEAR LOGIC. IFIFO is mainly used in the DDR memory interface, with functions including clock domain conversion from external non-continuous DQS to internal continuous clocks, realigning DDR3 read data, certain special Generic DDR applications, and compensating for phase differences between the sampling clock and the internal clock; GEAR LOGIC has the main functions of expanding the bit width of the sampled data and transferring it from the high-speed DESCLK to a lower-speed system clock domain for Fabric processing.

GTP_IDDR_E2 is a data deserializer, with the function as shown below, supporting edge-aligned SAME_PIPELINED mode.

Figure 2-24 GTP_IDDR_E2 Functional Diagram

```
GTP_IDDR_E2 #
(
.GRS_EN        ("TRUE")
) u_ GTP_IDDR_E2 (
.RS            (RS     ),
.CLK           (CLK    ),
.DI            (DI     ),
.Q1            (Q1     ),
.Q0            (Q0     )
);
```

The parameter and signal descriptions for GTP_IDDR_E2 are as follows:

Table 2-51 GTP_IDDR_E2 Parameter & Port Description

Parameter	Description
GRS_EN	Global reset enable, with "TRUE" indicating global reset is enabled, and "FALSE" indicating global reset is disabled.

Table 2-52 GTP_IDDR_E2 Parameter & Port Description

Port Signal	Direction	Description
D	Input	Data input
RS	Input	Local reset signal

Port Signal	Direction	Description
CLK	Input	Input system clock
Q0	Output	Data output
Q1	Output	Data output

The timing of GTP_IDDR_E2 is shown in the following diagram:

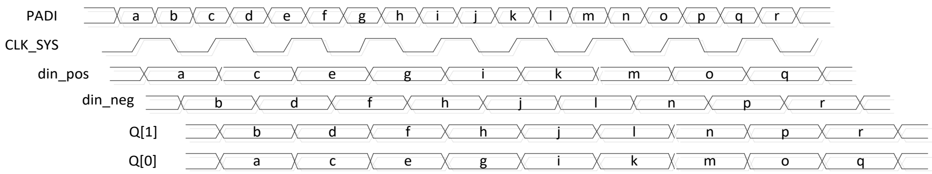


Figure 2-25 GTP_IDDR_E2 Timing Diagram

GTP_ISERDES is configured into different operating modes through the parameter ISERDES_MODE, including: IDDR, IMDDR, IDES4, IMDES4, IDES7, IDES8, and IMDES8.

The PDS software library provides dedicated primitives for the convenience of users utilizing the input logic unit, allowing users to instantiate the GTP_ISERDES prototype module in the source code (Verilog/VHDL). Taking Verilog instantiation as an example:

```
GTP_ISERDES #(
  .ISERDES_MODE    ("IDDR"),
.GRS_EN             ("TRUE" ),
.LRS_EN             ("TRUE" )
) u_ISERDES(
.DI                 (DI           ),
.ICLK               (ICLK         ),
.DESCLK             (DESCLK       ),
.RCLK               (RCLK         ),
.WADDR              (WADDR        ),
.RADDR              (RADDR        ),
.RST                (RST          ),
.DO                 (DO           )
);
```

The parameter and signal descriptions for GTP_ISERDES are as follows:

Table 2-53 GTP_ISERDES Parameter Description

Parameter	Description
ISERDES_MODE	ISERDES operating mode configuration, with the default value being IDDR, and other

Parameter	Description
	configurable parameters including "IDDR", "IMDDR", "IDES4", "IMDES4", "IDES7", "IDES8", and "IMDES8"
GRS_EN	Global reset enable, with "TRUE" indicating global reset is enabled, and "FALSE" indicating global reset is disabled.
LRS_EN	Local reset enable, with "TRUE" indicating local reset is enabled, and "FALSE" indicating local reset is disabled.

Table 2-54 GTP_ISERDES Port Description

Port Signal	Direction	Description
DO[7:0]	Output	Output data
DI	Input	PAD input signal
ICLK	Input	Input clock shared by IMDDR, IMDES4, and IMDES8
DESCLK	Input	Deserialization clock
RCLK	Input	Input clock shared by IDDR, IDES4, IDES7, and IDES8
WADDR[2:0]	Input	Write address signal for FIFO connected to DDC
RADDR[2:0]	Input	Read address signal for FIFO connected to DDC
RST	Input	Reset signal, active-high

GTP_ISERDES is typically used in conjunction with GTP_INBUF, GTP_INBUFG, GTP_INBUFDS, and GTP_INBUFGDS. The following diagram illustrates the connection method of GTP_ISERDES with GTP_INBUFDS as an example.

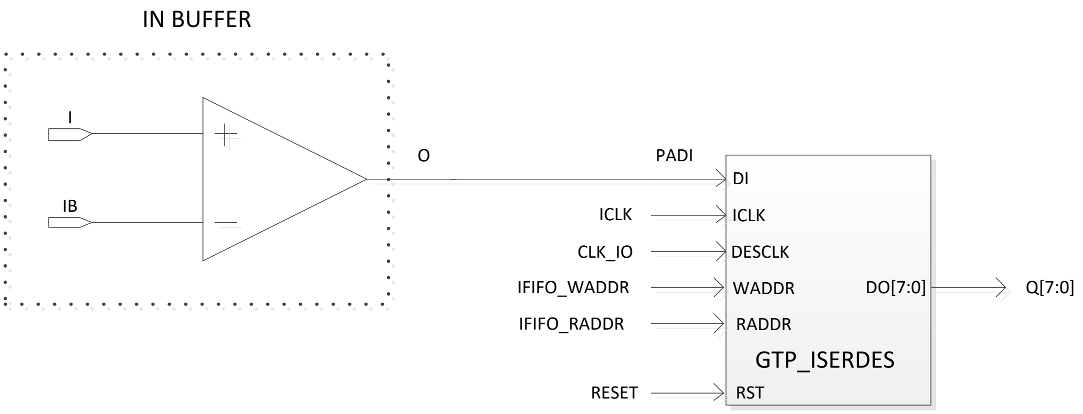


Figure 2-26 Common Connection Methods for GTP_ISERDES

The different operating modes of the input logic are introduced below.

- IDDR

When the input logic is configured into IDDR mode, its functional diagram can be simplified as below.

Figure 2-27 IDDR Functional Diagram

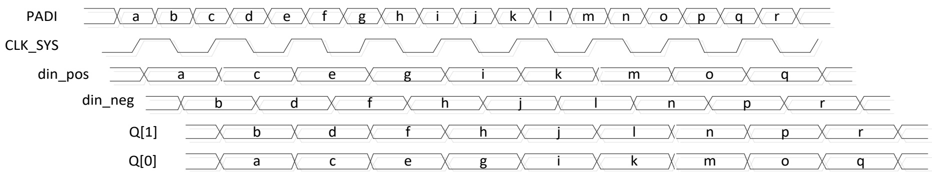


Figure 2-28 IDDR Timing Diagram

Note: In the timing diagram, the letters, such as a, b, c, d, represent the position information of bit data, which in terms of data, is valued as "0" or "1".

➢ IMDDR

When the input logic is configured into IMDDR mode, compared to the IDDR structure, IMDDR enables the IFIFO. Its functional diagram can be simplified as below.

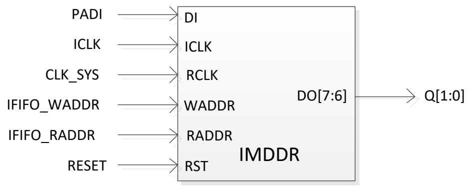


Figure 2-29 IMDDR Block Diagram

The IMDDR timing is as follows.

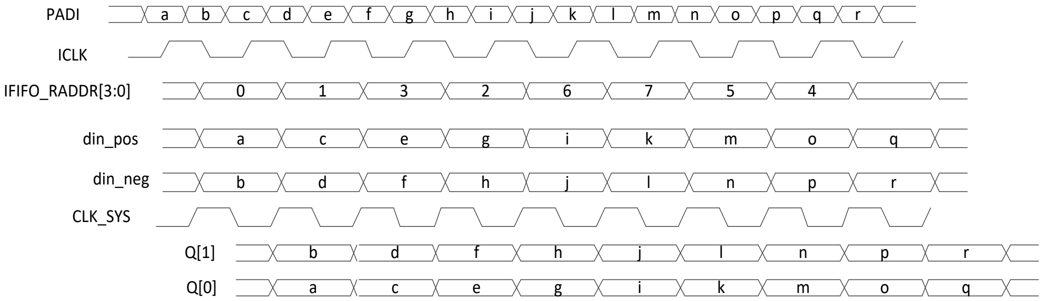


Figure 2-30 IMDDR Timing Diagram

➢ IDES4

When the input logic is configured into IDES4, it is used in conjunction with GTP_INBUF, GTP_INBUFG, GTP_INBUFDS, or GTP_INBUFGDS. Its functional diagram can be simplified as below.

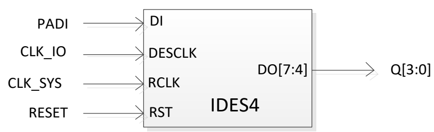


Figure 2-31 IDES4 Block Diagram

The IDES4 timing is shown below.

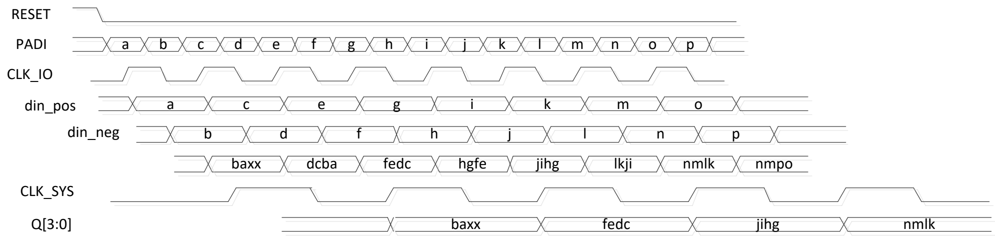


Figure 2-32 IDES4 Timing Diagram

- IMDES4

When the input logic is configured into IMDES4, compared to IDES4, IMDES4 enables the IFIFO. Its functional diagram can be simplified as below.

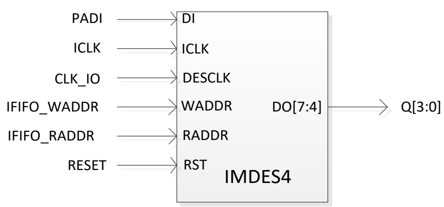


Figure 2-33 IMDES4 Functional Diagram

The IMDES4 timing is as follows.

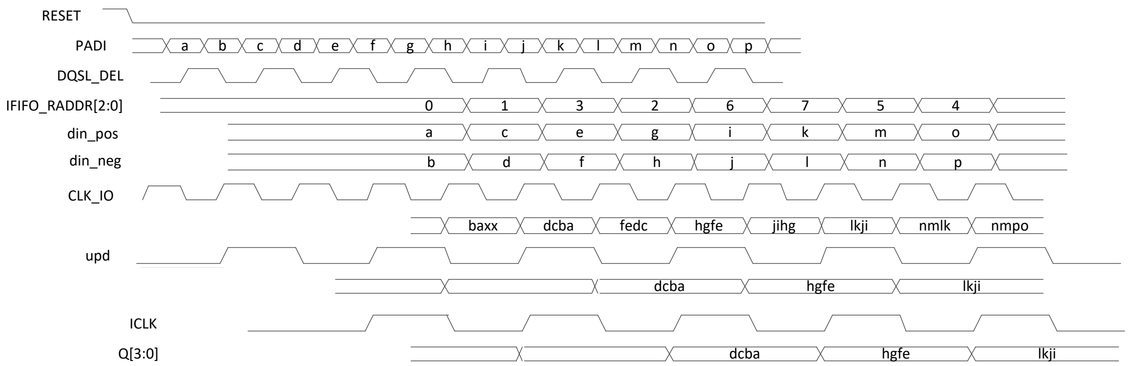


Figure 2-34 IMDES4 Timing Diagram

The upd signal becomes active one clk cycle after the asynchronous RESET and takes effect once every two CLK_IO cycles.

- IDES7

When the input logic is configured into IDES7, its usage is the same as IDES4. Its functional diagram can be simplified as below.

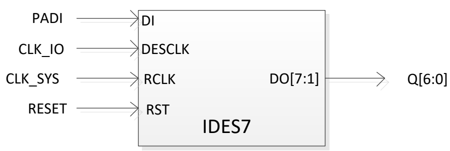


Figure 2-35 IDES7 Functional Diagram

The IDES7 timing is shown below.

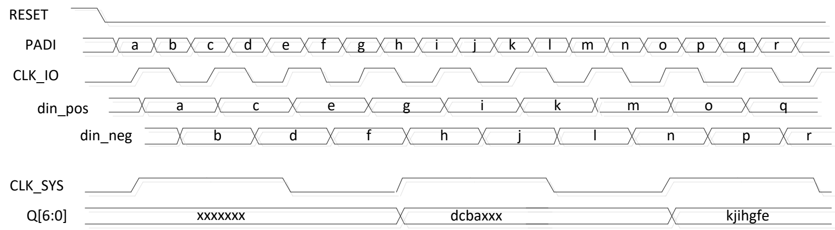


Figure 2-36 IDES7 Timing Diagram

- IDES8

When the input logic is configured into IDES8, its usage is the same as IDES4. Its functional diagram can be simplified as below.

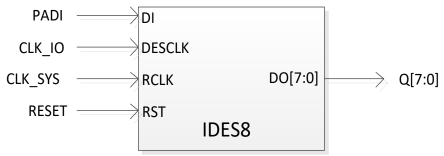


Figure 2-37 IDES8 Block Diagram

The IDES8 timing is shown below.

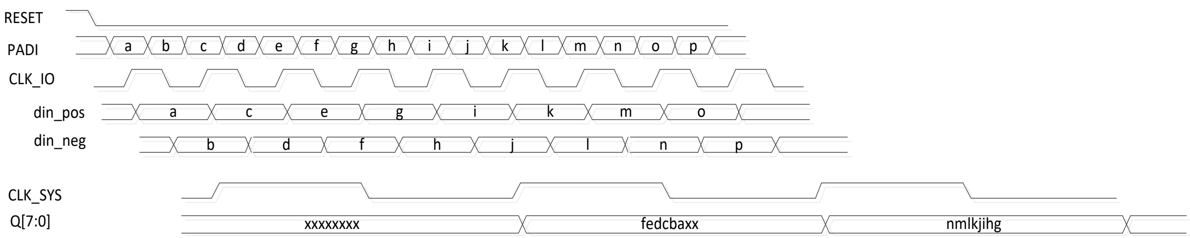


Figure 2-38 IDES8 Timing Diagram

- IMDES8

When the input logic is configured into IMDES8, compared toIDES8, IMDES8 enables the IFIFO. Its functional diagram can be simplified as below.

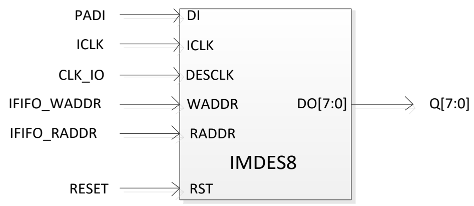


Figure 2-39 IMDES8 Functional Diagram

The IMDES8 timing is shown below.

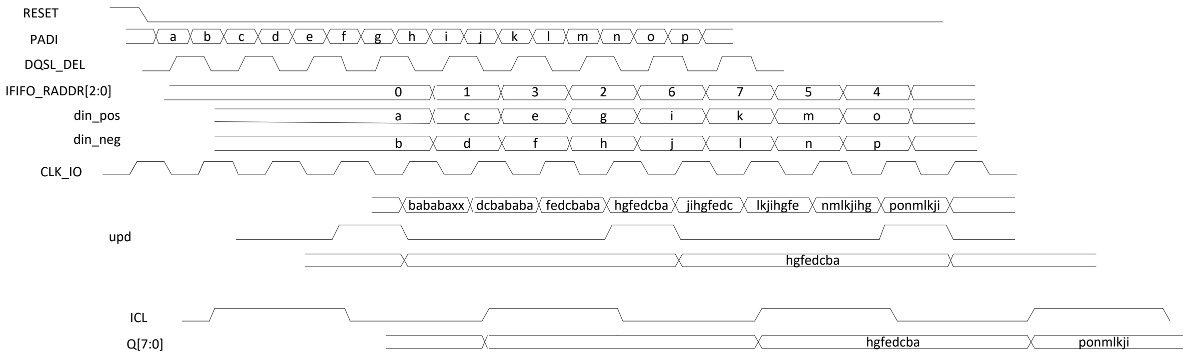


Figure 2-40 IMDES8 Functional Diagram

During IMDES8 functionality, the upd signal becomes active two clk cycles after the asynchronous rst and takes effect once every four clk cycles.

1) Output Logic Units

The primary function of the output logic is to transfer data from the Fabric from the CLK_SYS to the SERCLK clock domain and convert it into a high-speed serial data stream for transmission. Each output logic unit can support an output rate conversion of 2:1, 4:1, 7:1, and 8:1.

GTP_ODDR_E2 supports edge-aligned DDR2TO1 rate conversion. The system block diagram is shown below.

Figure 2-41 GTP_ODDR_E2 Functional Diagram

```
GTP_ODDR_E2#
(
.GRS_EN       ("TRUE")
) u_ GTP_ODDR_E2 (
. RS          (RS        ),
.CLK          (CLK       ),
. D0          (D0        ),
.D1           (D1        ),
. T           (T         ),
. Q           (Q         ),
. TQ          (TQ        )
);
```

The parameter and signal descriptions for GTP_ODDR_E2 are as follows:

Table 2-55 GTP_ODDR_E2 Parameter & Port Descriptions

Port Signal	Input/Output	Description
GRS_EN	Parameter	Global reset enable, with "TRUE" indicating global reset is enabled, and "FALSE" indicating global reset is disabled.
RS	Input	Local reset/set signal
CLK	Input	Input system clock
D0	Input	Input data signal
D1	Input	Input data signal
T	Input	Strobe data input
Q	Output	Data output
TQ	Output	Output strobe

The timing of GTP_ODDR_E2 is shown in the following diagram:

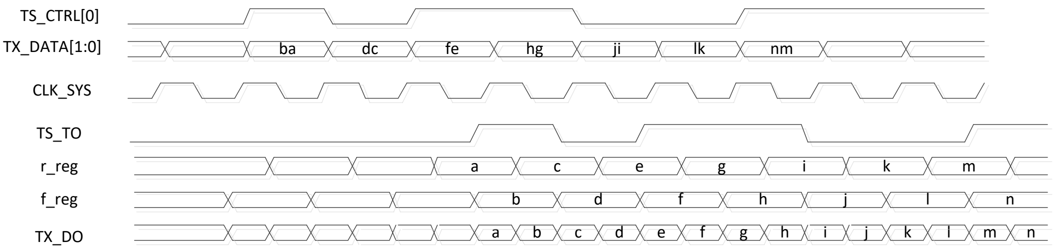


Figure 2-42 GTP_ODDR_E2 Timing Diagram

GTP_OSERDES can be configured into different operating modes through the parameter OSERDES_MODE, including: ODDR, OMDDR, OSER4, OMSER4, OSER7, OSER8, and OMSER8.

The PDS software library provides dedicated primitives for the convenience of users utilizing the output logic unit, allowing users to instantiate the GTP_OSERDES prototype module in the source code (Verilog/VHDL). Taking Verilog instantiation as an example:

```
GTP_OSERDES #(
    .OSERDES_MODE ("ODDR" ),
    .WL_EXTEND      ("FALSE "),
    .GRS_EN           ("TRUE"    ),
    .LRS_EN           ("TRUE"    ),
    .TSDDR_INIT      (1'b0          )
) u_OSERDES(
    .DO                   (DO              ),
  .TQ                   (TQ              ),
  .DI                    (DI              ),
  .TI                   (TI              ),
```

```
    .RCLK        (RCLK     ),
    .SERCLK      (SERCLK   ),
    .OCLK        (OCLK     ),
    .RST         (RST      )
);
```

The parameter and signal descriptions for GTP_OSERDES are as follows:

Table 2-56 GTP_OSERDES Parameter Description

Parameter	Description
OSERDES_MODE	OSERDES operating mode configuration, with the default value being ODDR, and other configurable parameters including "OMDDR", "OSER4", "OMSER4", "OSER7", "OSER8", and "OMSER8"
GRS_EN	Global reset enable, with "TRUE" indicating global reset is enabled, and "FALSE" indicating global reset is disabled.
LRS_EN	Local reset enable, with "TRUE" indicating local reset is enabled, and "FALSE" indicating local reset is disabled.
TSDDR_INIT	TQ initial state control, with 1'b0 indicating TQ initial state of 0, and 1'b1 indicating TQ initial state of 1
WL_EXTEND	Write Leveling extension, with the value of "TRUE" or "FALSE"

Table 2-57 GTP_OSERDES Port Description

Port Signal	Direction	Description
DO	Output	Output data
TQ	Output	Tri-State Control Output
DI[7:0]	Input	Input data
TI[3:0]	Input	Tri-state control input
OCLK	Input	Data output clock
SERCLK	Input	Serial Clock
RCLK	Input	Input Clock
RST	Input	Reset signal, active-high

GTP_OSERDES is typically used in conjunction with GTP_OUTBUF, GTP_OUTBUFDS, GTP_OUTBUFCO, GTP_OUTBUFTCO, GTP_OUTBUFTDS, and GTP_OUTBUFT. The diagram below takes GTP_OUTBUFTDS as an example to illustrate the connection relationship with GTP_OSERDES.

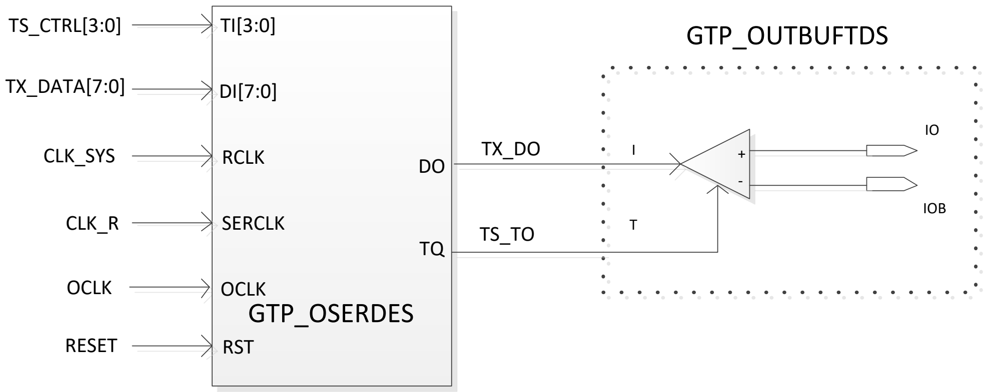


Figure 2-43 Common Connection Methods of GTP_OSERDES

When using GTP_OSERDES, there are two modes: with and without tri-state control. When there is no tri-state control, TI and TQ are not available in GTP_OSERDES.

The different operating modes of the output logic are introduced below.

➢ ODDR

When the output logic is configured into ODDR mode, its functional diagram can be simplified as below.

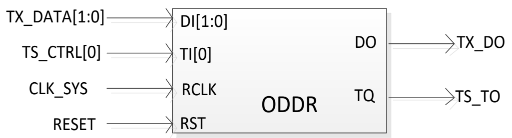


Figure 2-44 ODDR Functional Diagram

The ODDR timing is shown below.

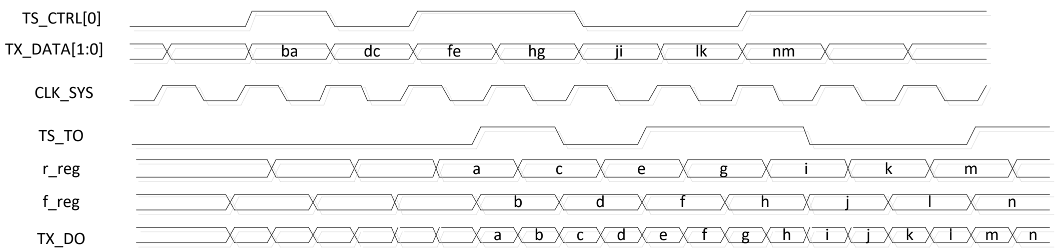


Figure 2-45 ODDR Timing Diagram

For ODDR, OMDDR, OSER4, OMSER4, OSER8, and OMSER8, there are two forms: output with tri-state control TS_TO as shown above, and output without tri-state; for OSER7, there if only output without TS_TO.

➢ OMDDR

When the output logic is configured into OMDDR mode, its functional diagram can be simplified as below.

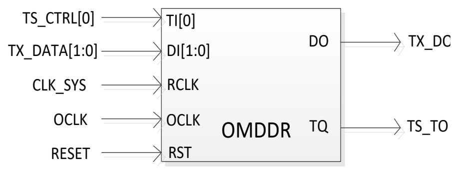


Figure 2-46 OMDDR Block Diagram

Compared with ODDR, OMDDR has one additional clock domain transition from CLK_SYS to OCLK. The timing is shown below.

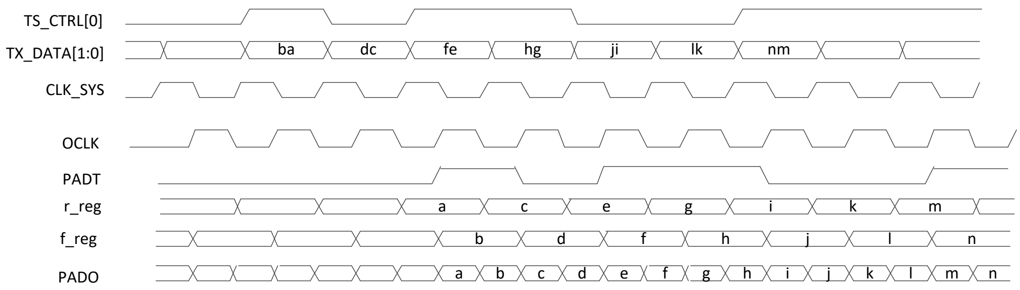


Figure 2-47 OMDDR Timing Diagram

➢ OSER4

When the output logic is configured into OSER4 mode, it is used in conjunction with GTP_OUTBUFT, GTP_OUTBUFTDS or GTP_OUTBUFTCO. Its functional diagram can be simplified as below.

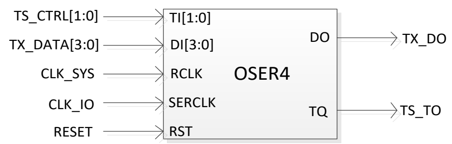


Figure 2-48 OSER4 Functional Diagram

The OSER4 timing is shown below.

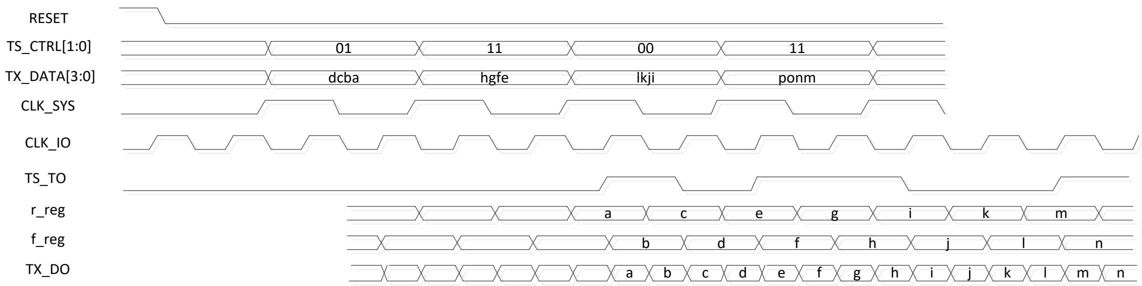


Figure 2-49 OSER4 Timing Diagram

➢ OMSER4

When the output logic is configured into OMSER4 mode, its functional diagram can be simplified as below.

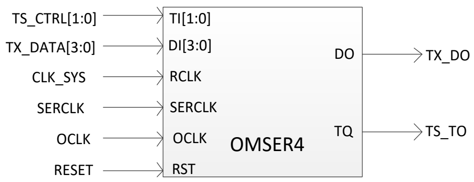


Figure 2-50 OMSER4 Block Diagram

Compared with OSER4, OMSER4 has one additional clock domain transition from SERCLK to OCLK. The timing for OMSER4 is as follows.

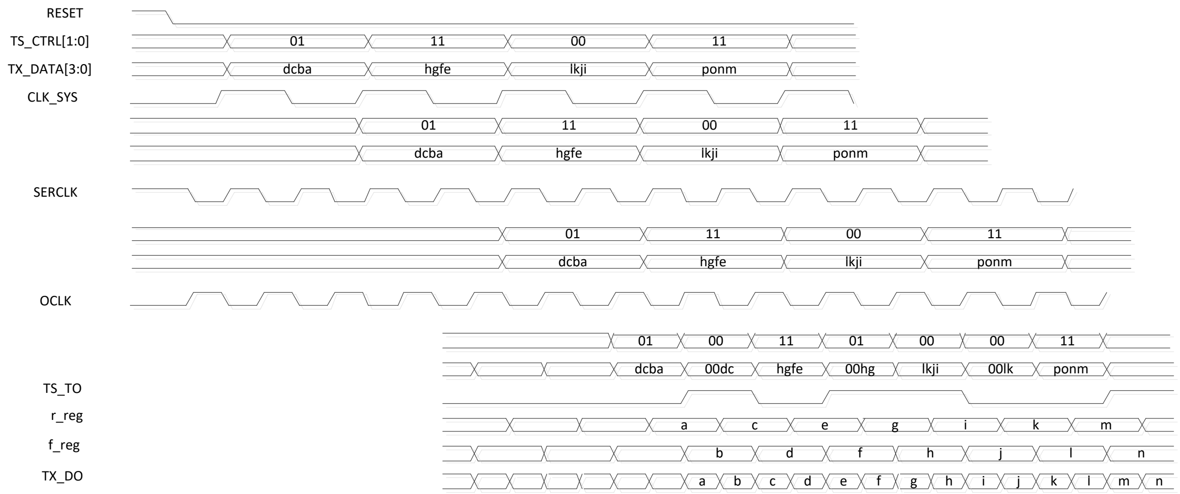


Figure 2-51 OMSER4 Timing Diagram

➢ OSER7

When the output logic is configured into OSER7 mode, it is used in conjunction with GTP_OUTBUF, GTP_OUTBUFDS, or GTP_OUTBUFCO. Its functional diagram can be simplified as below.

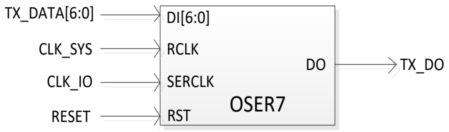


Figure 2-52 OSER7 Functional Block Diagram

The timing for OSER7 is as follows.

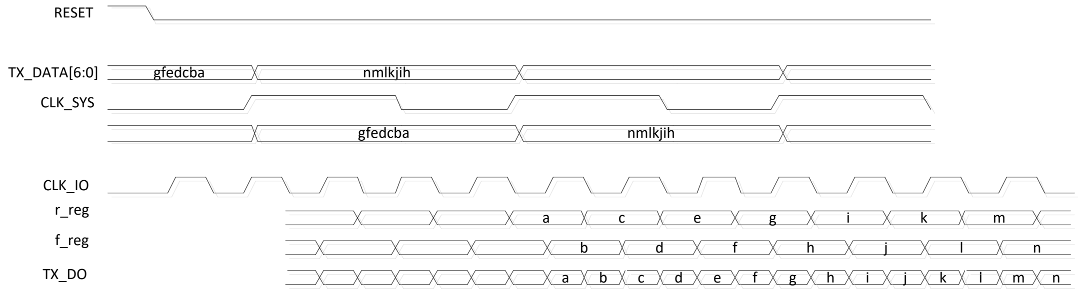


Figure 2-53 OSER7 Timing Diagram

➢ OSER8

When the output logic is configured into OSER8 mode, its usage is the same as OSER4.Its functional diagram can be simplified as below.

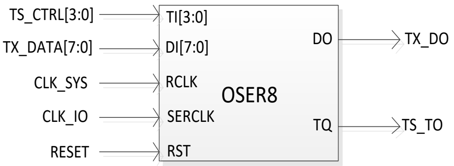


Figure 2-54 OSER8 Functional Block Diagram

The timing for OSER8 is as follows.

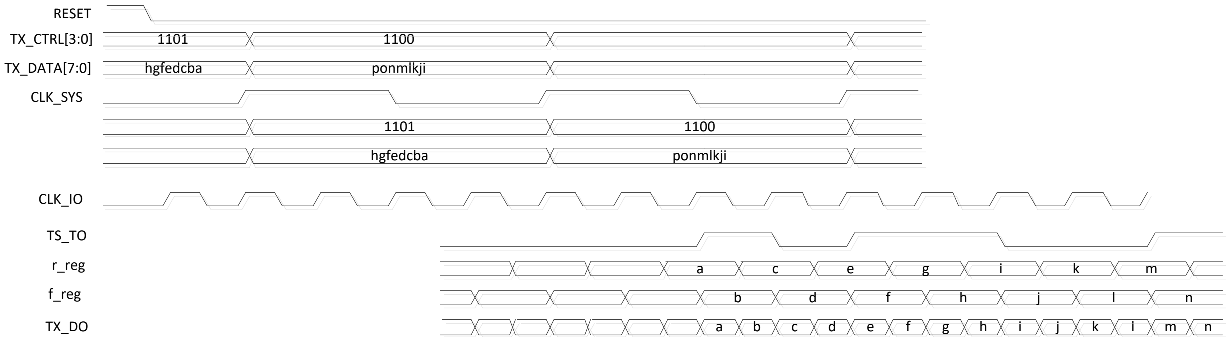


Figure 2-55 OSER8 Timing Diagram

➢ OMSER8

When the output logic is configured into OMSER8 mode, its functional diagram can be simplified as below.

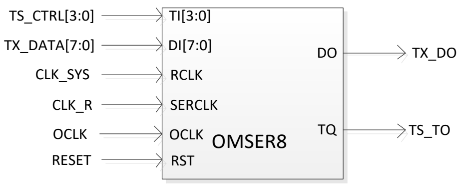


Figure 2-56 OMSER8 Block Diagram

Here, the selection for CLK_R is the DQSL interface clock with a 180-degree phase shift.

Compared with OSER8, OMSER8 has one additional clock domain transition from SERCLK to OCLK.The timing for OMSER8 is as follows.

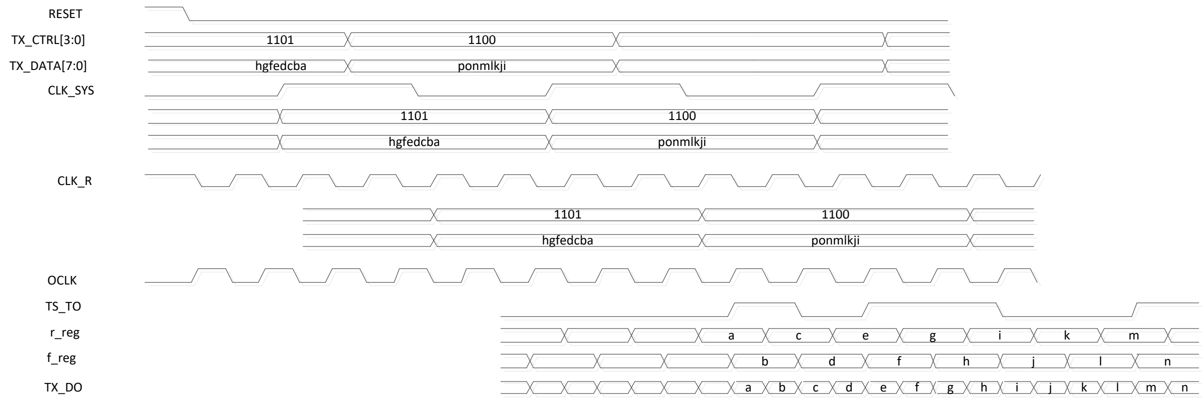


Figure 2-57 OMSER8 Timing Diagram

1) IOL Functions and Features

IOL-supported modes and corresponding applications are shown in the table below:

Table 2-58 IOL-Supported Modes and Applications

Input Mode	**Output Mode**	**Applications**
IFF	OFF/TSFF	SDR
IMDDR	OMDDR	DDR1/DDR2
IDDR	ODDR	Generic DDR
IMDES4	OMSER4	DDR2/DDR3
IDES4	OSER4	Generic DDR
IMDES8	OMSER8	DDR3
IDES8	OSER8	Generic DDR
IDES7	OSER7	Video
		7to1 LVDS

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