Compa Family CPLDs Clock Resources User Guide

(UG030003, V1.4)

(16.08.2023)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.4	16.08.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
CLKDIV	Clock Divider
PLL	Phase Lock Loop
CPLD	Complex Programmable Logic Device
PFD	Phase-Frequency Detector
VCO	Voltage Controlled Oscillator
LPF	Low Pass Filter
CP	Charge Pump
APB	Advanced Peripheral Bus
LDO	Low Drop Out regulator
SRB	Signal Relay Block

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Chapter 1 Overall Introduction

The Compa family products provide a variety of on-chip clock resources, including a global clock network, IO clock network, clock divider module (CLKDIV), clock delay unit (CLKDLY), PLL, and internal oscillator (OSC). The global clock network contains 8 dedicated GLOBAL CLOCKs and 8 GLOBAL SIGNALs evenly distributed throughout the chip. The 8 GLOBAL SIGNALs can be used as clock lines, thereby supporting up to 16 global clock lines in total. The IO clock network contains 4 IO CLOCKs dedicated to high-speed port applications. They are distributed on the upper and lower sides of the chip and can be bridged via IOCKBRG. The PGC1K/2K clock resource distribution diagram is shown in Figure 1-1:

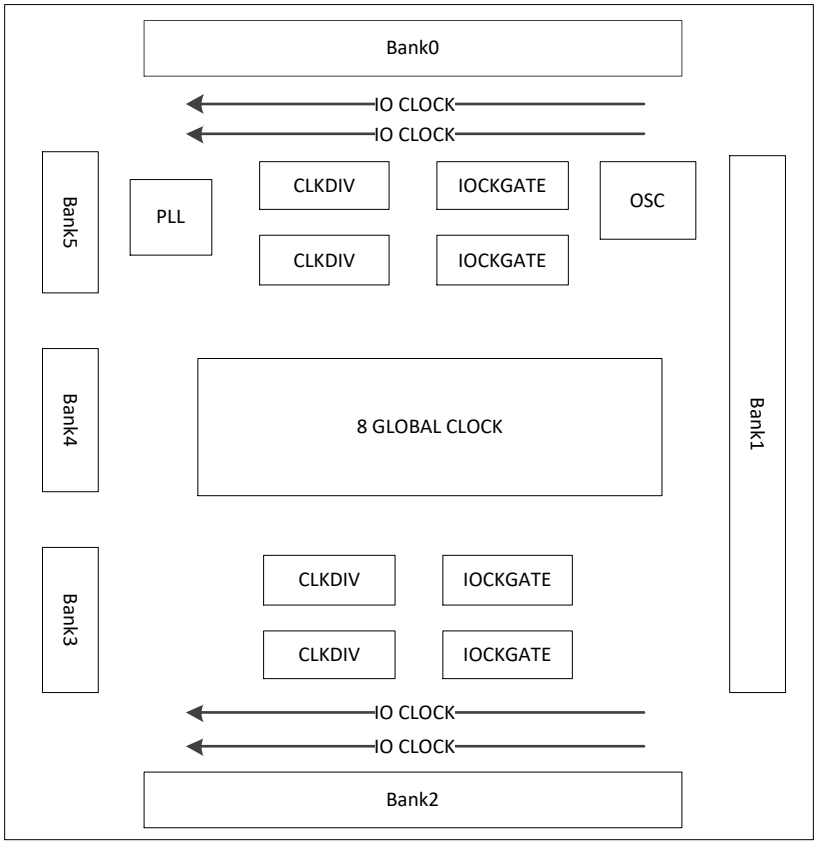

Figure 1-1 PGC1K/2K Major Clock Resource Distribution Diagram

The PGC4K/7K/10K clock resource distribution diagram is shown in Figure 1-2:

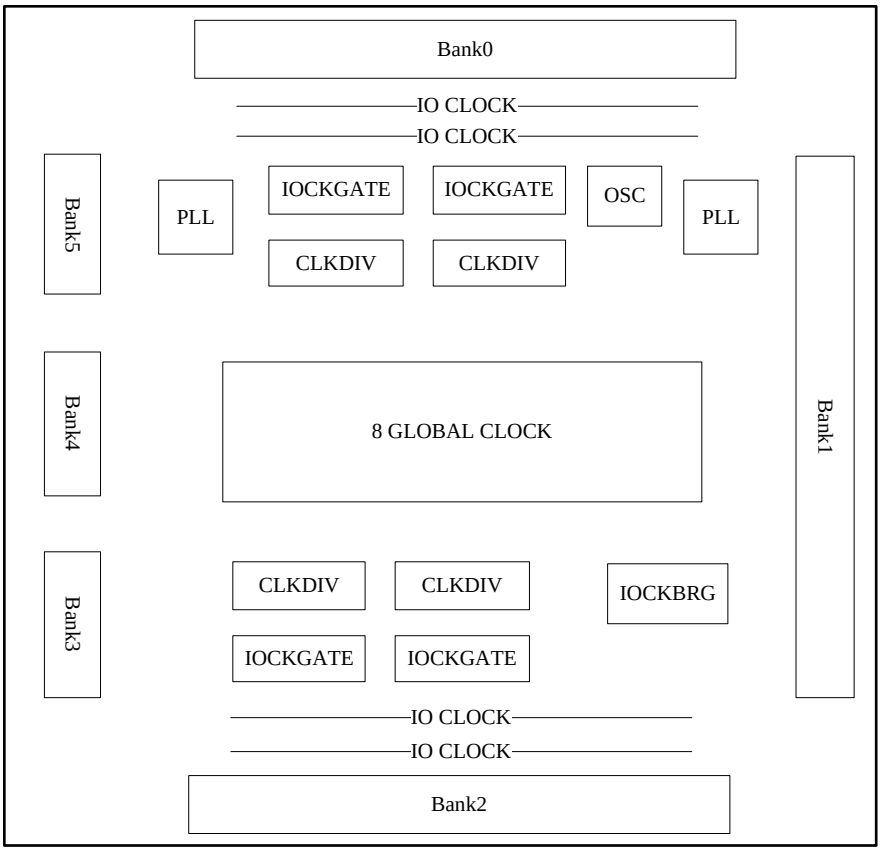

Figure 1-2 PGC4K/7K/10K Major Clock Resource Distribution Diagram

The Compa family products provide dedicated clock pins that allow dedicated clock routing within the chip to reach any GLOBAL CLOCK. Compared with general pins, using these dedicated clock input pins can avoid interference from ordinary routing resources, thus achieving better clock performance. When not used as clock inputs, these dedicated clock input pins can be used as general pins.

The number of main clock resources for Compa family products is shown in Table 1-1:

Table 1-1 Major Clock Resources of Compa Family Products

Name	**PGC1K**	**PGC2K**	**PGC4K**	**PGC7K**	**PGC10K**
PLL	1	1	2	2	2
GLOBAL CLOCK	8	8	8	8	8
GLOBAL SIGNAL	8	8	8	8	8
IO CLOCK	4	4	4	4	4
Clock divider module	4	4	4	4	4

Chapter 2 Detailed Introduction

2.1 Clock Input Pins

Compa family products provide dedicated pins related to the clock. There are three types of clock input pins, as shown in Table 2-1. The clock signal can be directly connected to the internal clock network through the clock input pin, thereby reducing interference and improving clock quality. The clock input pins support differential signals as well as single-ended signals. When receiving a single-ended signal, only the P-side can be directly connected to the internal clock network, while the N-side has to pass through an SRB. When not used as clock inputs, the clock input pins can be used as general pins.

Table 2-1 Clock Input Pins

Clock Input Pin	Symbol	Description
Global clock Input pin1	CLKxP_Bx/CLKxN_Bx	Inputs for GLOBAL CLOCK and IO CLOCK
PLL reference clock input pin2	PLLx_CLKIN_P/PLLx_CLKIN_N	PLL dedicated reference clock input
PLL feedback input clock pin	PLLx_CLKFB_P/PLLx_CLKFB_N	PLL external feedback clock input

Notes:

1. The global clock pins of BANK0/2 do not require an SRB and can be directly routed through a dedicated clock network to the PLL input clock port;

2. The PLL reference clock input pin needs to be connected to the global clock network via an SRB.

2.2 GLOBAL CLOCK

The Compa family products provide 8 GLOBAL CLOCKs. All GLOBAL CLOCKs support the dynamic enable function, among which two GLOBAL CLOCKs provide the function of dynamically switching input clocks. The GLOBAL CLOCK signal connection diagram is shown in Figure 2-1:

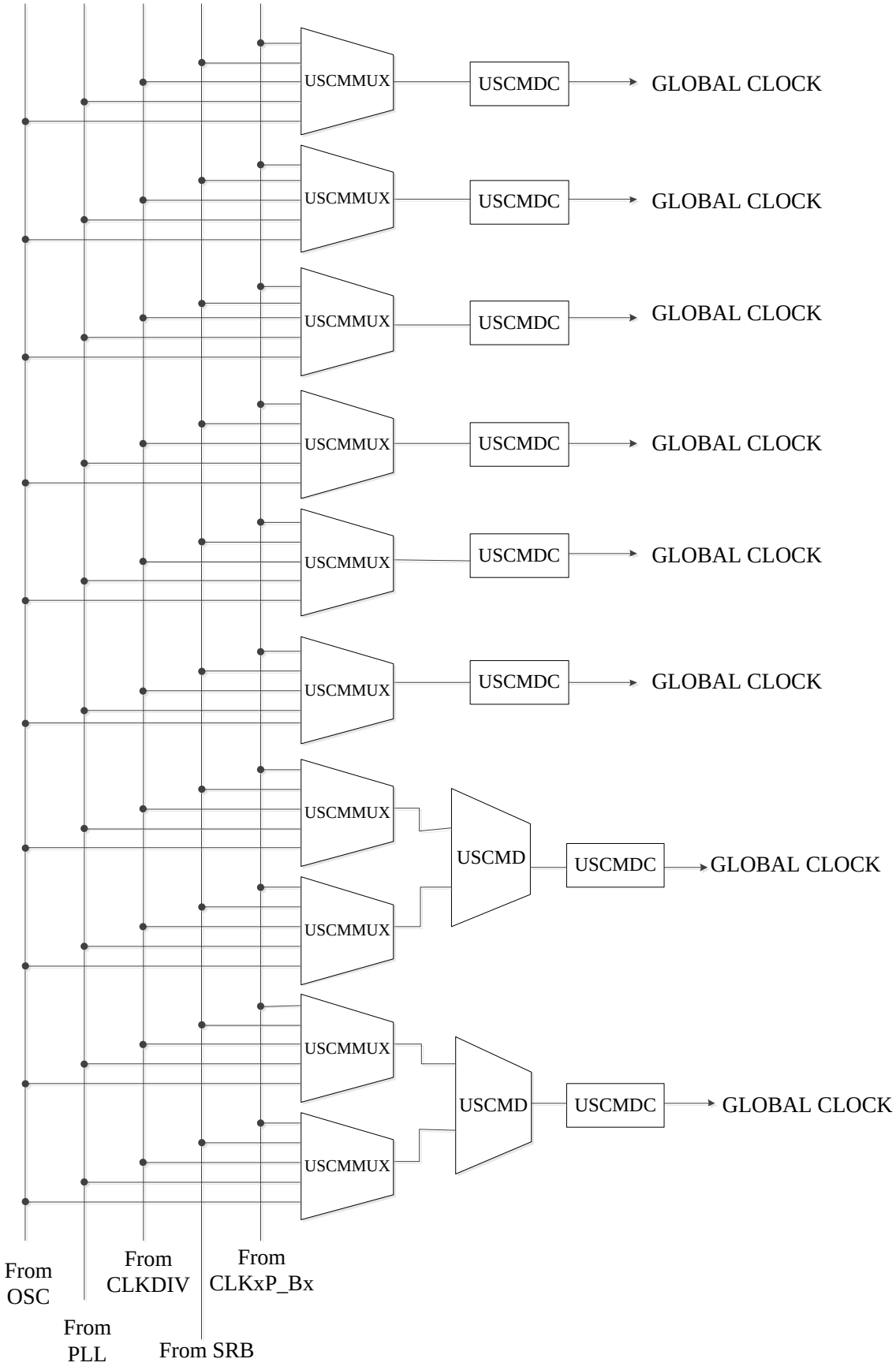

Figure 2-1 GLOBAL CLOCK Signal Connection Diagram

The signal connection diagram shows the clock source, the 28:1 multiplexer USCMMUX, the intelligent 2:1 multiplexer USCMD, and the buffer USCMDC with dynamic enable function. The GLOBAL CLOCK input source is delivered by vertical clock lines to the USCMMUX input at the middle of the chip. The GLOBAL CLOCK is evenly distributed to each column of logic cells via the global clock routing.

The description of GLOBAL CLOCK input sources is shown in the following table:

Table 2-2 GLOBAL CLOCK Input Sources

GLOBAL CLOCK Input Sources	**Description**
From CLKxP_Bx	The clock may come from global clock input pins, with up to 8 pairs of differential pins; and the single-ended clocks use the P-side; the pin name definitions can be found in the packaging manual; each pin can be connected to any USCMMUX.
From PLL	The clock may come from the PLL's output clocks CLKOUT0, CLKOUT1, CLKOUT2, CLKOUT3; each output can be connected to any USCMMUX.
From SRB	The clock may come from SRB outputs, that is, normal interconnection line outputs, with a total of 10 outputs, and each one is fixed to a USCMMUX.
From CLKDIV	The clock may come from the clock of divider outputs, CLKOUT and CLKDIVOUT, with each output connectible to any USCMMUX.
From OSC	The clock may come from the clock of the internal oscillator (OSC) output, connectible to any USCMMUX.

2.2.1 USCMMUX

USCMMUX is a 28-to-1 multiplexer that selects one clock signal from multiple clock sources as the GLOBAL CLOCK signal. Among them, the 10 signals from the SRB have a one-to-one fixed connection with the 10 USCMMUXs, while other clock sources can connect to any USCMMUX.

2.2.2 USCMDC

USCMDC is a buffer with enable control designed to meet users' requirements for dynamic control of GLOBAL CLOCK input sources without generating glitches. It is used by directly instantiating GTP_CLKBUFGCE or GTP_CLKBUFG.

➢ GTP_CLKBUFGCE

The GTP_CLKBUFGCE structure block diagram is shown in the figure below, the corresponding port descriptions are shown in Table 2-3, and the parameter descriptions are shown in Table 2-4.

Figure 2-2 GTP_CLKBUFGCE Structure Block Diagram

Table 2-3 GTP_CLKBUFGCE Port Description

Port Signal	Direection	Description
CLKIN	Input	Input Clock
CE	Input	When CE=1'b1, CLKOUT=CLKIN; When CE=1'b0, CLKOUT=0
CLKOUT	Output	Output clock

Table 2-4 GTP_CLKBUFGCE Parameter Description

Parameter	Description
DEFAULT_VALUE	For Compa family devices, the parameter can only be configured as 0; when CE=0, CLKOUT outputs 1'b0
SIM_DEVICE	Device selection parameter to choose the device as needed. The default value is "TITAN," with valid options being "TITAN," "LOGOS," "COMPACT," "LOGOS2," "TITAN2," and "TITAN3"

Taking Verilog instantiation as an example, the call method for GTP_CLKBUFGCE is as follows:

```
GTP_CLKBUFGCE
#(
.DEFAULT_VALUE      (1'b0       )
) I_GTP_CLKBUFGCE (
.CLKIN              (CLKIN      ),
.CE                 (CE         ),
.CLKOUT             (CLKOUT     )
);
```

When CE is high, CLKOUT=CLKIN; when CE is low, CLKOUT output is low level, with the timing diagram shown in the figure below:

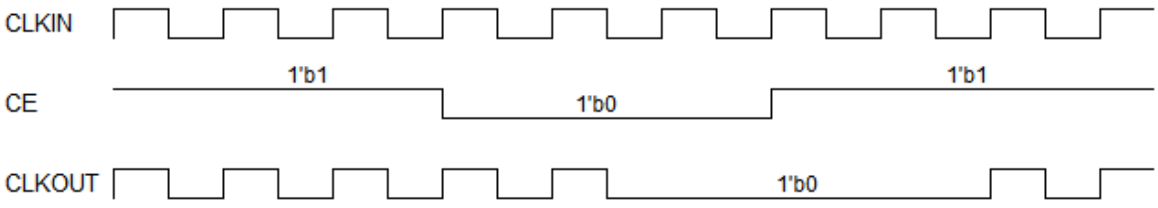

Figure 2-3 GTP_CLKBUFGCE Timing Diagram

➢ GTP_CLKBUFG

The GTP_CLKBUFG structure block diagram is shown in the figure below, and the port descriptions are shown in Table 2-5.

Figure 2-4 GTP_CLKBUFG Structure Block Diagram

Table 2-5 GTP_CLKBUFG Port Description

Port Signal	**Direction**	**Description**
CLKIN	Input	Input Clock
CLKOUT	Output	Output clock

Taking Verilog instantiation as an example, the call method for GTP_CLKBUFG is as follows:

```
GTP_CLKBUFG    I_ GTP_CLKBUFG (
    .CLKOUT          (CLKOUT    ),
    .CLKIN           (CLKIN     )
);
```

The timing diagram of GTP_CLKBUFG is shown in the figure below:

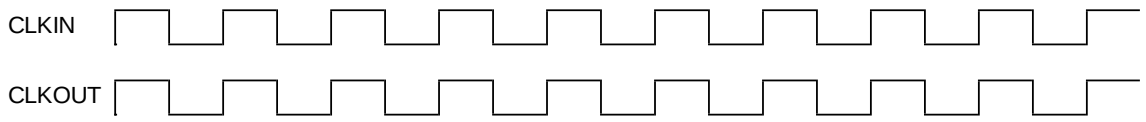

Figure 2-5 GTP_CLKBUFG Timing Diagram

2.2.3 USCMD

USCMD is an intelligent 2-to-1 clock signal multiplexer, where the control selection signal can be triggered at any time without generating glitches. When making clock selections, it is necessary to ensure that both clock inputs are functioning normally. USCMD can be used by instantiating GTP_CLKBUFGMUX.

➢ GTP_CLKBUFGMUX

GTP_CLKBUFGMUX can be used for dynamic switching between two global clock input sources; Compa products only support the "NEGEDGE" mode, and the glitchless switching is triggered by the falling edge of the clock (corresponding to TRIGGER_MODE="NEGEDGE"). It is important to note that both clock sources must be active. Otherwise, an abnormal CLKOUT output will occur during switching. The structure block diagram is shown in Figure 2-6:

Figure 2-6 GTP_CLKBUFGMUX Structure Block Diagram

Table 2-6 GTP_CLKBUFGMUX Port Description

Port Signal	Direction	Description
CLKIN0	Input	Input clock 0
CLKIN1	Input	Input clock 1
SEL	Input	The clock selection signal, which selects CLKIN0 when set to 0 and CLKIN1 when 1
CLKOUT	Output	Output clock

Table 2-7 GTP_CLKBUFGMUX Parameter Description

Parameter	Description
TRIGGER_MODE	Valid value 'NEGEDGE', mode selection; in this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched with the glitchless function triggered on the falling edge of the clock
SIM_DEVICE	Device selection parameter to choose the device as needed. The default value is "TITAN," with valid options being "TITAN," "LOGOS," "COMPACT," "LOGOS2," "TITAN2," and "TITAN3"

Taking Verilog instantiation as an example, the call method for GTP_CLKBUFGMUX is as follows:

```
GTP_CLKBUFGMUX
#(
.TRIGGER_MODE   ("NEGEDGE"    )
.SIM_DEVICE     ("COMPACT"    )
) I_CLKBUFGMUX (
    .CLKIN0             (CLKIN0         ),
    .CLKIN1             (CLKIN1         ),
    .SEL                (SEL            ),
    .CLKOUT         (CLKOUT         )
);
```

The timing diagram for GTP_CLKBUFGMUX is shown below. In TRIGGER_MODE='NEGEDGE' mode, when switching clocks, the output clock remains unchanged after two falling edges of the current clock, and then a active clock is output after two falling edges of the switched clock.

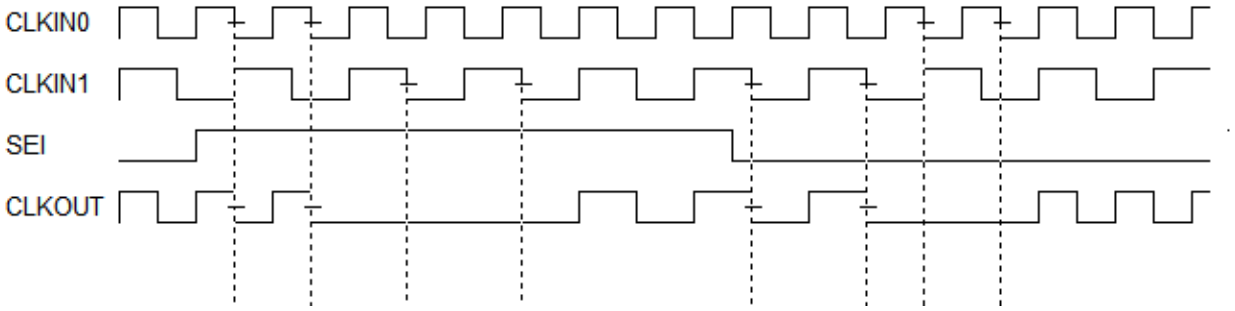

Figure 2-7 GTP_CLKBUFGMUX Timing Diagram

2.3 IO CLOCK

The IO clock network provides high-speed and low-skew clocks to IO logic resources. The IO clock network contains 4 IO CLOCKs, with 2 on each side of the chip; each side's IO CLOCK can drive nearby IO logic resources, while the IOCKBRG can also drive opposing IO logic resources.

Each IO CLOCK source outputs a clock through a multiplexer, after passing through the buffer IOCKGATE with dynamic enable function, it can drive IO logic resources, or enter the clock divider CLKDIV for frequency division as an input source for GLOBAL CLOCK, the connection diagram for IO CLOCK signals is shown in Figure 2-8:

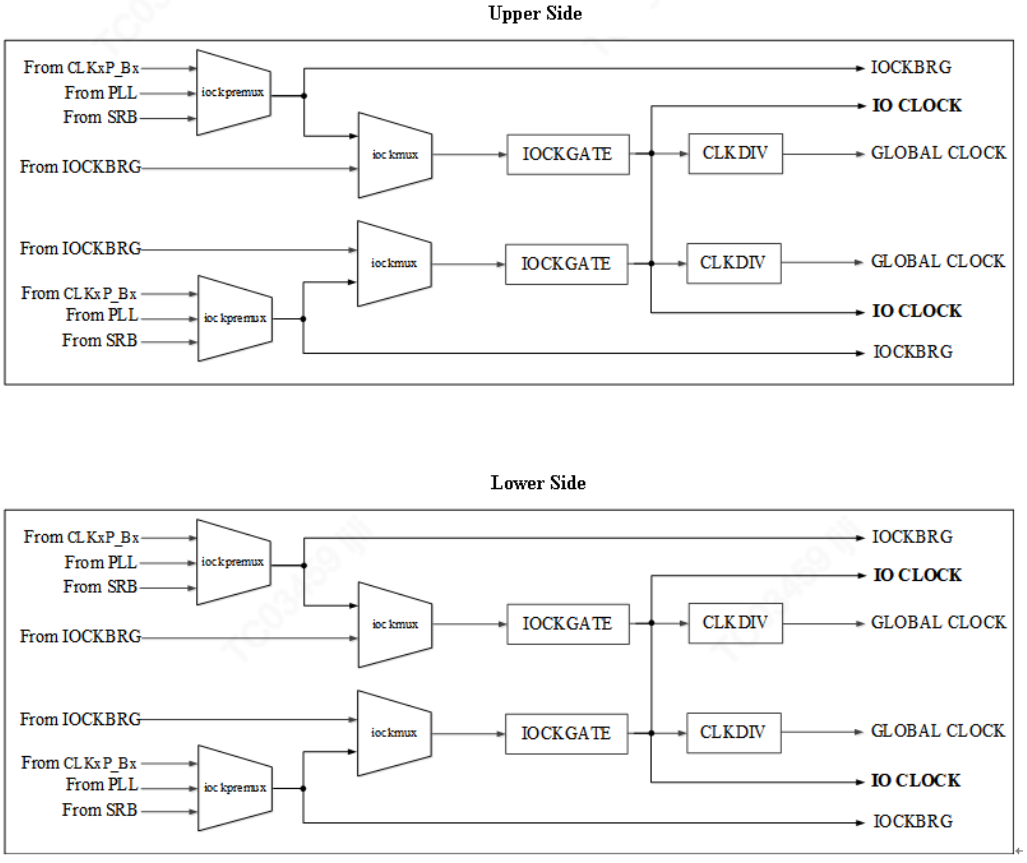

Figure 2-8 IO CLOCK Signal Connection Diagram

Table 2-8 IO CLOCK Input Sources

IO CLOCK Input Source	Description
From CLKxP_Bx	May come from the global clock input pins Upper-side IO CLOCK source: CLK0P_B0, CLK1P_B0, and CLK0P_B1 Lower-side IO CLOCK source: CLK0P_B2, CLK1P_B2, CLK0P_B3, CLK0P_B4, and CLK0P_B5
From PLL	May come from the PLL's output clocks CLKOUT0 and CLKOUT1 The IO CLOCK source of PGC1K/2K: PLL0 output clocks CLKOUT0 and CLKOUT1 The IO CLOCK source of PGC4K/7K/10K: PLL0 output clocks CLKOUT0 and CLKOUT1 and PLL1 output clocks CLKOUT0 and CLKOUT1
From SRB	May come from SRB output, with 4 signals each fixed to an iockpremux

2.3.1 IOCKGATE

In source-synchronous data transmission applications, to maintain synchronisation with the clock from the IO CLOCK, an IOCKGATE is added, providing the dynamic enable function to turn off or turn on the clock signal.

➢ GTP_IOCLKBUF

The use of IOCKGATE is implemented by instantiating GTP_IOCLKBUF; its structure block diagram is shown in Figure 2-9, the port descriptions are shown in Table 2-9, and parameters are listed in Table 2-10.

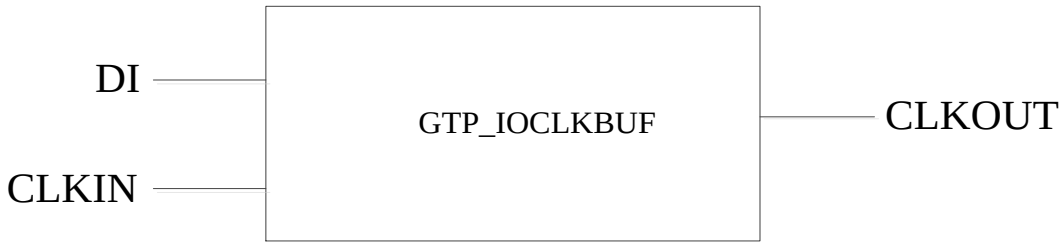

Figure 2-9 GTP_IOCLKBUF Structure Block Diagram

Table 2-9 GTP_IOCLKBUF Port Description

Port Signal	Direction	Description
CLKIN	Input	Input Clock
DI	Input	Enable signal. When DI is active, 0 denotes clock output disabled, and 1 denotes clock output enabled
CLKOUT	Output	Output clock

Table 2-10 GTP_IOCLKBUF Parameter Description

Parameter	Description
GATE_EN	When "TRUE", the enable signal DI is active; when "FALSE", the enable signal DI is inactive

Taking Verilog instantiation as an example, the call method for GTP_IOCLKBUF is as follows:

```
GTP_IOCLKBUF
#(
    .GATE_EN    ("FALSE"    )     //FALSE; TRUE
) I_ GTP_IOCLKBUF (
.CLKOUT     (CLKOUT ),
.CLKIN      (CLKIN     ),
.DI         (DI        )
);
```

When the parameter GATE_EN is "TRUE" or "FALSE", the corresponding timing diagram is as follows:

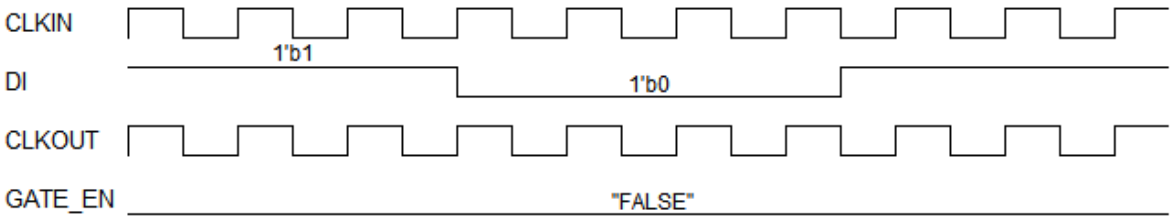

Figure 2-10 GTP_IOCLKBUF with GATE_EN="FALSE" Timing Diagram

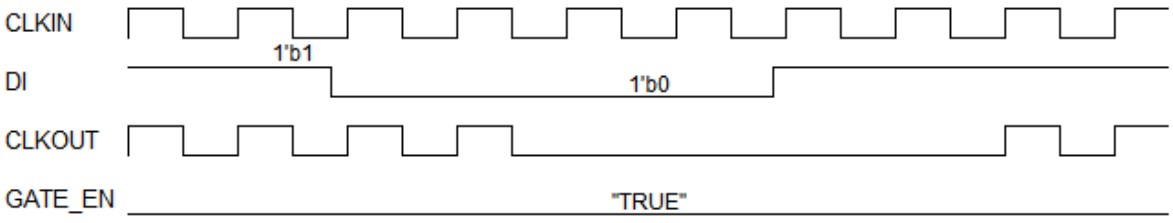

Figure 2-11 GTP_IOCLKBUF with GATE_EN="TRUE" Timing Diagram

2.3.2 CLKDIV

The divider CLKDIV divides the clock received from IOCKGATE by 2, 3.5, or 4. The divider has two output clocks: the undivided output clock CLKOUT and the divided output clock CLKDIVOUT.

- GTP_IOCLKDIV_E1

CLKDIV can be used by directly instantiating GTP_IOCLKDIV_E1. The GTP_IOCLKDIV_E1

structure block diagram is shown in the figure below, the port descriptions are shown in Table 2-11, and the parameter descriptions are shown in Table 2-12.

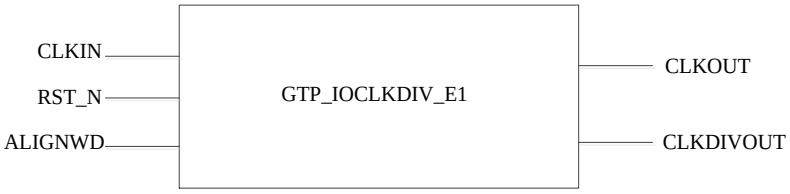

Figure 2-12 GTP_IOCLKDIV_E1 Structure Block Diagram

Table 2-11 GTP_IOCLKDIV_E1 Port Description

Port Signal	Direction	Description
CLKIN	Input	Input Clock
ALIGNWD	Input	Provides the level hold function to the output division clock; in divide-by-2 or divide-by-4 modes, it is triggered by the rising edge of the input clock, during even-numbered ALIGNWD pulses, the division clock is held for one input clock cycle upon the fourth rising edge of the input clock. In the divide-by-3.5 mode, the division clock is maintained for one input clock cycle when the fourth rising edge of the input clock occurs in each ALIGNWD pulse.
RST_N	Input	Reset signal, active low
CLKDIVOUT	Output	Divided output clock
CLKOUT	Output	Output clock without division

Table 2-12 GTP_IOCLKDIV_E1 Parameter Description

Parameter	Description
DIV_FACTOR	When set to "DIV_DIS", CLKOUT=1'b1, and CLKDIVOUT=1'b1; when set to "2," "3.5," or "4," CLKOUT is CLKIN and CLKDIVOUT outputs the division clock
GRS_EN	Global enable signal. "TRUE" indicates the global enable signal is active; "FALSE" indicates the global enable signal is inactive.

Taking Verilog instantiation as an example, the call method for GTP_IOCLKDIV_E1 is as follows:

```
GTP_IOCLKDIV_E1 #(
.DIV_FACTOR          ("DIV_DIS"      ),     //"DIV_DIS";"2"; "3.5"; "4";
.GRS_EN              ("TRUE"         )      //"TRUE"; "FALSE"
)I_IOCLKDIV_E1(
.CLKIN          (CLKIN          ),
.RST_N          (RST_N          ),
.ALIGNWD        (ALIGNWD        ),
.CLKOUT             (CLKOUT         ),
.CLKDIVOUT          (CLKDIVOUT      )
);
```

When DIV_FACTOR is "2" or "3.5", which means divide-by-2 or divide-by-3.5, the timing diagram for the clock output from GTP_IOCLKDIV_E1 is as follows:

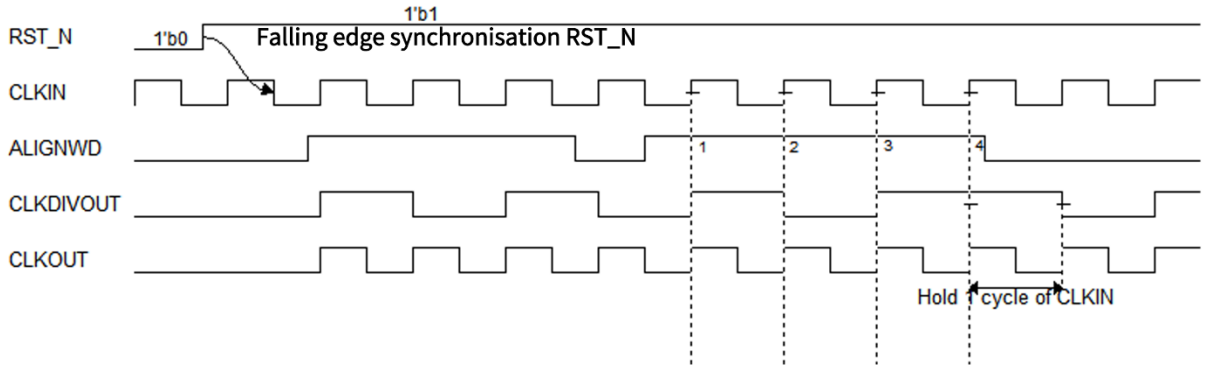

Figure 2-13 GTP_IOCLKDIV_E1 Divide-by-2 Timing Diagram

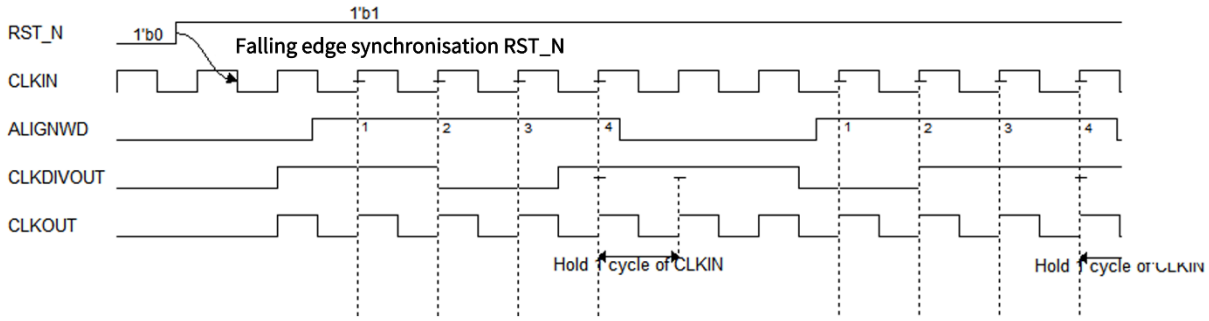

Figure 2-14 GTP_IOCLKDIV_E1 Divide-by-3.5 Timing Diagram

2.3.3 IOCKBRG

The IO CLOCKs on the upper and lower sides of the chip drive their respective sides' IO logic resources. To drive the IO logic resources on the opposite side, a bridging function is needed. The Compa family products include such IO CLOCK bridging resources, IOCKBRG, where the upper-side IO CLOCK can bridge to the lower side of the chip via IOCKBRG to drive the IO logic resources there, and the lower-side IO CLOCK can bridge to the upper side of the chip via IOCKBRG to drive the IO logic resources.

➢ GTP_IOCLKMUX

Users can bridge the IO CLOCK by instantiating GTP_IOCLKMUX, the structure block diagram of GTP_IOCLKMUX is shown below, and its port descriptions are shown in Table 2-13.

Figure 2-15 GTP_IOCLKMUX Block Diagram

Table 2-13 GTP_IOCLKMUX Port Description

Port Signal	**Direction**	**Description**
CLKIN0	Input	Input clock 0
CLKIN1	Input	Input clock 1
SEL	Input	Clock select signal. Select CLKIN0 when it is 1'b0; select CLKIN1 when it is 1'b1;
CLKOUT	Output	Output clock

Taking Verilog instantiation as an example, the call method for GTP_IOCLKMUX is as follows:

```
GTP_IOCLKMUX
I_ IOCLKMUX       (
    .CLKIN0             (CLKIN0         ),
    .CLKIN1             (CLKIN1         ),
    .SEL                (SEL            ),
    .CLKOUT         (CLKOUT         )
    );
```

The timing diagram of GTP_IOCLKMUX is shown below.

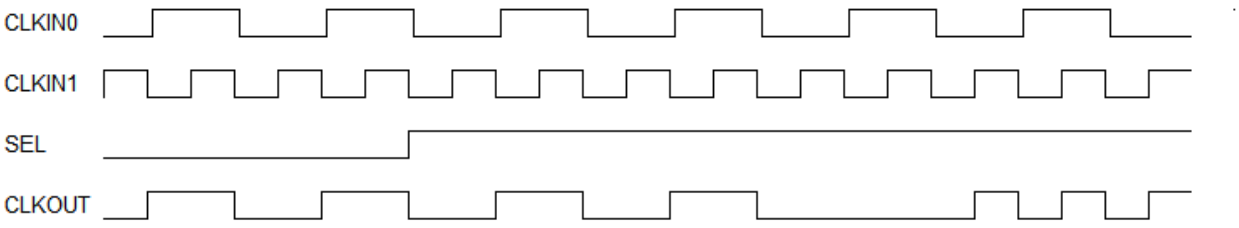

Figure 2-16 GTP_IOCLKMUX Timing Diagram

2.4 CLKDLY

To meet the need to adjust the input clock phase in some applications, the global clock input pins of the Compa family products offer an optional time delay function. The time delay of the input clock

is implemented by directly calling GTP_IOCLKDELAY.

➢ GTP_IOCLKDELAY

The GTP_IOCLKDELAY structure block diagram is shown in Figure 2-17, the port descriptions are shown in Table 2-14, and the parameter descriptions are shown in Table 2-15.

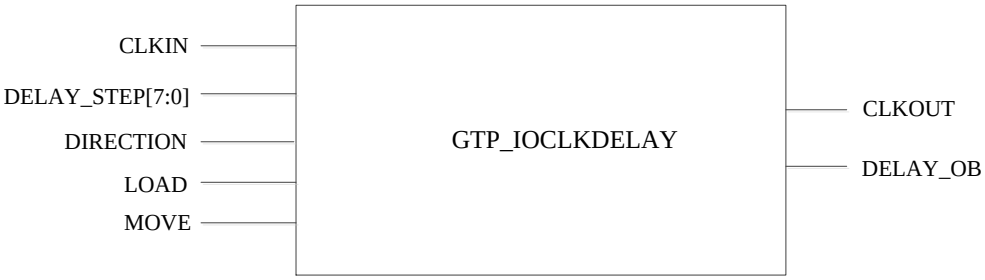

Figure 2-17 GTP_IOCLKDELAY Diagram

Table 2-14 GTP_IOCLKDELAY Port Description

Port Signal	**Direction**	**Description**
CLKIN	Input	Clock signal from global clock input pins
DELAY_STEP [7:0]	Input	Delay step from DLL
DIRECTION	Input	Set to 0 to dynamically increase the delay step; set to 1 to dynamically decrease the delay step.
LOAD	Input	When LOAD=1'b1, the static parameter configuration or the delay step value from DLL is loaded. When LOAD=1'b0, the delay time is dynamically adjusted.
MOVE	Input	The falling edge triggers dynamic fine adjustment, increasing or decreasing one step depending on the DIRECTION
CLKOUT	Output	Delayed clock output
DELAY_OB	Output	Dynamic fine adjustment overflow flag of delay step; it goes high when internal DELAY STEP is 127 with DIRECTION set to 0; it goes high when internal delay step is 0 with DIRECTION set to 1

Table 2-15 GTP_IOCLKDELAY Parameter Description

Parameter	**Description**
DELAY_STEP_VALUE	Static delay step, effective when DELAY_STEP_SEL is set to "PARAMETER"
DELAY_STEP_SEL	When set to"PORT," it selects the delay step from DLL; When set to"PARAMETER," it selects the delay step from the static parameter configuration
SIM_DEVICE	Device selection parameter to choose the device as needed. The default value is "TITAN," with valid options being "TITAN," "LOGOS," and "COMPACT"

Users can statically configure the delay step to adjust the number of delay chains, with each step delaying by 25ps; the minimum delay chain count is 0, and the maximum is 127 (8'b0–8'b0111_1111), or dynamically obtain the delay step using the on-chip DLL or dynamically fine adjust the delay step. In static configuration adjustment mode, MOVE and DIRECTION are not working.

Taking Verilog instantiation as an example, the call method for GTP_IOCLKDELAY is as follows:

```
GTP_IOCLKDELAY
#(
.DELAY_STEP_VALUE     (8'd10          ),  //Used for static DELAY STEP setting, 0~127
.DELAY_STEP_SEL       ("PARAMETER")   // "PARAMETER" or "PORT"
)
I_IOCLKDELAY (
.CLKIN                (CLKIN          ),
.DELAY_STEP           (DELAY_STEP     ),
.CLKOUT               (CLKOUT         ),
.DIRECTION            (DIRECTION      ),
.LOAD                 (LOAD           ),
.MOVE                 (MOVE           ),
.DELAY_OB             (DELAY_OB       )
);
```

In the above example, the DELAY_STEP_VALUE parameter is set to 10, LOAD is set to 1'b1, DIRECTION and MOVE are set to 1'bx, and the timing diagram is as follows:

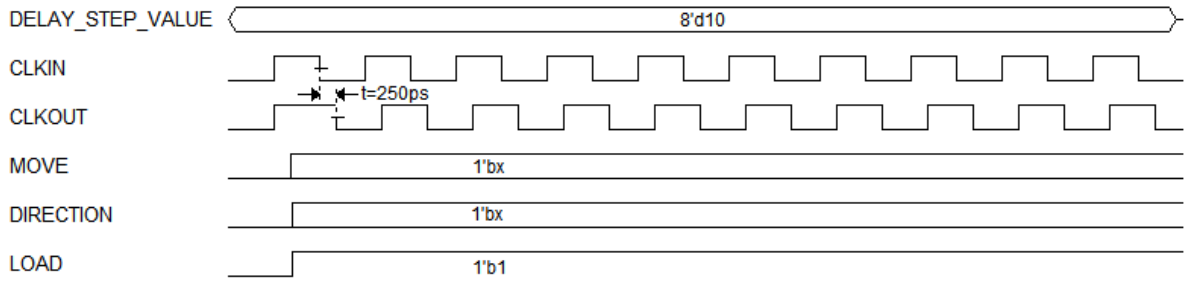

Figure 2-18 Static Configuration of GTP_IOCLKDELAY Timing Diagram

When adjusting in dynamic mode, LOAD=1'b0, MOVE acts as the trigger clock for the dynamic mode by triggered on the falling edge. With each trigger, the phase relationship between CLKOUT and CLKIN increases or decreases by one step. DIRECTION controls the increase or decrease of the step, decreasing the step when DIRECTION=1'b1; and increasing the step when DIRECTION=1'b0. The corresponding timing diagram is as follows, with each increase or decrease in time being T1.

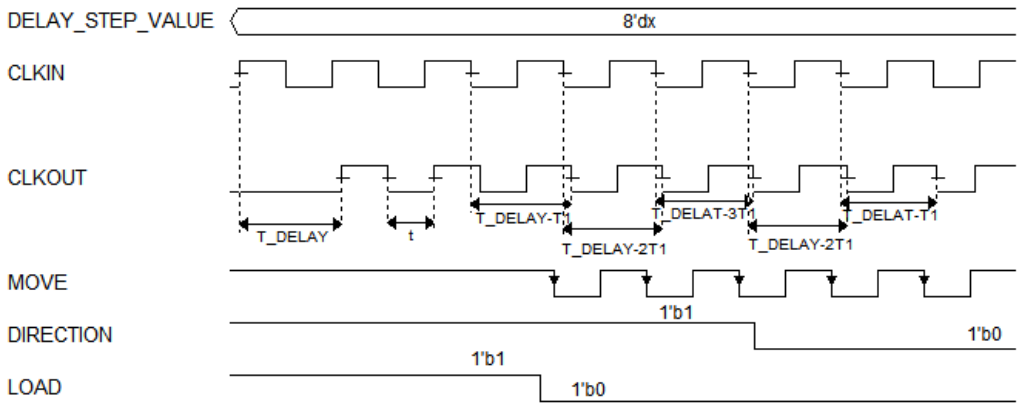

Figure 2-19 Dynamic Delay Example of GTP_IOCLKDELAY Timing Diagram

For DELAY_OB, as described in the diagram below, after the moment t0, DIRECTION=1'b0; if the count M of MOVE falling edges plus the value of DELAY_STEP_VALUE set or the DELAY_STEP value x from DLL reaches 127, then DELAY_OB transitions to a high level, indicating that the maximum adjustable DELAY TIME has been reached and no further steps can be added; when DELAY_STEP_VALUE or DELAY_STEP is set to 8'd0, if DIRECTION=1'b1, then DELAY_OB transitions to a high level, indicating that the minimum adjustable DELAY TIME has been reached and no further steps can be reduced.

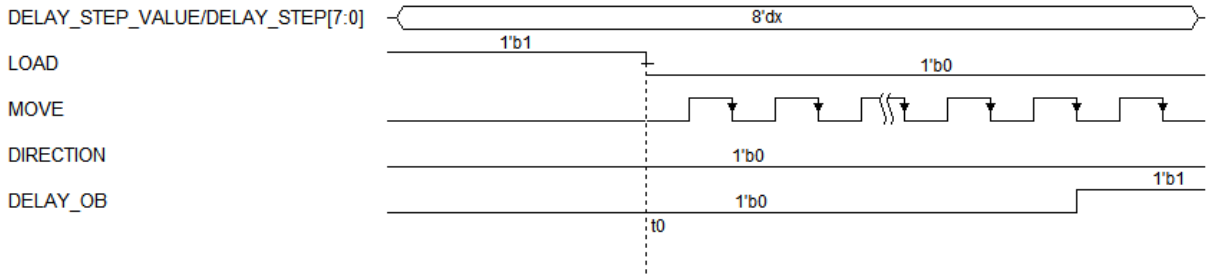

Figure 2-20 DELAY_OB Transitioning to High Level with Maximum Delay Timing Diagram

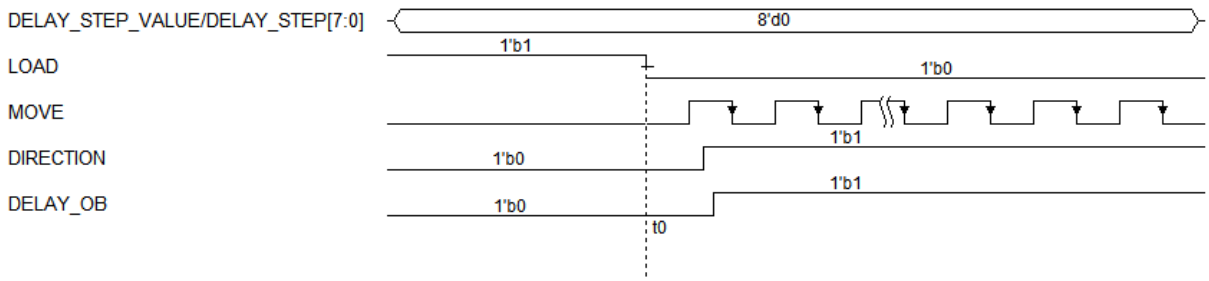

Figure 2-21 DELAY_OB Transitioning to High Level with Minimum Delay Timing Diagram

2.5 GLOBAL SIGNAL

Compa family products provide 8 GLOBAL SIGNALs, each of which can act both as a global reset signal and a global clock signal evenly distributed throughout the chip. The GLOBAL SIGNAL connection diagram is shown in Figure 2-22:

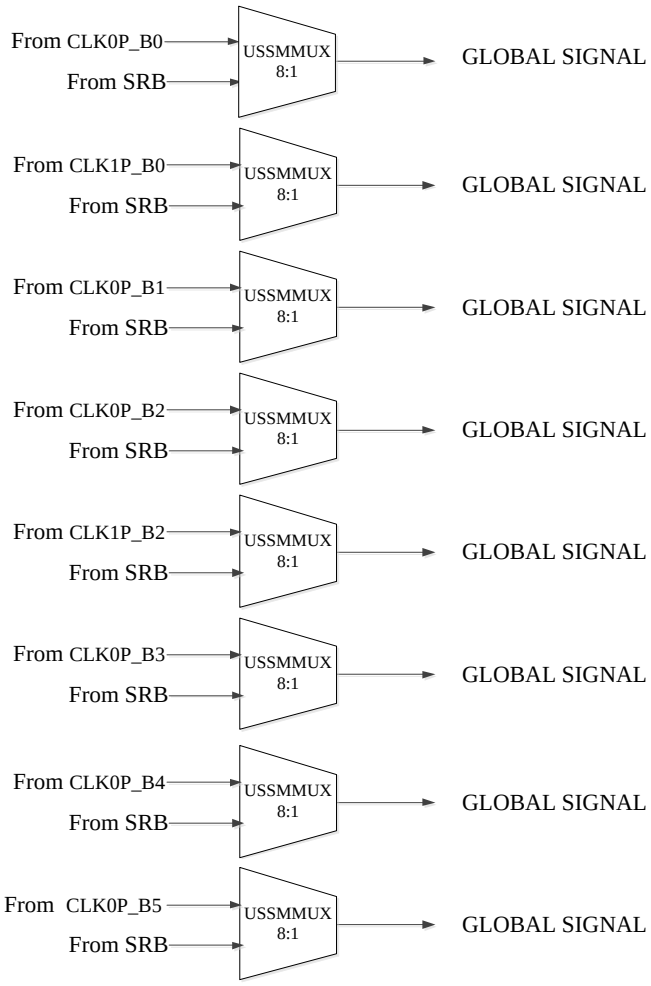

Figure 2-22 GLOBAL SIGNAL Connection Diagram

The signal sources for GLOBAL SIGNAL come from 8 global clock input pins and 7 internal SRB output signals of the chip. Each global clock input pin is fixed to a USSMMUX, and the output of an SRB can be connected to any USSMMUX.

➢ GTP_BUFGS

By instantiating GTP_BUFGS, signals can be fed into USSMMUX and reach the driven logic modules evenly. The GTP_BUFGS structure block diagram is shown in the figure below, and the port descriptions are shown in Table 2-16:

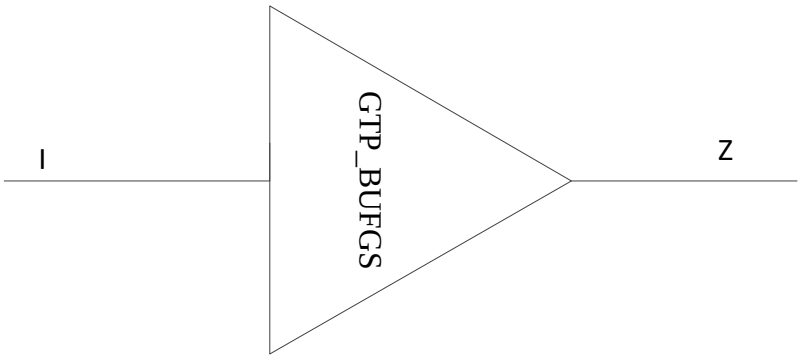

Figure 2-23 GTP_BUFGS Block Diagram

Table 2-16 GTP_BUFGS Port Description

Port Signal	Direction	Description
I	Input	Global signal input port
Z	Output	Global signal output port

Taking Verilog instantiation as an example, the call method for GTP_BUFGS is as follows:

```
GTP_BUFGS BUFGS_inst (
    .I      (  I  ),
    .Z      (  Z  )
);
```

2.6 Phase Locked Loop (PLL)

2.6.1 PLL Function Overview

The PLL of the Compa family products offers functions like frequency synthesis, phase adjustment, clock skew reduction, and power consumption reduction. The system block diagram of PLL is shown in Figure 2-24:

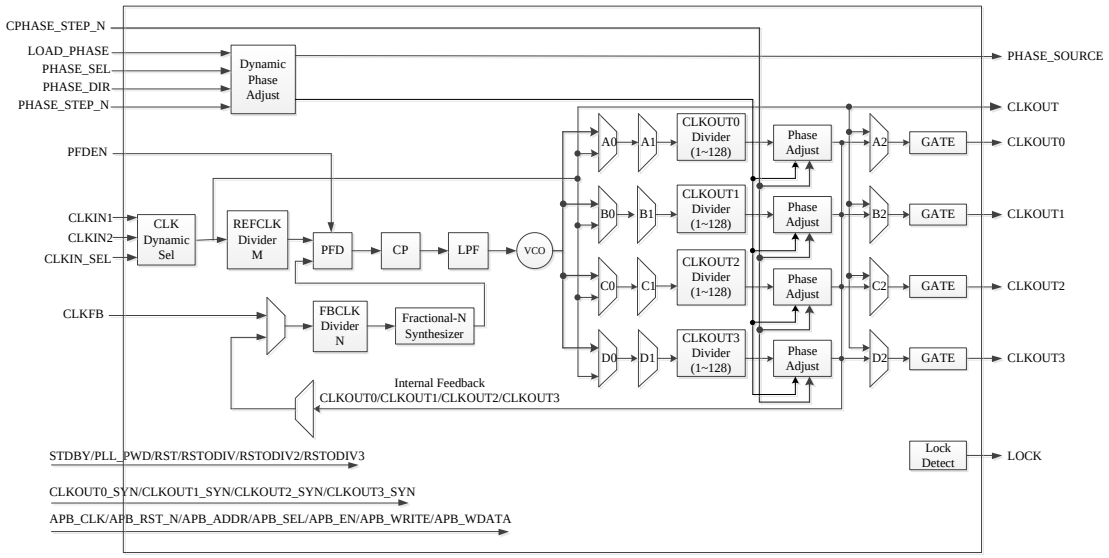

Figure 2-24 PLL Schematic Block Diagram

The key features of PLL are:

- Dynamic switching of input reference clock
- Two feedback modes: internal feedback and external feedback
- Fractional division function
- Dynamic enable of output clock
- Static and dynamic phase adjustment
- PLL dynamic configuration
- Mutual cascading of output clocks

2.6.2 GTP_PLL_E2

Users can generate PLL function modules through IPC when using PLL or directly instantiate GTP_PLL_E2. The GTP_PLL_E2 structure block diagram is shown in the figure below, the port descriptions are shown in Table 2-17, and the parameter descriptions are shown in Table 2-18 GTP_PLL_E2.

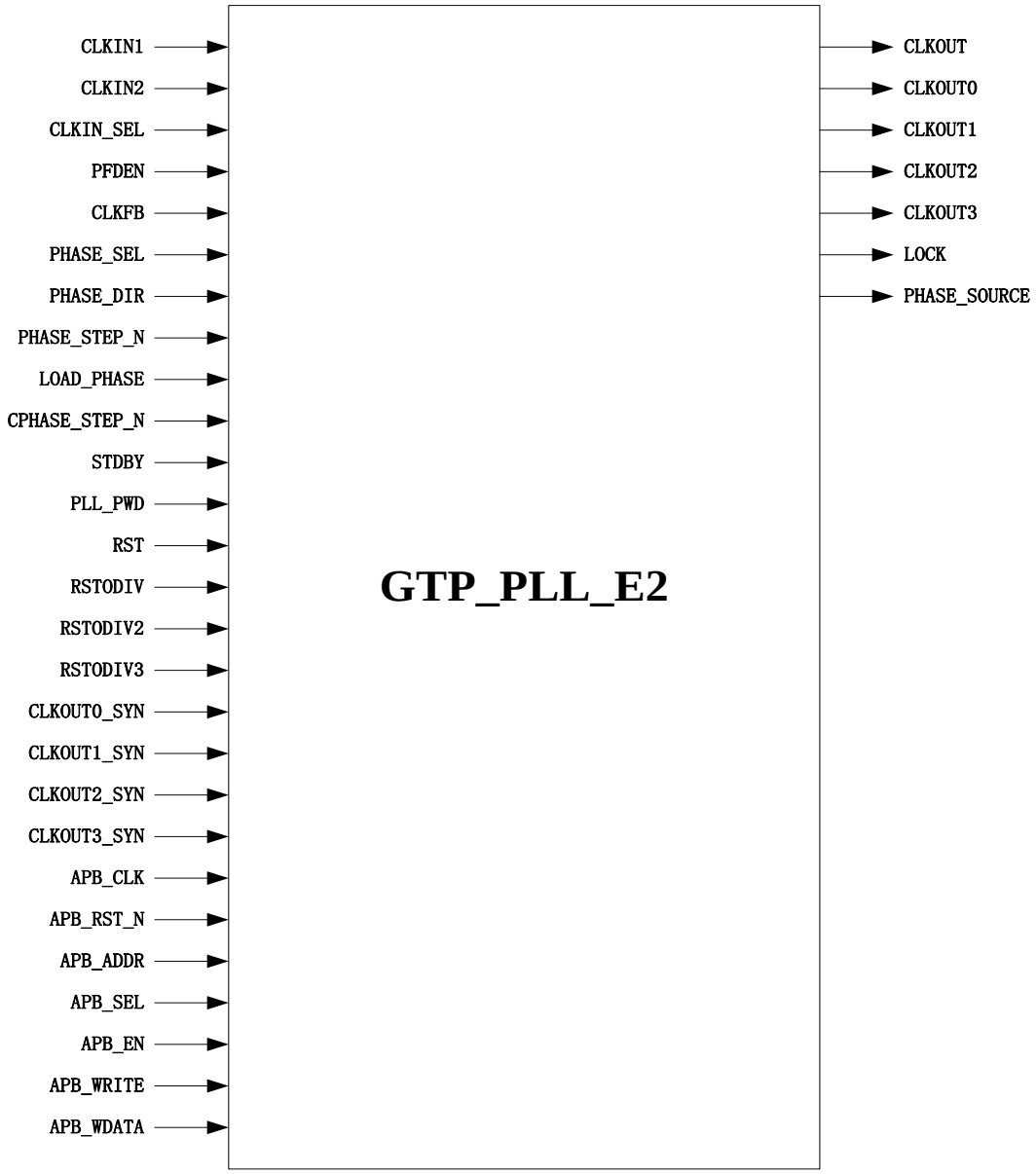

Figure 2-25 GTP_PLL_E2 Top-Level Ports

Table 2-17 GTP_PLL_E2 Port Description

Port Signal	Direction	Function Description
CLKOUT	Output	PLL reference clock output; reference clock enters the PLL and is directly bypassed output (Bypass PLL) without going through the input clock divider, PFD, CP, LPF, VCO, and output divider
CLKOUT0	Output	The first output clock of the PLL, with phase adjustment function
CLKOUT1	Output	The second output clock of the PLL, with phase adjustment function
CLKOUT2	Output	The third output clock of the PLL, with phase adjustment function
CLKOUT3	Output	The fourth output clock of the PLL, with phase adjustment function
PHASE_SOURCE	Output	Indication signal for the source of PLL dynamic phase adjustment control signal 1'b0: Indicates that the control signal comes from the APB port 1'b1: Indicates that the control signal comes from ports, i.e. CPHASE_STEP_N, LOAD_PHASE, PHASE_SEL, PHASE_DIR, and PHASE_STEP_N. If the user didn't choose a dynamic port, the register with

Port Signal	Direction	Function Description
		the APB port will be used by default for dynamic phase adjustment settings
LOCK	Output	An asynchronous PLL frequency lock indication signal; when the signal is pulled high, it indicates that the PLL feedback clock signal is locked to the input clock signal; When the clock recovers from a lost or unstable state, PLL needs to be reset via the reset pin RST
CLKIN1	Input	PLL reference input clock 1
CLKIN2	Input	PLL reference input clock 2
CLKFB	Input	PLL feedback clock input
CLKIN_SEL	Input	The input clock selection signal, which selects either of the input reference clocks CLKIN1 and CLKIN2 as the input clock for the input divider; selects CLKIN1 when it is 1'b0 and selects CLKIN2 when it is 1'b1
PFDEN	Input	PFD enable signal for the PLL; 1'b0 indicates that the PFD is disabled, and 1'b1 indicates that the PFD is enabled; PFDEN is an optional signal, and the user can decide whether PFDEN is effective through the static configuration parameter PFDEN_EN. Note that after PFD is turned off, the LOCK signal still maintains a high level for a period of time before pulling down, during which there will still be clock output, but the clock will be unstable
PHASE_SEL	Input	Select any PLL output clock for phase adjustment 2'b00: Selects CLKOUT0, 2'b01: Selects CLKOUT3, 2'b10: Selects CLKOUT2, 2'b11: Selects CLKOUT1;
PHASE_DIR	Input	Select the direction for dynamic phase fine adjustment; 1'b0: lag, 1'b1: lead
PHASE_STEP_N	Input	Dynamic phase fine adjustment trigger signal; with each trigger, the output clock phase is adjusted by 1/8 T_{vco} (where T_{vco} represents the clock cycle of the input VCO)
LOAD_PHASE	Input	Load signal for the current phase fine adjustment value of the selected channel is a pulse signal, active high
CPHASE_STEP_N	Input	Dynamic phase coarse adjustment trigger signal; each trigger increments the counter by +1, adjusting the output clock phase by n*T_{vco}, where n*T_{vco} is set through phase coarse static configuration
CLKOUT0_SYN	Input	The CLKOUT0 output clock enable control signal; active high. The signal is active when the user sets CLKOUT0_SYN_EN to "TRUE." If the user sets the CLKOUT0 output as active, or if there is no requirement for the signal CLKOUT0_SYN, the CLKOUT0 output clock is always active unless the PLL is in Standby mode.
CLKOUT1_SYN	Input	The CLKOUT1 clock output enable control signal; active high; its function is the same as CLKOUT0_SYN
CLKOUT2_SYN	Input	The CLKOUT2 clock output enable control signal; active high; its function is the same as CLKOUT0_SYN
CLKOUT3_SYN	Input	The CLKOUT3 clock output enable control signal; active high; its function is the same as CLKOUT0_SYN
STDBY	Input	Standby mode control signal; active high; turns off all PLL modules; the STDBY signal can be controlled via user logic or the Power Controller module. The STDBY signal is optional and is controlled by the configuration bit STDBY_EN. It is active when set to "TRUE" and inactive when set to "FALSE"
PLL_PWD	Input	The PLL Power Down signal; active high; disable modules except for the LDO
RST	Input	The PLL reset signal, active high; this signal resets the VCO, PFD, CP, LPF, and all clock dividers, including input dividers and output dividers. The reset signal will pull down the PLL output directly to ground. After the reset is released, the PLL starts to enter the lock state, and the PLL frequency lock

Port Signal	Direction	Function Description
		is completed after t_{LOCK} (PLL lock time)
RSTODIV	Input	The PLL reset signal, active high; this signal resets the VCO, PFD, CP, LPF and all dividers except the input divider RSTODIV cannot reset the input divider (M-divider), as there may be synchronization requirements between the external clock and the reference clock. In this case, a phase relationship between the external clock and the output clock of the M-divider needs to be maintained, even during the reset of the PLL circuit. After the reset is released, the PLL starts to enter the lock state, and the PLL frequency lock is completed after t_{LOCK} (PLL lock time)
RSTODIV2	Input	RSTODIV2 only resets the CLKOUT2 output divider; the signal can be generated by internal fabric logic or input via IO pins. Using this reset signal will pull down the CLKOUT2 output to ground, unless the PLL is in the bypass mode This signal is active-high and is option. If the CLKOUT2 output is used in the PLL feedback path, it is recommended to use the RST/RSTODIV signal to reset the PLL, rather than the RSTODIV2 reset signal
RSTODIV3	Input	RSTODIV3 only resets the CLKOUT3 output divider; the signal can be generated by internal fabric logic or input via IO pins. Using this reset signal will pull down the CLKOUT3 output to ground, unless the PLL is in the bypass mode This signal is active-high and is option. If the CLKOUT3 output is used in the PLL feedback path, it is recommended to use the RST/ RSTODIV signal to reset the PLL, rather than the RSTODIV3 reset signal
APB_CLK	Input	PLL APB port bus clock
APB_RST_N	Input	PLL APB port bus asynchronous reset signal, active low
APB_ADDR	Input	PLL APB port bus address
APB_SEL	Input	PLL APB port bus select signal to select the slave device, active high
APB_EN	Input	The PLL APB port bus enable signal, which indicates the second and subsequent cycles of transmission, active high;
APB_WRITE	Input	PLL APB port bus write enable signal; 1'b0: read operation, 1'b1: write operation
APB_WDATA	Input	PLL APB port bus data input

Table 2-18 GTP_PLL_E2 Parameter Description

Parameter Name	Valid Values	Function Description
CLKIN_FREQ	10MHz~500MHz	Input Clock Frequency
PFDEN_EN	"FALSE", "TRUE"	PFDEN signal enable configuration "FALSE": PFDEN signal input is invalid "TRUE": PFDEN signal input is active;
PFDEN_APB_EN	"FALSE", "TRUE"	PLL PFD enable signal source configuration "FALSE": from dynamic port "TRUE": from APB port
LOCK_MODE	1’b0~1’b1	PLL frequency detection mode configuration 1'b0: real-time monitoring mode 1'b1: hold mode
STATIC_RATIOI	1~50	The division ratio configuration of the input clock divider
STATIC_RATIO0	1~128	The division ratio configuration of the CLKOUT0 divider
STATIC_RATIO1	1~128	The division ratio configuration of the CLKOUT1 divider
STATIC_RATIO2	1~128	The division ratio configuration of the CLKOUT2 divider

Parameter Name	Valid Values	Function Description
STATIC_RATIO3	1~128	The division ratio configuration of the CLKOUT3 divider
STATIC_RATIOF	1~128	Feedback divider's division ratio configuration Integer divider: 1~128 Fractional divider: 7~120
FRACN_EN	"FALSE", "TRUE"	Fractional division function enable "FALSE": fractional division function disabled "TRUE": fractional division function enabled
FRACN_DIV	0~65535	Fractional division decimal configuration
PHASE_APB_EN	"FALSE", "TRUE"	Source configuration for control signal of dynamic phase adjustment "FALSE": from dynamic port "TRUE": from APB port
STATIC_PHASE0	0~7	The CLKOUT0 phase fine adjustment static configuration parameter
STATIC_PHASE1	0~7	The CLKOUT1 phase fine adjustment static configuration parameter
STATIC_PHASE2	0~7	The CLKOUT2 phase fine adjustment static configuration parameter
STATIC_PHASE3	0~7	The CLKOUT3 phase fine adjustment static configuration parameter
STATIC_CPHASE0	0~127	The CLKOUT0 phase coarse adjustment static configuration parameter
STATIC_CPHASE1	0~127	The CLKOUT1 phase coarse adjustment static configuration parameter
STATIC_CPHASE2	0~127	The CLKOUT2 phase coarse adjustment static configuration parameter
STATIC_CPHASE3	0~127	The CLKOUT3 phase coarse adjustment static configuration parameter
VCOCLK_BYPASS0	"FALSE", "TRUE"	The VCO clock bypass configuration (MUXA0 configuration bit) "FALSE": select VCO clock "TRUE": select PLL reference clock
VCOCLK_BYPASS1	"FALSE", "TRUE"	The VCO clock bypass configuration (MUXB0 configuration bit) "FALSE": select VCO clock "TRUE": select PLL reference clock
VCOCLK_BYPASS2	"FALSE", "TRUE"	The VCO clock bypass configuration (MUXC0 configuration bit) "FALSE": select VCO clock "TRUE": select PLL reference clock
VCOCLK_BYPASS3	"FALSE", "TRUE"	The VCO clock bypass configuration (MUXD0 configuration bit) "FALSE": select the VCO clock "TRUE": select PLL reference clock
ODIV0_CLKIN_SEL	0~3	MUXA1 configuration in front of the CLKOUT0 divider 0: select the output of the MUXA0 1: select the output of the CLKOUT3 divider 2: select the output of the CLKOUT1 divider 3: select the output of the CLKOUT2 divider
ODIV1_CLKIN_SEL	0~3	MUXB1 configuration in front of the CLKOUT1 divider 0: select the output of the MUXB0 1: select the output of the CLKOUT0 divider 2: select the output of the CLKOUT3 divider 3: select the output of the CLKOUT2 divider
ODIV2_CLKIN_SEL	0~3	MUXC1 configuration in front of the CLKOUT2 divider 0: select the output of the MUXC0

Parameter Name	Valid Values	Function Description
		1: select the output of the CLKOUT0 divider 2: select the output of the CLKOUT1 divider 3: select the output of the CLKOUT3 divider
ODIV3_CLKIN_SEL	0~3	MUXD1 configuration in front of the CLKOUT3 divider 0: select the output of the MUXD0 1: select the output of the CLKOUT0 divider 2: select the output of the CLKOUT1 divider 3: select the output of the CLKOUT2 divider
CLKOUT0_SEL	0~4	MUXA2 configuration behind the CLKOUT0 divider 0: select the output of the CLKOUT0 divider 1: select the output of the CLKOUT1 divider 2: select the output of the CLKOUT2 divider 3: select the output of the CLKOUT3 divider 4: select PLL reference clock
CLKOUT1_SEL	0~4	MUXB2 configuration behind the CLKOUT1 divider 0: select the output of the CLKOUT1 divider 1: select the output of the CLKOUT2 divider 2: select the output of the CLKOUT3 divider 3: select the output of the CLKOUT0 divider 4: select PLL reference clock
CLKOUT2_SEL	0~4	MUXC2 configuration behind the CLKOUT2 divider 0: select the output of the CLKOUT2 divider 1: select the output of the CLKOUT3 divider 2: select the output of the CLKOUT0 divider 3: select the output of the CLKOUT1 divider 4: select PLL reference clock
CLKOUT3_SEL	0~4	MUXD2 configuration behind the CLKOUT3 divider 0: select the output of the CLKOUT3 divider 1: select the output of the CLKOUT0 divider 2: select the output of the CLKOUT1 divider 3: select the output of the CLKOUT2 divider 4: select PLL reference clock
CLKOUT0_SYN_EN	"FALSE", "TRUE"	Configuration for CLKOUT0_SYN signal enable "FALSE": CLKOUT0_SYN input is inactive "TRUE": CLKOUT0_SYN input is active
CLKOUT1_SYN_EN	"FALSE", "TRUE"	Configuration for CLKOUT1_SYN signal enable "FALSE": CLKOUT1_SYN input is inactive "TRUE": CLKOUT1_SYN input is active
CLKOUT2_SYN_EN	"FALSE", "TRUE"	Configuration for CLKOUT2_SYN signal enable "FALSE": CLKOUT2_SYN input is inactive "TRUE": CLKOUT2_SYN input is active
CLKOUT3_SYN_EN	"FALSE", "TRUE"	Configuration for CLKOUT3_SYN signal enable "FALSE": CLKOUT3_SYN input is inactive "TRUE": CLKOUT3_SYN input is active
INTERNAL_FB	"CLKOUT0" "CLKOUT1" "CLKOUT2" "CLKOUT3" "DISABLE"	Internal feedback path select
EXTERNAL_FB	"CLKOUT0" "CLKOUT1" "CLKOUT2" "CLKOUT3" "DISABLE"	External feedback path select
BANDWIDTH	"LOW", "HIGH" "OPTIMIZED"	Bandwidth select configuration

Parameter Name	Valid Values	Function Description
STDBY_EN	"FALSE", "TRUE"	STDBY signal enable configuration "FALSE": STDBY input is inactive "TRUE": STDBY input is active
RST_INNER_EN	"FALSE", "TRUE"	Reset signal RST enable configuration "FALSE": RST input is inactive "TRUE": RST input is active
RSTODIV_EN	"FALSE", "TRUE"	Reset signal RSTODIV enable configuration "FALSE": RSTODIV input is inactive "TRUE": RSTODIV input is active
RSTODIV2_EN	"FALSE", "TRUE"	Reset signal RSTODIV2 enable configuration "FALSE": RSTODIV2 input is inactive "TRUE": RSTODIV2 input is active
RSTODIV3_EN	"FALSE", "TRUE"	Reset signal RSTODIV3 enable configuration "FALSE": RSTODIV3 input is inactive "TRUE": RSTODIV3 input is active

2.6.3 Standby Mode

When the PLL is not required to work, the STDBY signal can power down the PLL completely, entering Standby mode to reduce power consumption; the STDBY signal can be controlled by user logic or the Power Controller module. The STDBY signal is optional and is controlled by the configuration bit STDBY_EN. It is active when set to "TRUE" and inactive when set to "FALSE."

2.6.4 PLL Operation Mode

➢ PLL clock bypass mode:

Mode 1: After the input reference clock CLKIN enters the PLL, it does not pass through the input divider, phase frequency detector (PFD), charge pump (CP), loop filter (LPF), and oscillator (VCO), and output dividers; it is directly routed through a bypass structure as shown in Figure 2-26.

Mode 2: After the input reference clock CLKIN enters the PLL, it does not pass through the input divider, PFD, CP, LPF, and VCO modules, but does pass through the output divider. The divided clock signals are then output from the PLL output ports CLKOUT0/CLKOUT1/CLKOUT2 /CLKOUT3; the specific flow of clock signals in bypass mode is shown in Figure 2-26.

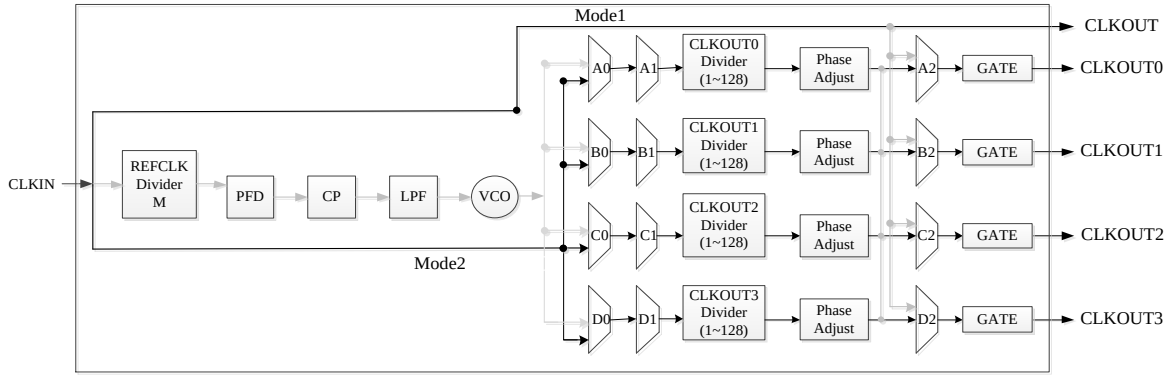

Figure 2-26 PLL Bypass Output Diagram

➢ Internal feedback mode

Internal feedback mode, where the PLL feedback divider output does not go through the clock network, and the feedback clock signal flow is directly implemented locally within the PLL. The clock from the output divider directly enters the PFD input through the feedback divider via the shortest path. This will improve the jitter feature of the PLL.

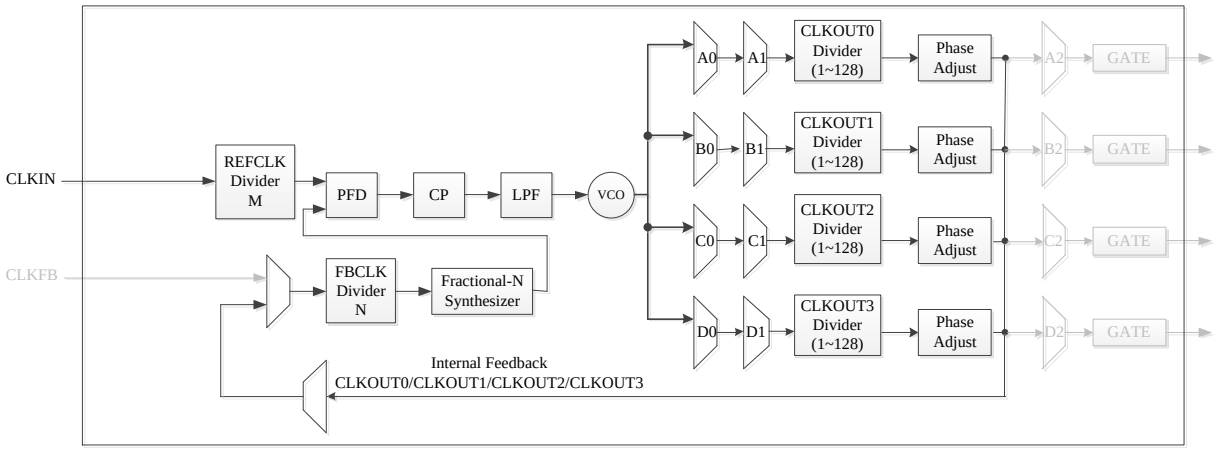

Figure 2-27 PLL Internal Feedback Diagram

➢ External feedback mode

External feedback mode, where the output clock from the PLL is fed back externally from the PLL. The phase difference between the PLL input and output is subject to the delay in the feedback path.

2.6.5 Output Frequency Programming

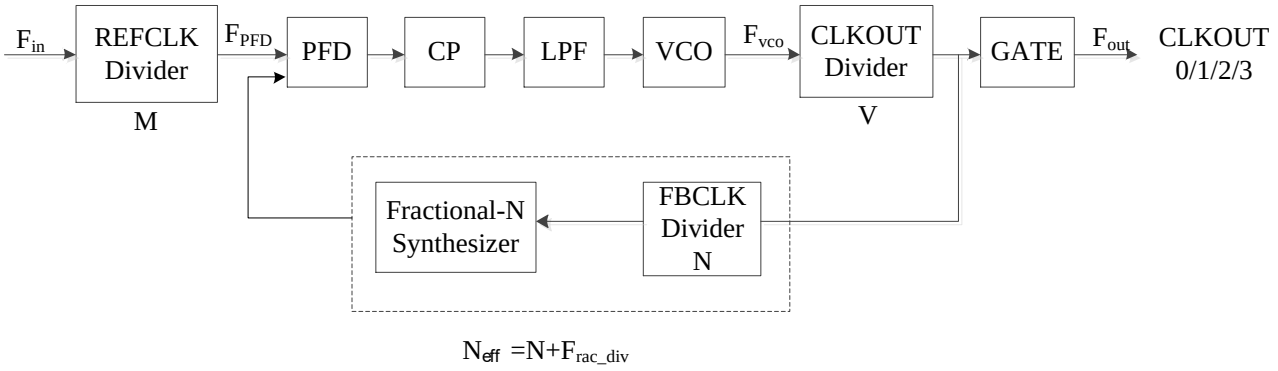

Figure 2-28 PLL Output Frequency Calculation Block Diagram

The definitions of the parameters in the figure are as follows:

Table 2-19 Definitions of Output Frequency Programming Parameters

Symbol	**Description**
Fin	Input reference frequency
FPFD	Input reference frequency of the PFD
Fvco	Output frequency of the VCO
Fout	Output frequency of the CLKOUT0/1/2/3
M	The division ratio of the input divider
V	The division ratio of the output divider
Neff	The division ratio of the feedback divider
N	The integer division ratio of the feedback divider
Frac_div	The fractional division ratio of the feedback divider

The calculation formulas of the parameters are as follows:

$F_{PFD} = F_{in}/M$

$F_{vco} = (F_{in}/M)*V*N_{eff}$

$F_{out} = F_{vco}/V$

$N_{eff}=N+ F_{rac\_div}$

Whereas, V in the calculation of F_{vco} represents the output division ratio of the feedback clock. If a clock that requires output Clock Frequency calculation is same as the feedback clock, then $F_{out} = (F_{in}/M)*N_{eff}$.

2.6.6 Fractional Frequency Synthesis

The PLL supports a 16-bit high-precision fractional division frequency synthesizer, the effective division number for the feedback divider is:

Neff = N + (F/65536)

Whereas, N is the integer division factor for the feedback divider, and F is the fractional division factor.

Note that the fractional division function only supports input reference clocks with a frequency greater than 20MHz.

2.6.7 PLL Lock Indication

Once the PLL's input reference clock is stable and the reset signal is released, the internal frequency locking module of the PLL starts working, with two counters in the reference clock domain and the feedback clock domain beginning their independent counts. When the count of the reference clock counter reaches the predetermined value of 8191, the frequency lock module captures the current count of the feedback clock counter. It compares the difference between the counts of the two counters with the lock accuracy threshold of 9. If the count difference is less than the accuracy threshold, the frequency is considered to be locked, and the PLL_LOCK is pulled high. If the count difference exceeds the lock accuracy threshold, both counters restart their count, and then the comparison is made again. At any time after frequency locking, if the count difference between the two counters exceeds the out-of-lock accuracy threshold of 16, it is considered that the PLL is out of lock, and the PLL_LOCK is pulled down.

The frequency accuracy calculation formula is shown as follows:

$$\Delta = \frac{N_{REFCLK} - N_{FBCLK}}{N_{REFCLK}} \times 10^6 \text{ ppm}$$

The lock accuracy of the PLL is ±1100ppm, and the out-of-lock accuracy is ±2000ppm.

When the frequency error is within the lock accuracy, the PLL is deemed to be locked, and the PLL_LOCK signal is high.

When the frequency error exceeds the out-of-lock accuracy, the PLL is deemed to be out of lock, and the PLL_LOCK signal is low.

The PLL frequency locking is divided into two modes: real-time monitoring mode and hold mode. Real-time monitoring mode refers to the PLL_LOCK pulled high when $\Delta \leq \pm 1100$ppm, with the frequency error monitored in real-time. As long as it does not exceed ±2000ppm, the PLL_LOCK signal remains high. Otherwise, the PLL_LOCK signal is pulled down. Hold mode refers to the PLL_LOCK signal remaining high after it has been pulled high unless the RST signal is active.

Users can configure the LOCK_MODE parameter to select the locking mode according to their needs, as described in Table 2-20. The LOCK_MODE can be configured either by directly instantiating GTP_PLL_E2 or by using the Advanced Configurations interface of the IPC PLL. Checking the "LOCK Latch Mode" option will select the hold mode.

Table 2-20 PLL Lock Mode

Parameter	Configuration Value	Function Description
LOCK_MODE	1'b0	Real-time monitoring mode: Pull high the LOCK signal within the lock precision range. As long as it does not exceed the out-of-lock accuracy, the LOCK signal may continue to be pulled high. Otherwise, the signal is pulled down
	1'b1	Hold mode: Pull high the LOCK signal within the lock precision range, and unless the PLL is reset or powered down, the LOCK signal remains high

2.6.8 Output Clock Phase Adjustment

After the chip enters user mode, the default phase relationship of the PLL's 4 output clocks, CLKOUT0, CLKOUT1, CLKOUT2, and CLKOUT3, is aligned. The PLL also supports the phase adjustment function of each output clock. Phase adjustment is divided into fine adjustment and coarse adjustment, each of which can be used to adjust the output clock's phase through static configuration and dynamic adjustment.

2.6.8.1 Phase Fine Adjustment

With respect to the input VCO clock, the minimum step for phase fine adjustment of the output clocks CLKOUT0/CLKOUT1/CLKOUT2/CLKOUT3 is $T_{vco}/8$, with an adjustment range of $0\sim7/8T_{vco}$; where T_{vco} is the VCO clock cycle.

- Static configuration

The static configuration for phase fine adjustment of the output clocks CLKOUT0, CLKOUT1, CLKOUT2, and CLKOUT3 is controlled by STATIC_PHASE0, STATIC_PHASE1, STATIC_PHASE2, and STATIC_PHASE3, respectively. Please refer to Table 2-21 for parameter descriptions.

For example, when the coarse phase adjustment parameters are all set to 0 and the output clock is a divide-by-two frequency of the VCO clock, the phase fine adjustment parameter settings are shown in the table.

Table 2-21 Static Phase Fine Adjustment Parameter Configuration

Phase Fine Adjustment Parameters	Configuration Value
STATIC_PHASE0	0

Phase Fine Adjustment Parameters	Configuration Value
STATIC_PHASE1	2
STATIC_PHASE2	4
STATIC_PHASE3	6

Based on the configuration values, the timing diagrams of phase fine adjustment for each output clock are shown in Figure 2-29:

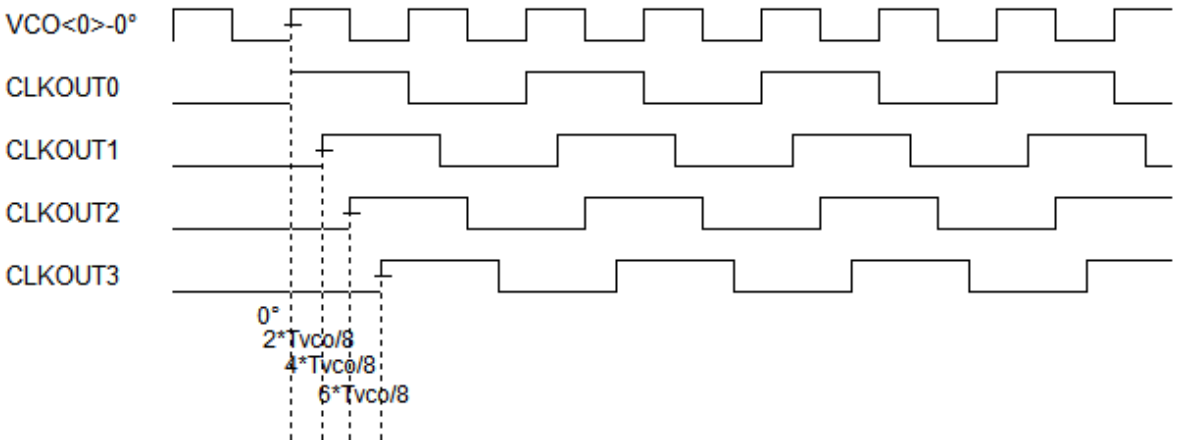

Figure 2-29 Phase Fine Adjustment Static Configuration

➢ Dynamic adjustment

The ports for dynamic phase fine adjustment include PHASE_SEL, PHASE_DIR, PHASE_STEP_N, and LOAD_PHASE. Please refer to Table 2-17 for port descriptions. All the output clocks CLKOUT0/CLKOUT1/CLKOUT2/CLKOUT3 have dynamic phase fine adjustment features, but only one output clock can be adjusted at a time.

PHASE_SEL and PHASE_DIR must remain stable before the LOAD_PHASE signal is triggered. LOAD_PHASE must be released before triggering the PHASE_STEP_N signal. Phase adjustment is achieved by triggering PHASE_STEP_N, with each trigger adjusting the phase by one step ($T_{vco}/8$). The PHASE_STEP_N signal must start from logic 1 and phase adjustment will start at the rising edge. When switching phase adjustment channels or directions, the current phase fine adjustment value of the selected channel must be loaded with the LOAD_PHASE signal. The timing requirements are shown in the figure below:

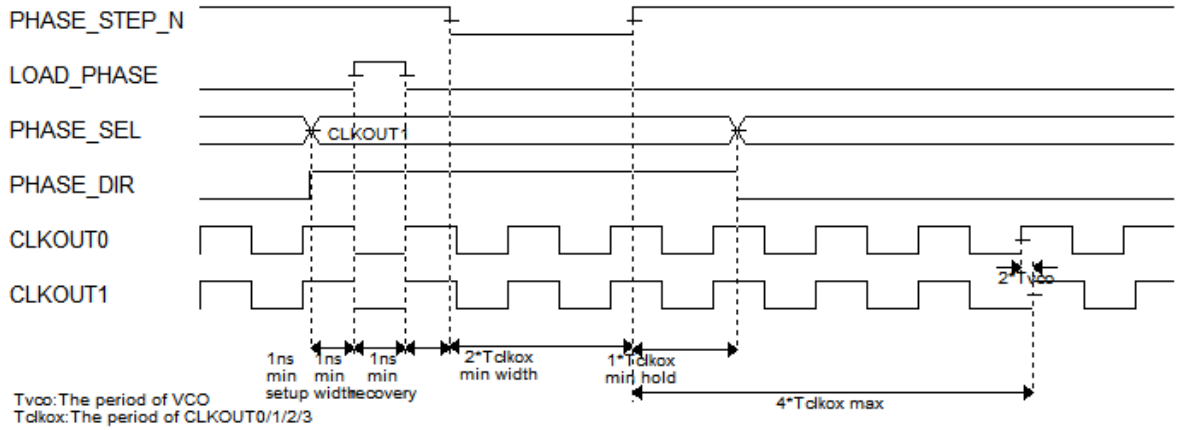

Figure 2-30 Timing Requirements of Dynamic Phase Fine-Tuning

2.6.8.2 Phase Coarse Adjustment

With respect to the input VCO clock, the minimum step for phase coarse adjustment of the output clocks CLKOUT0/CLKOUT1/CLKOUT2/CLKOUT3 is T_{vco}, with an adjustment range of [0~V-1]*T_{vco}, where V is the output divider factor.

➢ Static configuration

The static configuration for the phase coarse adjustment of the output clocks CLKOUT0, CLKOUT1, CLKOUT2, and CLKOUT3 is controlled by STATIC_CPHASE0, STATIC_CPHASE1, STATIC_CPHASE2, and STATIC_CPHASE3, respectively.

For example, when the phase fine adjustment parameters are all set to 0 and the output clock is a divide-by-four frequency of the VCO clock, the phase coarse adjustment parameter settings are shown in the table, and the timing diagram for the corresponding phase coarse adjustment are shown in Figure 2-31:

Table 2-22 Static Phase Coarse Adjustment Parameter Configuration

Phase Coarse Adjustment Parameters	**Configuration Value**
STATIC_CPHASE0	0
STATIC_CPHASE1	1
STATIC_CPHASE2	2
STATIC_CPHASE3	3

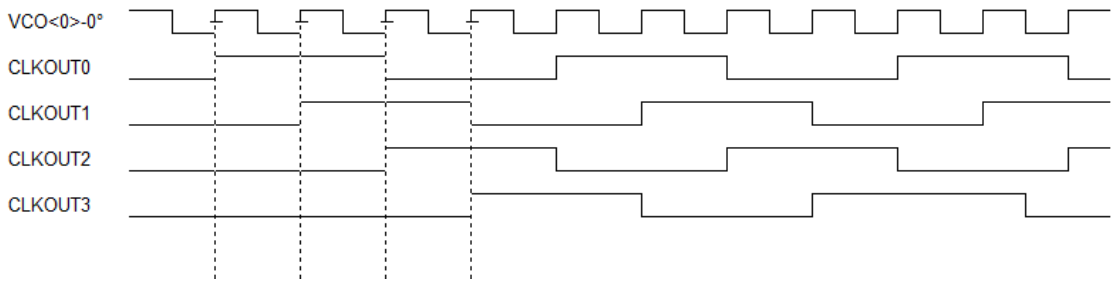

Figure 2-31 Coarse Phase Adjustment Static Configuration

Fine and coarse phase adjustments can be statically configured simultaneously, with configuration parameter are shown in the table below, and the corresponding timing diagrams is shown in Figure 2-32:

Table 2-23 Phase Static Parameters Configuration of Fine and Coarse Phase Adjustment

Phase Parameter	**Configuration Value**
STATIC_PHASE0	0
STATIC_PHASE1	2
STATIC_PHASE2	0
STATIC_PHASE3	2
STATIC_CPHASE0	0
STATIC_CPHASE1	0
STATIC_CPHASE2	1
STATIC_CPHASE3	1

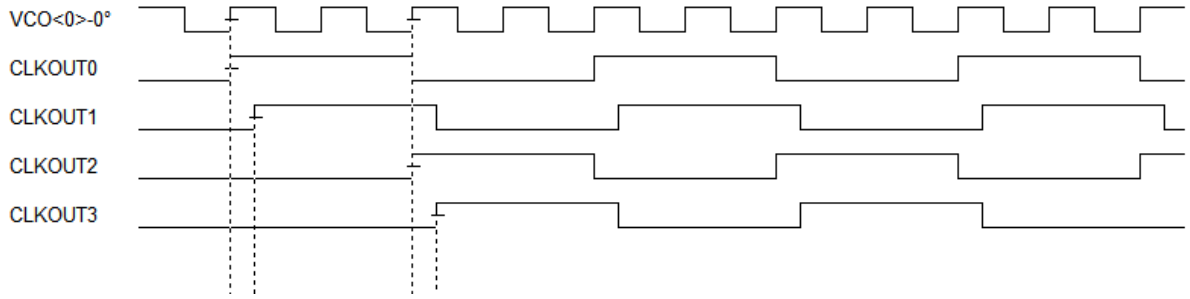

Figure 2-32 PLL Phase Static Configuration

The timing diagram resulting from phase parameter configuration values are shown in Table 2-23. CLKOUT0 is generated from a divide-by-two frequency of the VCO's 0 °clock. Taking CLKOUT0 as the reference, the fine adjustment phase for CLKOUT1 is $2*T_{vco}/8$ with a coarse adjustment phase of 0; CLKOUT2 has a fine adjustment phase of 0, with a coarse adjustment of phase T_{vco}; CLKOUT3 has a fine adjustment phase of $2*T_{vco}/8$, with a coarse adjustment phase of T_{vco}.

➢ Dynamic adjustment

The dynamic phase coarse adjustment ports are PHASE_SEL and CPHASE_STEP_N, with

dynamic phase coarse adjustment applied after a delay. Output clocks CLKOUT0/CLKOUT1/ CLKOUT2/ CLKOUT3 have the feature of dynamic coarse phase adjustment, but only one output clock can be adjusted at a time.

PHASE_SEL must maintain a stable configuration before the CPHASE_STEP_N signal is triggered. Once PHASE_SEL is set, phase adjustment is achieved by triggering CPHASE_STEP_N, adjusting by an increment of n* T_{vco} (with n* T_{vco} being the coarse adjustment initial value set by static configuration, and n ranging from 0 to 127). The CPHASE_STEP_N signal must start from logical 1 and begin phase adjustment at the rising edge, with timing requirements as shown in the figure below:

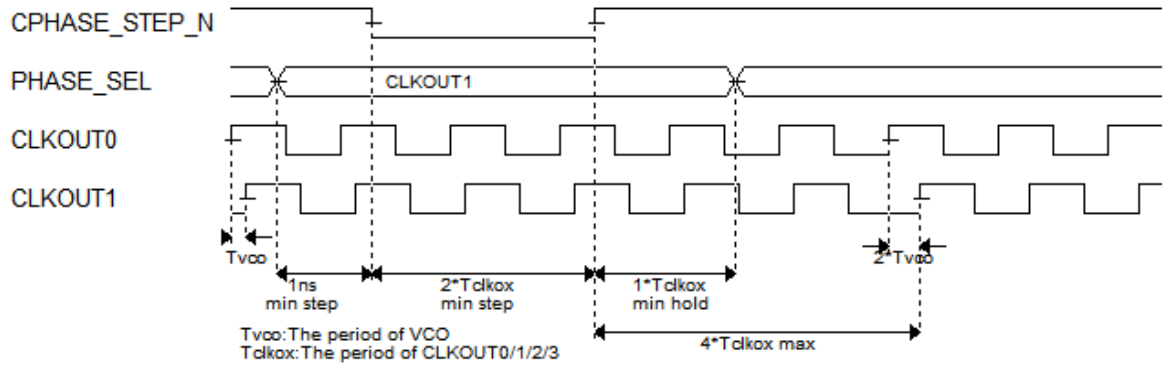

Figure 2-33 Timing Requirements of Dynamic Phase Coarse Adjustment

2.6.9 Output Clock Cascading

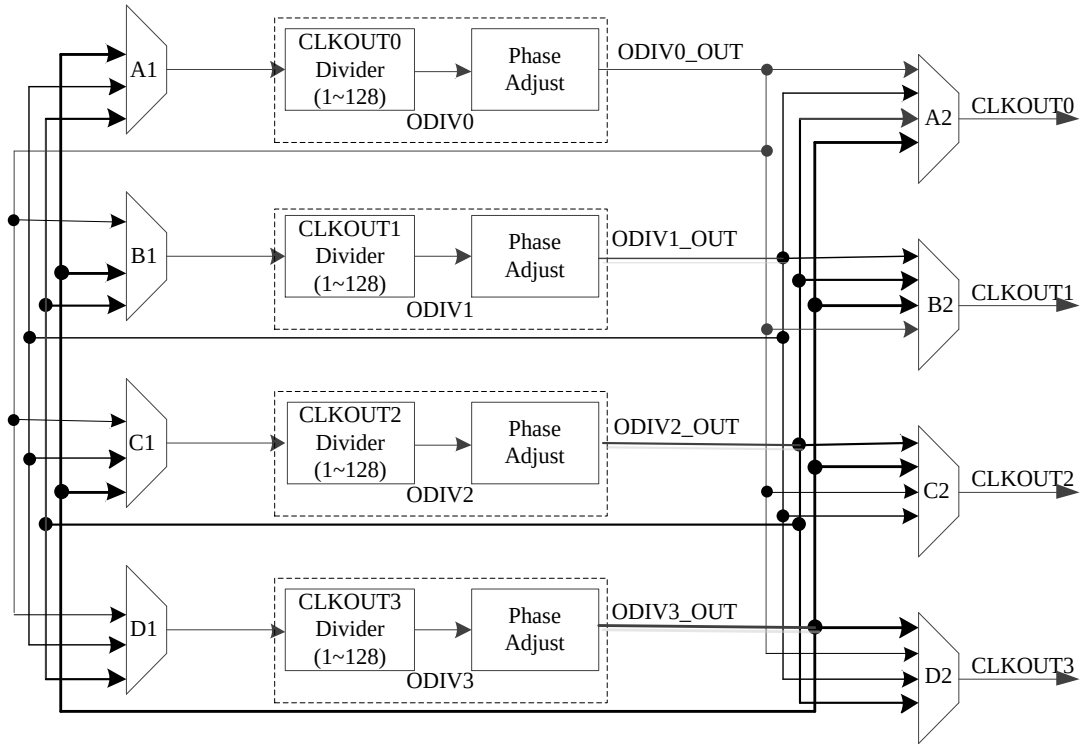

Figure 2-34 Output Clock Cascading Block Diagram

The PLL output clock cascading is shown in the figure above; the output clocks from the dividers (ODIV0/ODIV1/ODIV2/ODIV3), after being routed through multiplexers A1/B1/C1/D1, implement the cascading function of the dividers, generating clocks with lower frequency. The selection of all clock multiplexers in the diagram can be statically configured or dynamically changed via the APB port.

2.6.10 Output Clock Dynamic Enable

The PLL input signal CLKOUT0_SYN is used to enable and disable CLKOUT0 clock output; when the CLKOUT0 clock is not required, it can be turned off to reduce power consumption. The CLKOUT0_SYN signal is optional and is active when the user sets CLKOUT0_SYN_EN to "TRUE."

Similarly, the input signals CLKOUT1_SYN, CLKOUT2_SYN, and CLKOUT3_SYN work in conjunction with configuration bits CLKOUT1_SYN_EN, CLKOUT2_SYN_EN, and CLKOUT3_SYN_EN, respectively enabling and disabling the CLKOUT1, CLKOUT2, and CLKOUT3 clocks.

Taking the output clock CLKOUT0 as an example, the functional diagram is as follows:

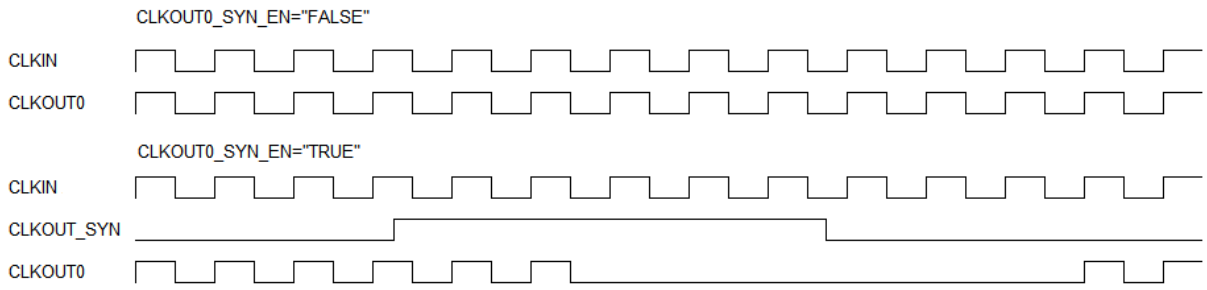

Figure 2-35 Output Clock GATE Timing Diagram

2.6.11 APB Ports

Allows user logic to change the PLL's operating parameters dynamically via the APB port. Writing configurations into the PLL's internal registers via APB port to change the PLL working parameters. It should be noted that:

- After the APB rewrites the input divider, output divider, and feedback divider ratios, a reset is required to ensure their normal working.
- After the APB rewrites the phase (fine or coarse adjustment) initial value, it is necessary to reset the PLL to load the initial value.

Table 2-24 APB Port Description

Port Signal	**Direction**	**Description**
APB_CLK	Input	Clock, sampled on the rising edge
APB_RST_N	Input	Asynchronous reset, active low; Only resets the data bus (does not reset register output)
APB_ADDR[4:0]	Input	Address bus
APB_SEL	Input	Selection signal, indicating that the slave device has been selected
APB_EN	Input	Enable signal, indicating the second and subsequent cycles of transmission
APB_WRITE	Input	Direction, 0: read, 1: write
APB_PWDATA[7:0]	Input	Data bus input

Table 2-25 Configuration Register Description: Address 0x00

Bits	**R/W**	**Corresponding Parameter Name**	**Description**
7:0	R/W	FRACN_DIV [7:0]	The lower 8 bits of the fractional divider configuration

Table 2-26 Configuration Register Description: Address 0x01

Bits	**R/W**	**Corresponding Parameter Name**	**Description**
7:0	R/W	FRACN_DIV [15:8]	The upper 8 bits of the fractional divider

Bits	R/W	Corresponding Parameter Name	Description
			configuration

Table 2-27 Configuration Register Description: Address 0x02

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	CLKI_DIV[7:0]	Division factor configuration of input divider

Table 2-28 Configuration Register Description: Address 0x03

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	CLKFB_DIV[7:0]	Division factor configuration of feedback divider

Table 2-29 Configuration Register Description: Address 0x04

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	CLKOUT0_DIV[7:0]	Division factor configuration of CLKOUT0 divider

Table 2-30 Configuration Register Description: Address 0x05

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	CLKOUT1_DIV[7:0]	Division factor configuration of CLKOUT1 divider

Table 2-31 Configuration Register Description: Address 0x06

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	CLKOUT2_DIV[7:0]	Division factor configuration of CLKOUT2 divider

Table 2-32 Configuration Register Description: Address 0x07

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	CLKOUT3_DIV[7:0]	Division factor configuration of CLKOUT3 divider

Table 2-33 Configuration Register Description: Address 0x08

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	CLKOUT0_CPHASE[7:0]	The phase coarse adjustment setting for CLKOUT0, with the value ranging from 0 to 127

Table 2-34 Configuration Register Description: Address 0x09

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	CLKOUT0_CPHASE[7:0]	The phase coarse adjustment setting for CLKOUT1, with the value ranging from 0 to 127

Table 2-35 Configuration Register Description: Address 0x0A

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	CLKOUT0_CPHASE[7:0]	The phase coarse adjustment setting for CLKOUT2, with the value ranging from 0 to 127

Table 2-36 Configuration Register Description: Address 0x0B

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	CLKOUT0_CPHASE[7:0]	The phase coarse adjustment setting for CLKOUT3, with the value ranging from 0 to 127

Table 2-37 Configuration Register Description: Address 0x0C

Bits	R/W	Corresponding Parameter Name	Description
2:0	R/W	CLKOUT0_FPHASE[2:0]	The phase fine adjustment static configuration for CLKOUT0, with the value ranging from 0 to 7
5:3	R/W	CLKOUT1_FPHASE[2:0]	The phase fine adjustment static configuration for CLKOUT1, with the value ranging from 0 to 7
6	R/W	CLKOUT0_SYN_ENABLE	Configuration for CLKOUT0_SYN signal enable, 1'b1: CLKOUT0_SYN signal is active 1'b0: CLKOUT0_SYN signal is inactive
7	R/W	CLKOUT1_SYN_ENABLE	Configuration for CLKOUT1_SYN signal enable, 1'b1: CLKOUT1_SYN signal is active 1'b0: CLKOUT1_SYN signal is inactive

Table 2-38 Configuration Register Description: Address 0x0D

Bits	R/W	Corresponding Parameter Name	Description
2:0	R/W	CLKOUT2_FPHASE[2:0]	The phase fine adjustment static configuration for CLKOUT2, with the value ranging from 0 to 7
5:3	R/W	CLKOUT3_FPHASE[2:0]	The phase fine adjustment static configuration for CLKOUT3, with the value ranging from 0 to 7
6	R/W	CLKOUT2_SYN_ENABLE	Configuration for CLKOUT2_SYN signal enable, 1'b1: CLKOUT2_SYN signal is active 1'b0: CLKOUT2_SYN signal is inactive
7	R/W	CLKOUT3_SYN_ENABLE	Configuration for CLKOUT3_SYN signal enable, 1'b1: CLKOUT3_SYN signal is active 1'b0: CLKOUT3_SYN signal is inactive

Table 2-39 Configuration Register Description: Address 0x0E

Bits	R/W	Corresponding Parameter Name	Description
1:0	R/W	ODIV0_CLKIN_SEL[1:0]	The MUXA1 configuration in front of the CLKOUT0 divider; 2'b00: select the output of the MUXA0, 2'b01: select the output of the CLKOUT3 divider, 2'b10: select the output of the CLKOUT1 divider, 2'b11: select the output of the CLKOUT2 divider;
3:2	R/W	ODIV1_CLKIN_SEL[1:0]	The MUXB1 configuration in front of the CLKOUT1 divider;

Bits	R/W	Corresponding Parameter Name	Description
			2'b00: select the output of the MUXB0, 2'b01: select the output of the CLKOUT0 divider, 2'b10: select the output of the CLKOUT3 divider, 2'b11: select the output of the CLKOUT2 divider;
5:4	R/W	ODIV2_CLKIN_SEL[1:0]	The MUXC1 configuration in front of the CLKOUT2 divider; 2'b00: select the output of the MUXC0, 2'b01: select the output of the CLKOUT0 divider, 2'b10: select the output of the CLKOUT1 divider, 2'b11: select the output of the CLKOUT3 divider;
7:6	R/W	ODIV3_CLKIN_SEL[1:0]	The MUXD1 configuration in front of the CLKOUT3 divider; 2'b00: select the output of the MUXD0, 2'b01: select the output of the CLKOUT0 divider, 2'b10: select the output of the CLKOUT1 divider, 2'b11: select the output of the CLKOUT2 divider;

Table 2-40 Configuration Register Description: Address 0x0F

Bits	R/W	Corresponding Parameter Name	Description
2:0	R/W	CLKOUT0_SEL[2:0]	The MUXA2 configuration behind the CLKOUT0 divider; 3'b000: select the output of the CLKOUT0 divider, 3'b001: select the output of the CLKOUT1 divider, 3'b010: select the output of the CLKOUT2 divider, 3'b011: select the output of the CLKOUT3 divider, 3'b100: select the reference clock CLKIN;
5:3	R/W	CLKOUT1_SEL[2:0]	The MUXB2 configuration behind CLKOUT1 divider; 3'b000: select the output of the CLKOUT1 divider, 3'b001: select the output of the CLKOUT2 divider, 3'b010: select the output of the CLKOUT3 divider, 3'b011: select the output of the CLKOUT0 divider, 3'b100: select the reference clock CLKIN;
6	R/W	VCOCLK_BYPASS0	The VCO clock bypass configuration (MUXA0 configuration bit); 1'b0: No bypass (select the VCO clock), 1'b1: bypass (select the reference clock CLKIN);
7	R/W	VCOCLK_BYPASS1	The VCO clock bypass configuration (MUXB0 configuration bit); 1'b0: No bypass (select the VCO clock), 1'b1: bypass (select the reference clock CLKIN);

Table 2-41 Configuration Register Description: Address 0x10

Bits	R/W	Corresponding Parameter Name	Description
2:0	R/W	CLKOUT2_SEL[2:0]	The MUXC2 configuration behind the CLKOUT2 divider; 3'b000: select the output of the CLKOUT2 divider, 3'b001: select the output of the CLKOUT3 divider, 3'b010: select the output of the CLKOUT0 divider, 3'b011: select the output of the CLKOUT1 divider, 3'b100: select the reference clock CLKIN;

Bits	R/W	Corresponding Parameter Name	Description
5:3	R/W	CLKOUT3_SEL[2:0]	The MUXD2 configuration behind the CLKOUT3 divider; 3'b000: select the output of the CLKOUT3 divider, 3'b001: select the output of the CLKOUT0 divider, 3'b010: select the output of the CLKOUT1 divider, 3'b011: select the output of the CLKOUT2 divider, 3'b100: select the reference clock CLKIN;
6	R/W	VCOCLK_BYPASS2	The VCO clock bypass configuration (MUXC0 configuration bit); 1'b0: No bypass (select VCO clock), 1'b1: bypass (select the reference clock CLKIN);
7	R/W	VCOCLK_BYPASS3	The VCO clock bypass configuration (MUXD0 configuration bit); 1'b0: No bypass (select VCO clock), 1'b1: bypass (select the reference clock CLKIN);

Table 2-42 Configuration Register Description: Address 0x11

Bits	R/W	Corresponding Parameter Name	Description
0	R/W	STDBY_ENABLE	STDBY signal enable configuration; 1'b0: STDBY signal is inactive, 1'b1: STDBY signal is active;
1	R/W	PLL_PWD_ENABLE	PLL_PWD signal enable configuration; 1'b0: PLL_PWD signal is inactive, 1'b1: PLL_PWD signal is active;
2	R/W	RST_ENABLE	Reset signal RST enable configuration; 1'b0: RST signal is inactive, 1'b1: RST signal is active;
3	R/W	RSTODIV_ENABLE	Reset signal RSTODIV enable configuration; 1'b0: RSTODIV signal is inactive, 1'b1: RSTODIV signal is active;
4	R/W	RSTODIV2_ENABLE	Reset signal RSTODIV2 enable configuration; 1'b0: RSTODIV2 signal is inactive, 1'b1: RSTODIV2 signal is active;
5	R/W	RSTODIV3_ENABLE	Reset signal RSTODIV3 enable configuration; 1'b0: RSTODIV3 signal is inactive, 1'b1: RSTODIV3 signal is active;
6	R/W	PLL_RST_APB	Function consistent with the dynamic port RST; 1'b0: PLL operates normally, 1'b1: PLL reset
7	R/W	PLL_PWD_APB	Function consistent with the dynamic port PLL_PWD; 1'b0: PLL on, 1'b1: PLL off;

Table 2-43 Configuration Register Description: Address 0x12

Bits	R/W	Corresponding Parameter Name	Description
1:0	R/W	PHASESEL_APB[1:0]	Function consistent with the dynamic port PHASE_SEL; Select the corresponding PLL output clock for phase adjustment; 2'b00: Selects the CLKOUT0, 2'b01: Selects the CLKOUT3,

Bits	R/W	Corresponding Parameter Name	Description
			2'b10: Selects the CLKOUT2, 2'b11: Selects the CLKOUT1;
2	R/W	PHASEDIR_APB	Function consistent with the dynamic port PHASE_DIR; Select the direction for dynamic phase fine adjustment; 1'b0: lag, 1'b1: lead;
3	R/W	PHASESTEP_N_APB	Function consistent with the dynamic port PHASE_STEP_N; Dynamic phase fine adjustment trigger signal; Each trigger adjusts the output clock phase by $1/8T_{vco}$
4	R/W	LOAD_PHASE_APB	Function consistent with the dynamic port LOAD_PHASE; Load signal for the current phase fine adjustment value of the selected channel, pulse signal, active-high;
5	R/W	CPHASESTEP_N_APB	Function consistent with the dynamic port CPHASE_STEP_N; Dynamic phase coarse adjustment trigger signal; Each trigger increments the counter by 1, adjusting the output clock phase by n*step (n*step determined by the initial value configured by static parameters)
6	R/W	DPHASE_SOURCE	Source configuration for control signal of dynamic phase adjustment; 1'b0: control signal from the dynamic port (SRB), 1'b1: control signal from the APB port;
7	R/W	DPFDEN_SOURCE	PFDEN enable signal source configuration of PLL PFD; 1'b0: control signal from the dynamic port (SRB), 1'b1: control signal from the APB port;

Table 2-44 Configuration Register Description: Address 0x13

Bits	R/W	Corresponding Parameter Name	Description
0	R/W	ICP_BASE_TRIM	CP current correction configuration in PLL; 1'b0: 5μA per step; 1'b1: 2.5μA per step;
1	R/W	FRACN_ENABLE	Fractional division function enable; 1'b0: Off, 1'b1: On;
4:2	R/W	LOCK_ACCURACY[2:0]	PLL frequency detection accuracy configuration; 3'b000:Lockin: ±1100ppm;Lockout: ±2000ppm; 3'b001:Lockin: ±5100ppm;Lockout: ±10000ppm; 3'b010:Lockin: ±10300ppm;Lockout: ±20000ppm; 3'b011:Lockin: ±15600ppm;Lockout: ±29300ppm; 3'b100:Lockin: ±20500ppm;Lockout: ±40100ppm; 3'b101:Lockin: ±30300ppm;Lockout: ±48900ppm; 3'b110:Lockin: ±49900ppm;Lockout: ±78200ppm; 3'b111:Lockin: ±550ppm; Lockout: ±1000ppm;
5	R/W	LOCK_MODE	PLL frequency detection mode configuration; 1'b0: normal frequency detection; 1'b1: maintains the state after frequency lock unless PLL is reset or powered down;

Bits	R/W	Corresponding Parameter Name	Description
6	R/W	PFDEN_APB	PLL PFD enable signal; 1'b0: PFD off, 1'b1: PFD on;
7	R/W	PFDEN_ENABLE	PFDEN signal enable configuration; 1'b0: PFDEN signal is inactive, 1'b1: PFDEN signal is active;

Users can control the PLL by directly instantiating GTP_APB, the corresponding port diagram of which is shown below, and the port descriptions are shown in Table 2-45.

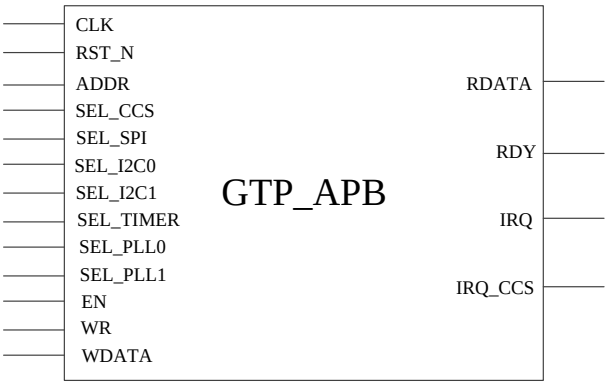

Figure 2-36 GTP_APB Diagram

Table 2-45 GTP_APB Port Description

Port	Direction	Function Description
CLK	Input	Clock
RST_N	Input	Asynchronous reset
ADDR	Input	Address bus
SEL_CCS	Input	Select CCS
SEL_SPI	Input	Select SPI
SEL_I2C0	Input	Select I2C0
SEL_I2C1	Input	Select I2C1
SEL_TIMER	Input	Select timer
SEL_PLL0	Input	Select PLL0
SEL_PLL1	Input	Select PLL1
EN	Input	Enabled
WR	Input	Read/write selection
WDATA	Input	Data bus input
RDATA	Output	Data bus output
RDY	Output	Ready
IRQ	Output	Master interrupt
IRQ_CCS	Output	CCS interrupt

Taking Verilog instantiation as an example, the call method for GTP_APB is as follows:

```
GTP_APB
I_GTP_APB
(
.CLK          CLK          ),
.RST_N        RST_N        ),
.ADDR         (ADDR        ),
.SEL_CCS      (SEL_CCS     ),
.SEL_SPI      (SEL_SPI     ),
.SEL_I2C0     (SEL_I2C0    ),
.SEL_I2C1     (SEL_I2C1    ),
.SEL_TIMER    (SEL_TIMER   ),
.SEL_PLL0     (SEL_PLL0    ),
.SEL_PLL1     (SEL_PLL1    ),
.EN           (EN          ),
.WR           (WR          ),
.WDATA        (WDATA       ),
.RDATA        (RDATA       ),
.RDY          (RDY         ),
.IRQ          (IRQ         ),
.IRQ_CCS      (IRQ_CCS     )
);
```

The read and write timing of APB is divided into the following types:

- Write without wait

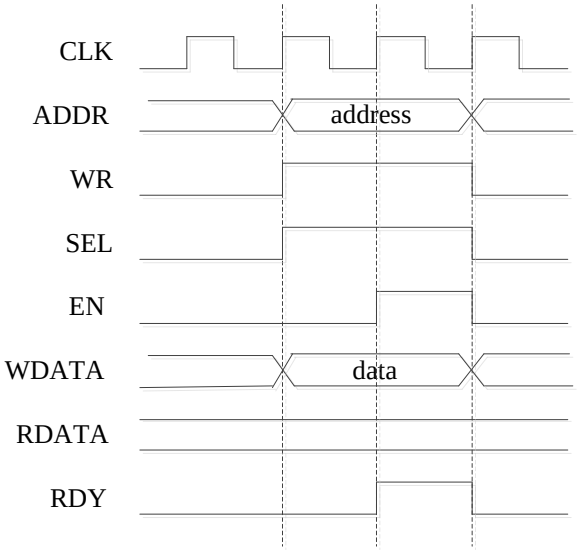

Figure 2-37 Timing of APB Write without Wait

➢ Write with wait

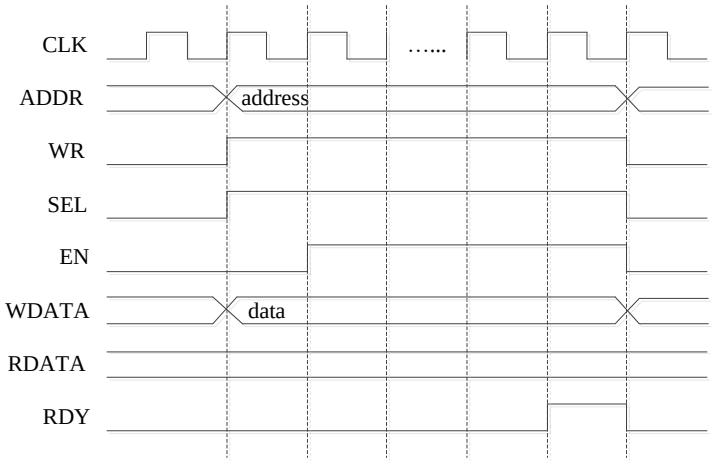

Figure 2-38 Timing of APB Write with Wait

➢ Continuous write

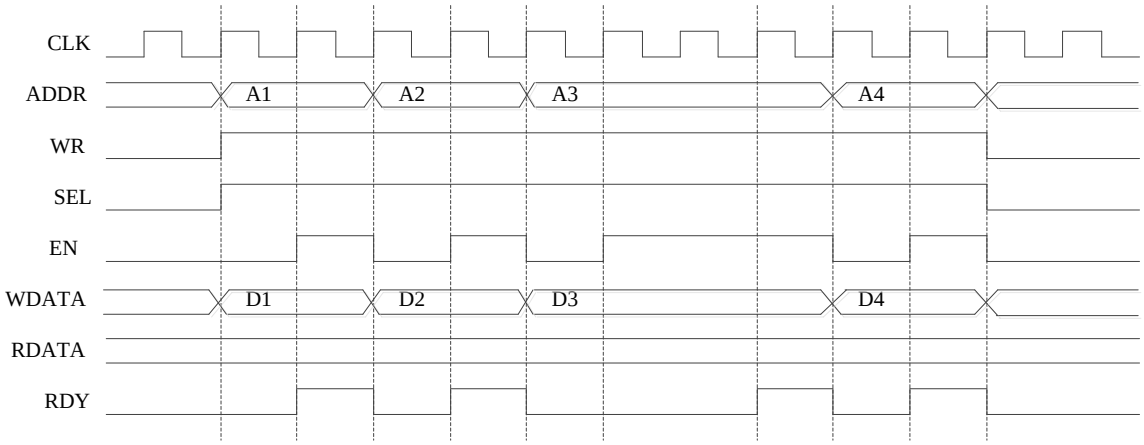

Figure 2-39 Timing of APB Continuous Write

➢ Read without wait

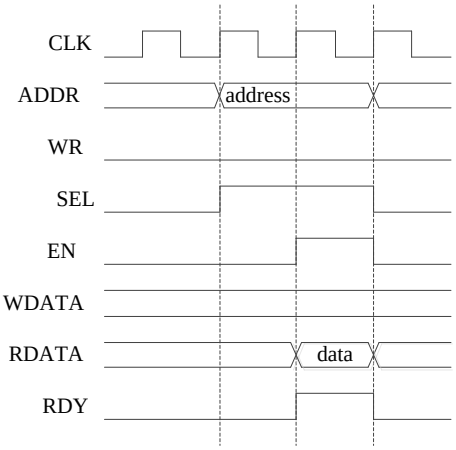

Figure 2-40 Timing of APB Read without Wait

➢ Read with wait

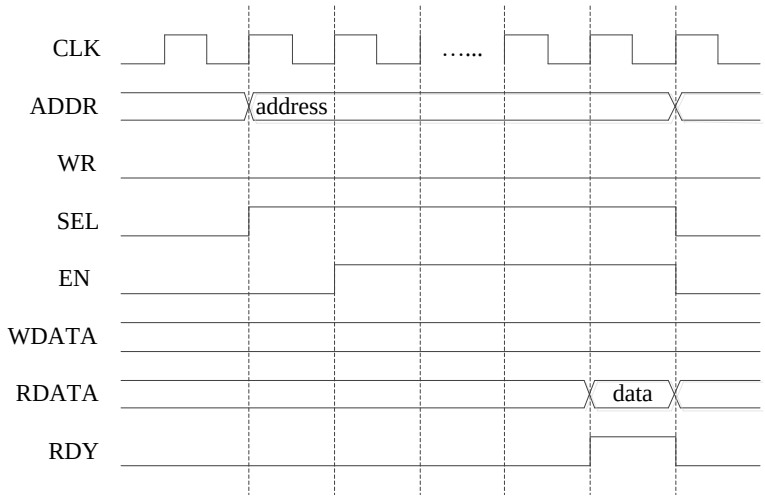

Figure 2-41 Timing of APB Read with Wait

➢ Continuous read

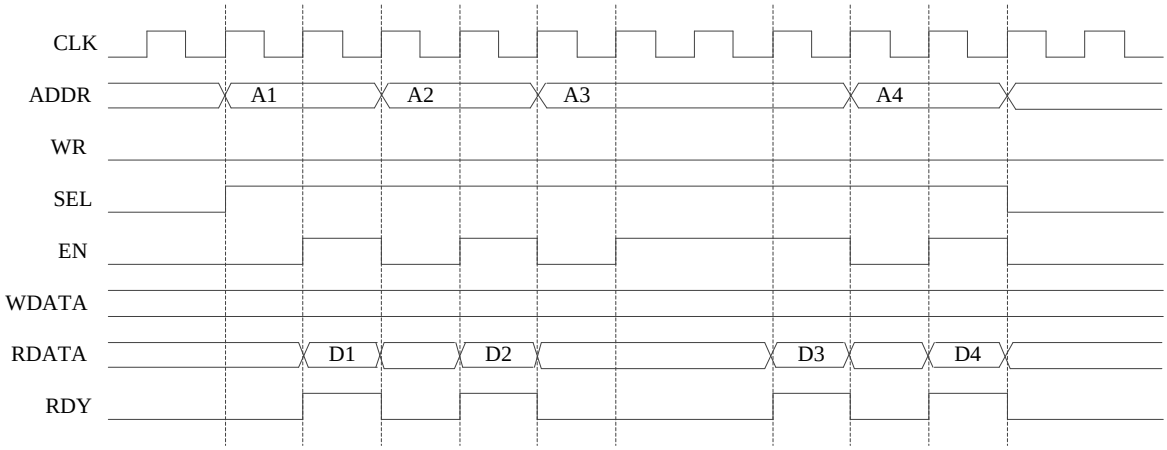

Figure 2-42 Timing of APB Continuous Read

➢ Write before read

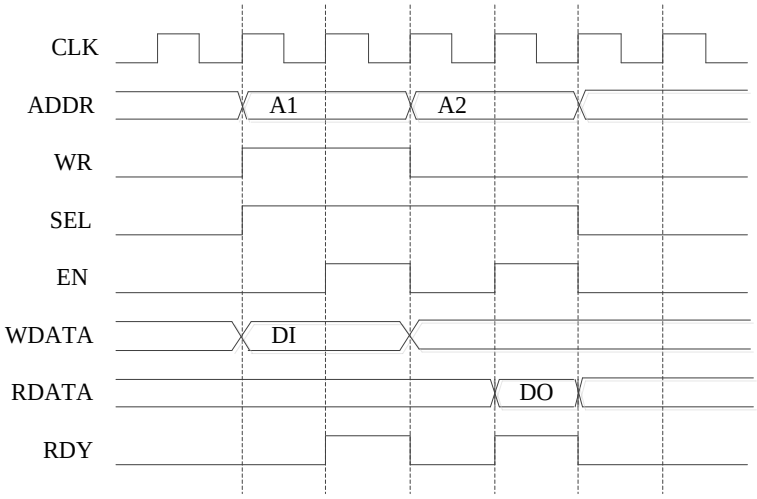

Figure 2-43 Timing of APB Write before Read

➢ Read before write

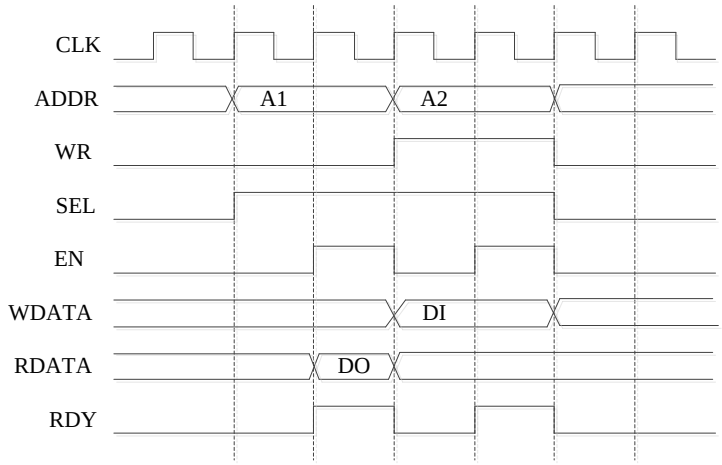

Figure 2-44 Timing of APB Read before Write

2.7 Internal Oscillator (OSC)

Compa family products provide an internal oscillator (OSC), which can be used as a clock source. The output clock from the internal oscillator can be used as a global clock input source. The OSC can be used by directly instantiating GTP_OSC_E2, with its structure block diagram shown below, the port descriptions shown in Table 2-46, and the parameter descriptions in Table 2-47.

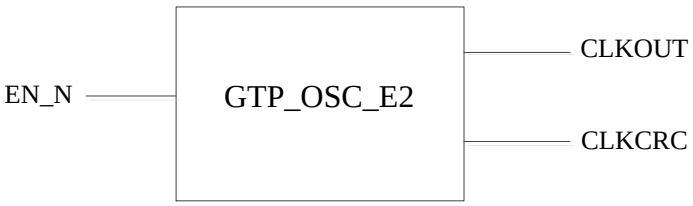

Figure 2-45 GTP_OSC_E2 Structure Block Diagram

Table 2-46 GTP_OSC_E2 Port Description

Port Name	Direction	Description
CLKOUT	Output	Output clock for user, with output frequency configured by CLK_DIV; please refer to Table 2-49 for the frequency that can be output. The port goes through the global clock network
CLKCRC	Output	Output clock, default frequency of 2.08MHz, provides clock for GTP_RBCRC
EN_N	Input	OSC output enable signal, which turns off OSC when high and turns on OSC when low

Table 2-47 GTP_OSC_E2 Parameter Description

Parameter	Description
CLK_DIV	Clock division factor setting, with the valid value ranging from 0 to 127

Parameter	Description
USER_DIV_EN	Clock division enable configuration, the value may be "FALSE" or "TRUE," and is active when "TRUE"

The correspondence between CLK_DIV values and division factors is shown in Table 2-48:

Table 2-48 Correspondence Between CLK_DIV Values and Division Factors

CLK_DIV	Division Factor
0	128
1	2
2	2
3	3
…	…
125	125
126	126
127	127

The frequency that can be output by CLKOUT are shown in Table 2-49:

Table 2-49 CLKOUT Output Frequency

OSC Output Frequency (Division Factor), in MHz							
2.08(128)	2.09(127)	2.11(126)	2.13(125)	2.15(124)	2.16(123)	2.18(122)	2.20(121)
2.22(120)	2.24(119)	2.25(118)	2.27(117)	2.29(116)	2.31(115)	2.33(114)	2.35(113)
2.38(112)	2.40(111)	2.42(110)	2.44(109)	2.46(108)	2.49(107)	2.51(106)	2.53(105)
2.56(104)	2.58(103)	2.61(102)	2.63(101)	2.66(100)	2.69(99)	2.71(98)	2.74(97)
2.77(96)	2.80(95)	2.83(94)	2.86(93)	2.89(92)	2.92(91)	2.96(90)	2.99(89)
3.02(88)	3.06(87)	3.09(86)	3.13(85)	3.17(84)	3.20(83)	3.24(82)	3.28(81)
3.33(80)	3.37(79)	3.41(78)	3.45(77)	3.50(76)	3.55(75)	3.59(74)	3.64(73)
3.69(72)	3.75(71)	3.80(70)	3.86(69)	3.91(68)	3.97(67)	4.03(66)	4.09(65)
4.16(64)	4.22(63)	4.29(62)	4.36(61)	4.43(60)	4.51(59)	4.59(58)	4.67(57)
4.75(56)	4.84(55)	4.93(54)	5.02(53)	5.12(52)	5.22(51)	5.32(50)	5.43(49)
5.54(48)	5.66(47)	5.78(46)	5.91(45)	6.05(44)	6.19(43)	6.33(42)	6.49(41)
6.65(40)	6.82(39)	7.00(38)	7.19(37)	7.39(36)	7.60(35)	7.82(34)	8.06(33)
8.31(32)	8.58(31)	8.87(30)	9.17(29)	9.50(28)	9.85(27)	10.23(26)	10.64(25)
11.08(24)	11.57(23)	12.09(22)	12.67(21)	13.30(20)	14.00(19)	14.78(18)	15.65(17)
16.63(16)	17.73(15)	19.00(14)	20.46(13)	22.17(12)	24.18(11)	26.60(10)	29.56(9)
33.25(8)	38.00(7)	44.33(6)	53.20(5)	66.50(4)	88.67(3)	133.00(2)	

Taking Verilog instantiation as an example, the call method for GTP_OSC_E2 is as follows:

GTP_ OSC_E2

#(

```
    . USER_DIV_EN      ("TRUE"     ),      //FALSE; TRUE
     . CLK_DIV         (0          )       //0-127
) I_ GTP_ OSC_E2   (
.CLKOUT            (CLKOUT   ),
.CLKCRC            (CLKCRC   ),
.EN_N              (EN_N     )
);
```

When the parameter USER_DIV_EN is set to "TRUE" and CLK_DIV is 0, the timing diagram is shown in the figure below:

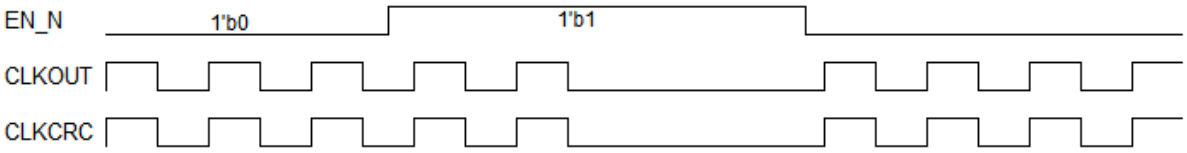

Figure 2-46 GTP_OSC_E2 Timing Diagram

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