PG2L100H_FBG676

(PK04001, V1.3)

(13.07.2023)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.3	13.07.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Full Spelling
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

PG2L100H_FBG676 uses a Wire-Bond BGA type of packaging. Package size: 27x27mm; Number of balls: 676; Ball pitch: 1.0mm; Maximum package thickness: 2.35mm

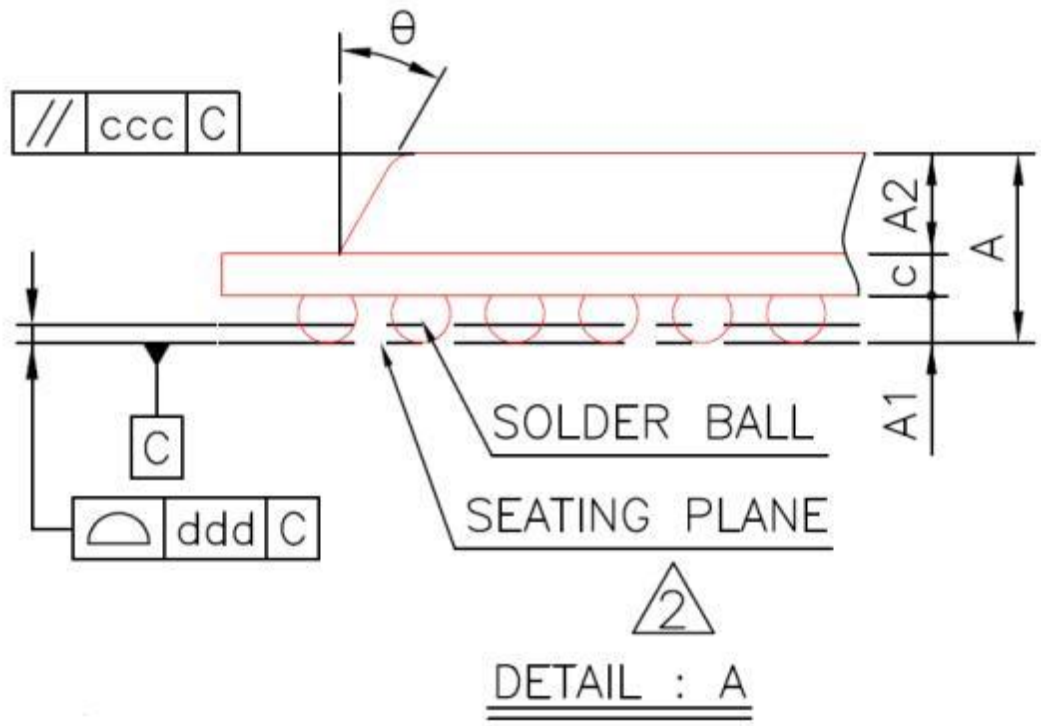
Chapter 2 Package Dimension and Pin

2.1 Package Dimension

Table 2-1 Dimensional Values

Note: Unit in millimeter

Dimension Symbol	Value			Dimension Symbol	Value		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	2.05	2.20	2.35	c	0.51	0.56	0.61
A1	0.42	0.47	0.52	e	-	1.0	-
A2	1.12	1.17	1.22	b	0.57	0.62	0.67
D	26.8	27.0	27.2	aaa	-	-	0.20
E	26.8	27.0	27.2	ccc	-	-	0.20
D1	-	25.0	-	ddd	-	-	0.15
E1	-	25.0	-	eee	-	-	0.25
D2	23.80	24.0	24.20	D3	-	18.0	-
E2	23.80	24.0	24.20	E3	-	18.0	-



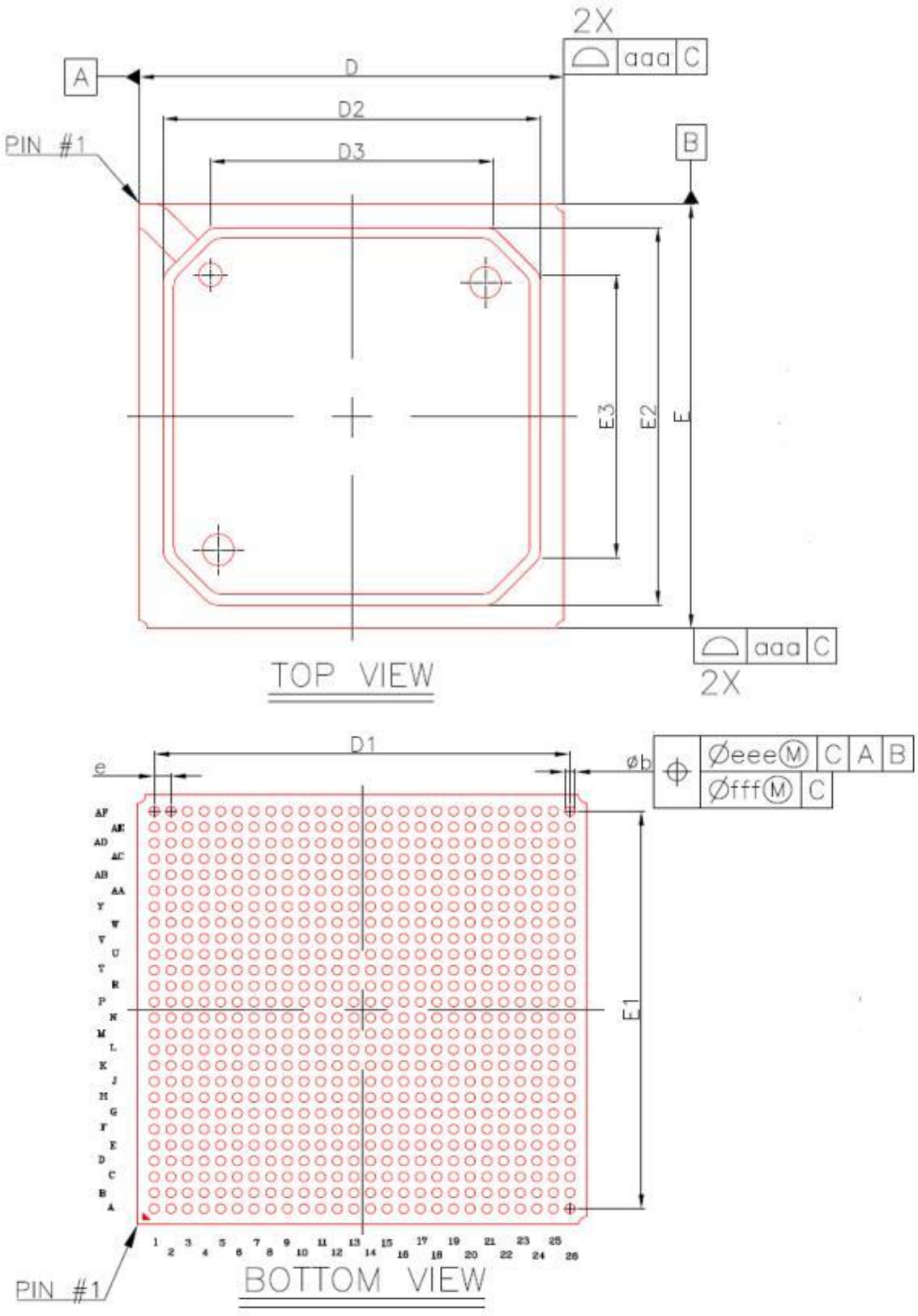


Figure 2-1 Package Outline Dimension (POD)

Note: Pin #1 is the pin 1 position of the chip.

2.2 Pin Definitions

PG2L100H_FBG676 has 300 user IOs.

Table 2-2 Product Pin Definitions

PIN Name	PIN Type	PIN Direction	PIN Description
General PIN			
DIFFIO_XX_GY_NN[P,N]	General	Input/Output	General pin; (1) "DIFFIO" indicates the pin supports differential input/output and can be used for transmitting and receiving LVDS signals; (2) " XX " indicates bank numbers, which can be L3, L4, L5, L6, R4, R5; (3) " G " indicates belonging to a memory group; (4) " Y " indicates the group number in a bank, each of which contains four groups; (5) "NN" indicates the sequence number of programmable IO pairs in a bank, increasing from 0, a bank contains 24 difference pairs; (6) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end; During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri-state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.
SIO_XX_NN	General	Input/Output	General pin; (1) " SIO " indicates the pin only supports single ended input/output; (2) " XX " indicates bank numbers, which can be L3, L4, L5, L6, R4, R5; (3) "NN" indicates the sequence number of programmable IO in a bank, increasing from 0, a bank contains 2 single ended IOs; During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri- state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.
Configuration PIN			
INIT_FLAG_N	Dedicated	Bidirectional (open-drain)	Initialization and configuration status dedicated pin: When it is low, it indicates that the FPGA is being initialized (clear configuration memory) or a configuration error has occurred. The pin has an internal weak pull-up resistor that is enabled during configuration; When the FPGA powers up completion, the pin is driven to low level. Once the FPGA completes initialization, the pin is released. During the power up and initialization process, this pin can accept an external low level input to delay the configuration process. When the FPGA detects high level input on this pin after initialization, the FPGA starts the configuration process.During configuration, this pin serves as an output

PIN Name	PIN Type	PIN Direction	PIN Description
			for the configuration error indication state, and low level indicates that an error occurred. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. After the configuration is complete, user can configure weak pull-up or float state for this pin.
CFG_DONE	Dedicated	Bidirectional (open-drain)	Dedicated configuration status pin, built in weak pull-up resistor about 10K. Output as the configuration completion indicator, high level indicates that the configuration is complete. This pin is an open-drain output. When the FPGA powers up completion, the pin is driven to low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released. After the configuration is complete, the pin can be driven externally to low level, Once the internal start-up timing finds that the external DONE pin is low and the internal start-up circuit stops until the external pin is high. After the configuration is complete, user can configure weak pull-up or float state for this pin.
RSTN	Dedicated	Input	Dedicated configuration reset pin, built in weak pull-up resistor and always effective. For restarting configuration logic and configuration memory, active-low. When this pin is low, the FPGA configuration memory is emptied and a new configuration process begins. The configuration logic reset begins with the falling edge of the pin, and the configuration process begins with the rising edge of the pin. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. Keeping this pin low during power up does not put the FPGA configuration logic in a reset state. After the configuration is complete, user can configure weak pull-up or float state for this pin.
CFG_CLK	Dedicated	Input/Output	Configuration clock pin. Except for the JTAG configuration mode, the configuration process of the FPGA is synchronizing by this clock in other modes. In the slave serial and slave parallel configuration modes, the pin serves as a clock input to obtain configuration data from external sources. In the master SPI configuration mode, the pin serves as a clock output to obtain configuration data from external sources and an external pull-up resistor of 1K is required. When the clock is not needed (such as in the JTAG mode), this pin is in the High-Z state. After the configuration is complete, user can configure weak pull-up or float state for this pin.
TCK	Dedicated	Input	Test clock input pin compliant with IEEE STD 1149.1 and provides a clock for the JTAG chain of the FPGA. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TMS	Dedicated	Input	Dedicated JTAG test mode selection input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDI	Dedicated	Input	Dedicated JTAG test data input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDO	Dedicated	Output	Dedicated JTAG test data output pin

PIN Name	PIN Type	PIN Direction	PIN Description
			Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
MODE_2	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_1	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_0	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
SCBV	Dedicated	Input	The pin is always effective on BANKCFG, but only on BANK which the multiplexing configuration pins is located during configuration. When the voltage of VCCIOCFG is 2.5V or 3.3V, the pin must be connected to high level and can be connected directly to the VCCIOCFG. When the voltage of VCCIOCFG is 1.8V or lower, the pin must be connected to low level and can be connected directly to the ground. Note: The pin must be used in conjunction with the software, and the SCBV selection in the bitstream setting must be consistent with the hardware setting. For details about the SCBV pin pull-up/pull-down level corresponds to the configured BANK power, see "UG040012_Logos2 Family Hardware Design Guide".
FCS_N	Multiplexed	Output	Multi-function configuration pin, used for the Master SPI configuration mode. (1) In the Master SPI X1, X2 and X4 modes, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
MOSI_D0	Multiplexed	Input/Output	Multi-function configuration data pin. (1) "MOSI", in the master SPI X1 mode; this pin used for serial data output and connects to the data input pin of the external SPI flash (such as DQ0,D,SI,IO0, etc). After the command and address are sent to the external SPI flash, the pin output high-Z or weak pull-up, depending on the state of the IO_STATUS_C pin. (2) In the master SPI X2, X4 and X8 modes, the pin is bidirectional data port, as command and address output to the external SPI flash. Receive the lowest bit data from the external SPI flash. The pin connects to the bidirectional data pin of the external SPI flash (such as DQ0,D,SI,IO0, etc). (3) " D0" , in the slave parallel mode, this pin serves as the D[0] bit of the data bus.

PIN Name	PIN Type	PIN Direction	PIN Description
			(4) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (5) After the configuration is complete, the pin serves as a general pin.
MISO_D1_DI	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X1 mode, "MISO" serves as data input and connects to the data output pin of the external SPI flash (such as DQ1,Q,SO,IO1, etc). (2) In the master SPI X2, X4 and X8 modes, "D1" connects to the second serial data output pin of the external SPI flash (such as DQ1,Q,SO,IO1, etc). (3) In the slave parallel mode, this pin serves as the D[1] bit of the data bus. (4) In the slave serial mode, "D1" serves as data input pin. (5) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. In the other configuration modes(such as JTAG), the state on the pin is ignored (6) After the configuration is complete, the pin serves as a general pin.
D[2 , 3]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X4 and X8 modes, serve as data input and connects to the data output pin of the external SPI flash. "D2" connects to the third bit data output pin of the external SPI flash (such as DQ2,W#,WP#,IO2, etc). "D3" connects to the fourth bit data output pin of the external SPI flash (such as DQ3,HOLD#, IO3, etc). These pins should be connected to VCCIO via an external weak pull-up resistor of 4.7K. (2) In the slave parallel mode, these pins serve as the D[3:2] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[4 , 5 , 6 , 7]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X8 mode, connect to the second flash in the same way as D[3:0]. (2) In the slave parallel mode, these pins serve as the D[7:4] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[8,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1)In the slave parallel X16 and X32 modes, serve as the D[15:8] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
D[16,…,31]_A[0,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the slave parallel X32 mode, serve as the D[31:16] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up

PIN Name	PIN Type	PIN Direction	PIN Description
			state. (3) After the configuration is complete, these pins serve as general pins.
A[16,…,28]	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (2) After the configuration is complete, these pins serve as general pins.
CS_N	Multiplexed	Input	Multi-function configuration pin. For chip select input. Active low. (1) When it is low level, this pin enables the slave parallel mode configuration interface. In the slave parallel configuration mode, the external controller can select the slave parallel bus of the FPGA by controlling this pin. Or this pin connected to the previous FPGA CSO_DOUT pin in the slave parallel configuration chain. (2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
RWSEL	Multiplexed	Input	Multi-function configuration pin. For selecting the read/write input in the slave parallel configuration mode (high for read and low for write). (1) When it is high level, the slave parallel configuration mode reads data from the data bus. (2) When it is low level, the slave parallel configuration mode writes data to the data bus. (3) Read and write can be switched only when CS_N is high level. (4) After the configuration is complete, the pin serves as a general pin. (5) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state.
CSO_DOUT	Multiplexed	Output	Multi-function configuration pin. Needed for cascade. (1) In the master SPI X1 mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2) In the slave serial configuration mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (3) In the slave parallel cascade configuration mode, this pin serves as a chip select signal open-drain output, connects to downstream chip CS_N pin and should be connected to VCCIO via an external pull-up resistor of 330Ω. (4) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state.
VS[0, 1]	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (2)After the configuration is complete, these pins as general pins.
IO_STATUS_C	Multiplexed	Input	Multi-function configuration pin, used for controlling whether the weak pull-up resistors for all general pins are enabled during the configuration process.

PIN Name	PIN Type	PIN Direction	PIN Description
			(1) When it is set to "0", the internal pull-up resistors for all general pins are enabled. (2) When it is set to "1", the internal pull-up resistors for all general pins are disabled. (3)It is recommended that the pin connects to VCCIO via an external weak pull-up resistor. (4)The pin can connect to VCCIO or VSS, either directly or via an external resistor of no more than 1K. (5) This pin must not be left floating before or during configuration.
ECCLKIN	Multiplexed	Input	The external clock input for the Master configuration mode, which is an optional external clock input to the configuration logic. (1) In the master SPI mode, the FPGA can select this clock input as the configuration clock for the configuration logic. This clock can be divided (Depends on the settings in the bitstream) and output from the CFG_CLK pin. (2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state.
BFOE_N	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2)After the configuration is complete, the pin as a general pin.
BFWE_ FCS2_N	Multiplexed	Output	Multi-function configuration pin used for the master SPI X8 configuration modes. (1) In the Master SPI X8 mode, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin as a general pin.
BADRVO_N	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2)After the configuration is complete, the pin as a general pin.
Clock PIN			
GMCLK	Multiplexed	Input	Multiplexing global multi-regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL, PPLL, and also drive the multi-regional clock buffer. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. When these pins serve as single regional clock sources, they are able to drive all the IO clock buffers and regional clock buffers of the BANK.
GSCLK	Multiplexed	Input	Multiplexing global single regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL and PPLL. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. They are able to drive all the IO clock buffers and regional clock buffers of the BANK.

PIN Name	PIN Type	PIN Direction	PIN Description
Memory Interface PIN			
DQS	Multiplexed	Input/Output	DDR DQS PIN, each memory group contains two pins.
Reference PIN			
VREF	Multiplexed	N/A	Input reference voltage pins,. When not used as external reference voltage pins, these pins serve as general pins.
Power/ Ground PIN			
VCC	Dedicated	N/A	Core logic power, 1.0V. Power supply for core logic
VCC_DRM	Dedicated	N/A	DRM power, 1.0V. Dedicated power supply for DRM. If the voltage is the same as VCC, it can be connected to VCC at the board.
VCCA	Dedicated	N/A	Analog power, 1.8V. Power supply for internal analog circuit.
VCCIO[L3, L4, L5, L6, R4, R5, CFG]	Dedicated	N/A	IO BANK power.
VCCB	Dedicated	N/A	Key memory backup battery power supply voltage, 1.0V~1.9V. When the key function is not used, the pin needs to be connected to the VCCA or ground.
VSS	Dedicated	N/A	Ground
ADC PIN			
VCCADC	Dedicated	N/A	ADC analog power, 1.8V. Power supply for ADC analog circuit.
VSSADC	Dedicated	N/A	GND relative to VCCADC
VAADC_P	Dedicated	Input	ADC dedicated analog differential input (Positive).
VAADC_N	Dedicated	Input	ADC dedicated analog differential input (Negative).
VREFADC_P	Dedicated	N/A	1.255V ADC reference voltage pin.
VREFADC_N	Dedicated	N/A	ADC reference voltage ground.
VAA[0,..,15]P,VAA[0,..,15]N	Multiplexed	Input	ADC differential analog input signals.
TSDP	Dedicated	N/A	Positive pin of the temperature sensor diode. When not used temperature diode, the pin needs to be connected to the VSS. When temperature sensor diode is to be used, then appropriate external temperature monitoring chip is required.
TSDN	Dedicated	N/A	Negative pin of the temperature sensor diode.
HSST PIN			
HSSTAVCC_Q[R3 , R6]	Dedicated	N/A	1.0V analog power pin, power supply for HSST internal transmits and receives circuit.
HSSTAVCCPLL_Q[R3 , R6]	Dedicated	N/A	1.2V analog power pin, power supply for HSST internal PLL.
HSSTRREF_Q[R3 , R6]	Dedicated	Input	Calibration resistance input pin of the terminal resistance calibration circuit.
HSSTREFCLK[0,1]P_Q[R3, R6]	Dedicated	Input	Positive end of differential clock input pin, provide a reference clock to HSST.
HSSTREFCLK[0,1]N_Q[R3, R6]	Dedicated	Input	Negative end of differential clock input pin, provide a reference clock to HSST.
HSSTTX[0,1,2,3][P,N]_Q[R3, R6]	Dedicated	Output	Channel differential outputs of HSST. Each HSST has 4 pairs.
HSSTRX[0,1,2,3][P,N]_Q[R3, R6]	Dedicated	Input	Channel differential inputs of HSST. Each HSST has 4 pairs.

2.2.1 Pin Name List

Table 2-3 Pin Name List

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L3	SIO_L3_00	H17		52.6985	
L3	DIFFIO_L3_G0_00P	H14	IO_1_P	87.4086	L3_G0
L3	DIFFIO_L3_G0_00N	H15	IO_1_N	87.1403	L3_G0
L3	DIFFIO_L3_G0_01P	G17	IO_2_P	50.0723	L3_G0
L3	DIFFIO_L3_G0_01N	F17	IO_2_N	48.559	L3_G0
L3	DIFFIO_L3_G0_02P_DQS	F18	IO_3_P	103.798	L3_G0_DQS
L3	DIFFIO_L3_G0_02N_DQS	F19	IO_3_N	94.4035	L3_G0_DQS
L3	DIFFIO_L3_G0_03P	G15	IO_4_P	94.6945	L3_G0
L3	DIFFIO_L3_G0_03N	F15	IO_4_N	92.5069	L3_G0
L3	DIFFIO_L3_G0_04P	G19	IO_5_P	97.4201	L3_G0
L3	DIFFIO_L3_G0_04N	F20	IO_5_N	92.3003	L3_G0
L3	DIFFIO_L3_G0_05P	H16	IO_6_P	118.976	L3_G0
L3	DIFFIO_L3_G0_05N_VREF	G16	IO_6_N	112.212	L3_G0
L3	DIFFIO_L3_G1_06P	C17	IO_7_P	138.124	L3_G1
L3	DIFFIO_L3_G1_06N	B17	IO_7_N	134.117	L3_G1
L3	DIFFIO_L3_G1_07P	E16	IO_8_P	99.6338	L3_G1
L3	DIFFIO_L3_G1_07N	D16	IO_8_N	101.159	L3_G1
L3	DIFFIO_L3_G1_08P_DQS	A17	IO_9_P	154.172	L3_G1_DQS
L3	DIFFIO_L3_G1_08N_DQS	A18	IO_9_N	156.645	L3_G1_DQS
L3	DIFFIO_L3_G1_09P	B19	IO_10_P	128.17	L3_G1
L3	DIFFIO_L3_G1_09N	A19	IO_10_N	132.267	L3_G1
L3	DIFFIO_L3_G1_10P_GSCLK	E17	IO_11_P	158.711	L3_G1
L3	DIFFIO_L3_G1_10N_GSCLK	E18	IO_11_N	155.486	L3_G1
L3	DIFFIO_L3_G1_11P_GMCLK	D18	IO_12_P	104.124	L3_G1
L3	DIFFIO_L3_G1_11N_GMCLK	C18	IO_12_N	106.692	L3_G1
L3	DIFFIO_L3_G2_12P_GMCLK	D19	IO_13_P	148.107	L3_G2
L3	DIFFIO_L3_G2_12N_GMCLK	C19	IO_13_N	152.12	L3_G2
L3	DIFFIO_L3_G2_13P_GSCLK	E20	IO_14_P	100.036	L3_G2
L3	DIFFIO_L3_G2_13N_GSCLK	D20	IO_14_N	102.606	L3_G2
L3	DIFFIO_L3_G2_14P_DQS	B20	IO_15_P	142.263	L3_G2_DQS
L3	DIFFIO_L3_G2_14N_DQS	A20	IO_15_N	153.074	L3_G2_DQS
L3	DIFFIO_L3_G2_15P	C21	IO_16_P	112.631	L3_G2
L3	DIFFIO_L3_G2_15N	B21	IO_16_N	114.126	L3_G2
L3	DIFFIO_L3_G2_16P	B22	IO_17_P	134.934	L3_G2
L3	DIFFIO_L3_G2_16N	A22	IO_17_N	139.706	L3_G2
L3	DIFFIO_L3_G2_17P	E21	IO_18_P	126.012	L3_G2
L3	DIFFIO_L3_G2_17N	D21	IO_18_N	121.101	L3_G2

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L3	DIFFIO_L3_G3_18P	C22	IO_19_P	136.452	L3_G3
L3	DIFFIO_L3_G3_18N_VREF	C23	IO_19_N	133.896	L3_G3
L3	DIFFIO_L3_G3_19P	B25	IO_20_P	166.166	L3_G3
L3	DIFFIO_L3_G3_19N	A25	IO_20_N	171.514	L3_G3
L3	DIFFIO_L3_G3_20P_DQS	A23	IO_21_P	182.95	L3_G3_DQS
L3	DIFFIO_L3_G3_20N_DQS	A24	IO_21_N	183.447	L3_G3_DQS
L3	DIFFIO_L3_G3_21P	C26	IO_22_P	175.751	L3_G3
L3	DIFFIO_L3_G3_21N	B26	IO_22_N	175.785	L3_G3
L3	DIFFIO_L3_G3_22P	C24	IO_23_P	143.841	L3_G3
L3	DIFFIO_L3_G3_22N	B24	IO_23_N	141.815	L3_G3
L3	DIFFIO_L3_G3_23P	D23	IO_24_P	125.381	L3_G3
L3	DIFFIO_L3_G3_23N	D24	IO_24_N	124.697	L3_G3
L3	SIO_L3_01	E22		126.044	
L4	SIO_L4_00	K18		39.6354	
L4	DIFFIO_L4_G0_00P_VAA1P	K15	IO_25_P	140.021	L4_G0
L4	DIFFIO_L4_G0_00N_VAA1N	J16	IO_25_N	135.572	L4_G0
L4	DIFFIO_L4_G0_01P_VAA2P	J14	IO_26_P	123.128	L4_G0
L4	DIFFIO_L4_G0_01N_VAA2N	J15	IO_26_N	122.707	L4_G0
L4	DIFFIO_L4_G0_02P_DQS_VAA3P	K16	IO_27_P	116.236	L4_G0_DQS
L4	DIFFIO_L4_G0_02N_DQS_VAA3N	K17	IO_27_N	113.602	L4_G0_DQS
L4	DIFFIO_L4_G0_03P	M14	IO_28_P	114.408	L4_G0
L4	DIFFIO_L4_G0_03N	L14	IO_28_N	106.468	L4_G0
L4	DIFFIO_L4_G0_04P_VAA5P	M15	IO_29_P	127.656	L4_G0
L4	DIFFIO_L4_G0_04N_VAA5N	L15	IO_29_N	119.814	L4_G0
L4	DIFFIO_L4_G0_05P	M16	IO_30_P	85.3678	L4_G0
L4	DIFFIO_L4_G0_05N_VREF	M17	IO_30_N	84.687	L4_G0
L4	DIFFIO_L4_G1_06P_VAA7P	J19	IO_31_P	132.426	L4_G1
L4	DIFFIO_L4_G1_06N_VAA7N	H19	IO_31_N	121.276	L4_G1
L4	DIFFIO_L4_G1_07P_VAA8P	L17	IO_32_P	84.3231	L4_G1
L4	DIFFIO_L4_G1_07N_VAA8N	L18	IO_32_N	86.0156	L4_G1
L4	DIFFIO_L4_G1_08P_DQS_VAA9P	K20	IO_33_P	125.293	L4_G1_DQS
L4	DIFFIO_L4_G1_08N_DQS_VAA9N	J20	IO_33_N	126.198	L4_G1_DQS
L4	DIFFIO_L4_G1_09P_VAA10P	J18	IO_34_P	144.772	L4_G1
L4	DIFFIO_L4_G1_09N_VAA10N	H18	IO_34_N	147.22	L4_G1
L4	DIFFIO_L4_G1_10P_GSCLK	G20	IO_35_P	140.322	L4_G1
L4	DIFFIO_L4_G1_10N_GSCLK	G21	IO_35_N	138.353	L4_G1
L4	DIFFIO_L4_G1_11P_GMCLK	K21	IO_36_P	94.5133	L4_G1
L4	DIFFIO_L4_G1_11N_GMCLK	J21	IO_36_N	91.2378	L4_G1

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L4	DIFFIO_L4_G2_ 12P_GMCLK	H21	IO_37_P	128.762	L4_G2
L4	DIFFIO_L4_G2_ 12N_GMCLK	H22	IO_37_N	123.057	L4_G2
L4	DIFFIO_L4_G2_ 13P_GSCLK	J23	IO_38_P	96.787	L4_G2
L4	DIFFIO_L4_G2_ 13N_GSCLK	H23	IO_38_N	103.2	L4_G2
L4	DIFFIO_L4_G2_ 14P_DQS	G22	IO_39_P	142.678	L4_G2_DQS
L4	DIFFIO_L4_G2_ 14N_DQS_BADRVO_N	F22	IO_39_N	151.199	L4_G2_DQS
L4	DIFFIO_L4_G2_ 15P_A28	J24	IO_40_P	129.219	L4_G2
L4	DIFFIO_L4_G2_ 15N_A27	H24	IO_40_N	119.507	L4_G2
L4	DIFFIO_L4_G2_ 16P_A26	F23	IO_41_P	154.202	L4_G2
L4	DIFFIO_L4_G2_ 16N_A25	E23	IO_41_N	160.685	L4_G2
L4	DIFFIO_L4_G2_ 17P_A24	K22	IO_42_P	93.5236	L4_G2
L4	DIFFIO_L4_G2_ 17N_A23	K23	IO_42_N	100.206	L4_G2
L4	DIFFIO_L4_G3_ 18P_A22	G24	IO_43_P	142.637	L4_G3
L4	DIFFIO_L4_G3_ 18N_VREF_A21	F24	IO_43_N	140.639	L4_G3
L4	DIFFIO_L4_G3_ 19P_A20	E25	IO_44_P	165.617	L4_G3
L4	DIFFIO_L4_G3_ 19N_A19	D25	IO_44_N	170.517	L4_G3
L4	DIFFIO_L4_G3_20P_DQS	E26	IO_45_P	165.915	L4_G3_DQS
L4	DIFFIO_L4_G3_20N_DQS_A18	D26	IO_45_N	178.053	L4_G3_DQS
L4	DIFFIO_L4_G3_21P_A17	H26	IO_46_P	155.264	L4_G3
L4	DIFFIO_L4_G3_21N_A16	G26	IO_46_N	148.073	L4_G3
L4	DIFFIO_L4_G3_22P_BFOE_N	G25	IO_47_P	145.98	L4_G3
L4	DIFFIO_L4_G3_22N_BFWE_FCS2_N	F25	IO_47_N	142.796	L4_G3
L4	DIFFIO_L4_G3_23P_VS1	J25	IO_48_P	127.512	L4_G3
L4	DIFFIO_L4_G3_23N_VS0	J26	IO_48_N	124.158	L4_G3
L4	SIO_L4_01	L19		67.7555	
L5	SIO_L5_00	M19		47.7229	
L5	DIFFIO_L5_G0_00P_MOSI_D0	R14	IO_49_P	156.218	L5_G0
L5	DIFFIO_L5_G0_00N_MISO_D1_DI	R15	IO_49_N	157.899	L5_G0
L5	DIFFIO_L5_G0_01P_D2	P14	IO_50_P	115.245	L5_G0
L5	DIFFIO_L5_G0_01N_D3	N14	IO_50_N	117.308	L5_G0
L5	DIFFIO_L5_G0_02P_DQS_IO_STATUS_C	P15	IO_51_P	148.282	L5_G0_DQS
L5	DIFFIO_L5_G0_02N_DQS_ECCLKIN	P16	IO_51_N	152.803	L5_G0_DQS
L5	DIFFIO_L5_G0_03P_D4	N16	IO_52_P	92.9069	L5_G0
L5	DIFFIO_L5_G0_03N_D5	N17	IO_52_N	93.6141	L5_G0
L5	DIFFIO_L5_G0_04P_D6	R16	IO_53_P	151.995	L5_G0
L5	DIFFIO_L5_G0_04N_D7	R17	IO_53_N	157.099	L5_G0
L5	DIFFIO_L5_G0_05P_FCS_N	P18	IO_54_P	82.2825	L5_G0
L5	DIFFIO_L5_G0_05N_VREF_D8	N18	IO_54_N	81.4269	L5_G0

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L5	DIFFIO_L5_G1_06P_D9	K25	IO_55_P	123.773	L5_G1
L5	DIFFIO_L5_G1_06N_D10	K26	IO_55_N	131.126	L5_G1
L5	DIFFIO_L5_G1_07P_D11	M20	IO_56_P	84.8704	L5_G1
L5	DIFFIO_L5_G1_07N_D12	L20	IO_56_N	101.74	L5_G1
L5	DIFFIO_L5_G1_08P_DQS_N	L24	IO_57_P	107.452	L5_G1_DQS
L5	DIFFIO_L5_G1_08N_DQS_D13	L25	IO_57_N	107.78	L5_G1_DQS
L5	DIFFIO_L5_G1_09P_D14	M24	IO_58_P	96.4851	L5_G1
L5	DIFFIO_L5_G1_09N_D15	M25	IO_58_N	103.687	L5_G1
L5	DIFFIO_L5_G1_10P_GSCLK	L22	IO_59_P	131.126	L5_G1
L5	DIFFIO_L5_G1_ 10N_GSCLK	L23	IO_59_N	129.222	L5_G1
L5	DIFFIO_L5_G1_ 11P_GMCLK	M21	IO_60_P	101.981	L5_G1
L5	DIFFIO_L5_G1_ 11N_GMCLK	M22	IO_60_N	103.63	L5_G1
L5	DIFFIO_L5_G2_ 12P_GMCLK	N21	IO_61_P	135.462	L5_G2
L5	DIFFIO_L5_G2_ 12N_GMCLK	N22	IO_61_N	130.987	L5_G2
L5	DIFFIO_L5_G2_13P_GSCLK	P20	IO_62_P	72.4165	L5_G2
L5	DIFFIO_L5_G2_ 13N_GSCLK	P21	IO_62_N	71.4694	L5_G2
L5	DIFFIO_L5_G2_ 14P_DQS_RWSEL	N23	IO_63_P	103.978	L5_G2_DQS
L5	DIFFIO_L5_G2_ 14N_DQS_CSO_DOUT	N24	IO_63_N	107.911	L5_G2_DQS
L5	DIFFIO_L5_G2_ 15P_CS_N	P19	IO_64_P	85.1348	L5_G2
L5	DIFFIO_L5_G2_15N_D31_A15	N19	IO_64_N	86.3187	L5_G2
L5	DIFFIO_L5_G2_16P_D30_A14	P23	IO_65_P	99.7743	L5_G2
L5	DIFFIO_L5_G2_16N_D29_A13	P24	IO_65_N	95.9185	L5_G2
L5	DIFFIO_L5_G2_17P_D28_A12	R20	IO_66_P	67.7728	L5_G2
L5	DIFFIO_L5_G2_17N_D27_A11	R21	IO_66_N	67.0141	L5_G2
L5	DIFFIO_L5_G3_18P_D26_A10	R25	IO_67_P	112.04	L5_G3
L5	DIFFIO_L5_G3_ 18N_VREF_D25_A9	P25	IO_67_N	117.105	L5_G3
L5	DIFFIO_L5_G3_19P_D24_A8	N26	IO_68_P	126.076	L5_G3
L5	DIFFIO_L5_G3_ 19N_D23_A7	M26	IO_68_N	133.517	L5_G3
L5	DIFFIO_L5_G3_20P_DQS	T24	IO_69_P	102.021	L5_G3_DQS
L5	DIFFIO_L5_G3_20N_DQS_D22_ A6	T25	IO_69_N	104.006	L5_G3_DQS
L5	DIFFIO_L5_G3_21P_D21_A5	R26	IO_70_P	123.749	L5_G3
L5	DIFFIO_L5_G3_21N_D20_A4	P26	IO_70_N	132.548	L5_G3
L5	DIFFIO_L5_G3_22P_D19_A3	T22	IO_71_P	123.93	L5_G3
L5	DIFFIO_L5_G3_22N_D18_A2	R22	IO_71_N	129.664	L5_G3
L5	DIFFIO_L5_G3_23P_D17_A1	T23	IO_72_P	124.984	L5_G3
L5	DIFFIO_L5_G3_23N_D16_A0	R23	IO_72_N	120.974	L5_G3
L5	SIO_L5_01	R18		49.9747	
L6	SIO_L6_00	U24		86.5192	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L6	DIFFIO_L6_G0_00P	U25	IO_73_P	106.46	L6_G0
L6	DIFFIO_L6_G0_00N	U26	IO_73_N	109.858	L6_G0
L6	DIFFIO_L6_G0_01P	V26	IO_74_P	119.683	L6_G0
L6	DIFFIO_L6_G0_01N	W26	IO_74_N	119.259	L6_G0
L6	DIFFIO_L6_G0_02P_DQS	AB26	IO_75_P	143.853	L6_G0_DQS
L6	DIFFIO_L6_G0_02N_DQS	AC26	IO_75_N	144.457	L6_G0_DQS
L6	DIFFIO_L6_G0_03P	W25	IO_76_P	116.072	L6_G0
L6	DIFFIO_L6_G0_03N	Y26	IO_76_N	117.844	L6_G0
L6	DIFFIO_L6_G0_04P	Y25	IO_77_P	113.888	L6_G0
L6	DIFFIO_L6_G0_04N	AA25	IO_77_N	115.663	L6_G0
L6	DIFFIO_L6_G0_05P	V24	IO_78_P	108.765	L6_G0
L6	DIFFIO_L6_G0_05N_VREF	W24	IO_78_N	106.59	L6_G0
L6	DIFFIO_L6_G1_06P	AA24	IO_79_P	121.538	L6_G1
L6	DIFFIO_L6_G1_06N	AB25	IO_79_N	120.842	L6_G1
L6	DIFFIO_L6_G1_07P	AA22	IO_80_P	125.563	L6_G1
L6	DIFFIO_L6_G1_07N	AA23	IO_80_N	122.992	L6_G1
L6	DIFFIO_L6_G1_08P_DQS	AB24	IO_81_P	110.054	L6_G1_DQS
L6	DIFFIO_L6_G1_08N_DQS	AC24	IO_81_N	109.749	L6_G1_DQS
L6	DIFFIO_L6_G1_09P	V23	IO_82_P	88.9402	L6_G1
L6	DIFFIO_L6_G1_09N	W23	IO_82_N	87.3967	L6_G1
L6	DIFFIO_L6_G1_10P_GSCLK	Y22	IO_83_P	87.1056	L6_G1
L6	DIFFIO_L6_G1_ 10N_GSCLK	Y23	IO_83_N	90.2616	L6_G1
L6	DIFFIO_L6_G1_ 11P_GMCLK	U22	IO_84_P	96.7315	L6_G1
L6	DIFFIO_L6_G1_ 11N_GMCLK	V22	IO_84_N	95.1447	L6_G1
L6	DIFFIO_L6_G2_ 12P_GMCLK	U21	IO_85_P	107.285	L6_G2
L6	DIFFIO_L6_G2_ 12N_GMCLK	V21	IO_85_N	103.693	L6_G2
L6	DIFFIO_L6_G2_13P_GSCLK	W21	IO_86_P	73.6629	L6_G2
L6	DIFFIO_L6_G2_ 13N_GSCLK	Y21	IO_86_N	73.5298	L6_G2
L6	DIFFIO_L6_G2_ 14P_DQS	T20	IO_87_P	163.185	L6_G2_DQS
L6	DIFFIO_L6_G2_ 14N_DQS	U20	IO_87_N	160.298	L6_G2_DQS
L6	DIFFIO_L6_G2_ 15P	W20	IO_88_P	60.1669	L6_G2
L6	DIFFIO_L6_G2_ 15N	Y20	IO_88_N	60.7123	L6_G2
L6	DIFFIO_L6_G2_ 16P	T19	IO_89_P	161.724	L6_G2
L6	DIFFIO_L6_G2_ 16N	U19	IO_89_N	159.094	L6_G2
L6	DIFFIO_L6_G2_ 17P	V19	IO_90_P	62.6159	L6_G2
L6	DIFFIO_L6_G2_ 17N	W19	IO_90_N	60.2878	L6_G2
L6	DIFFIO_L6_G3_ 18P	V18	IO_91_P	122.367	L6_G3
L6	DIFFIO_L6_G3_ 18N_VREF	W18	IO_91_N	123.7	L6_G3
L6	DIFFIO_L6_G3_ 19P	T14	IO_92_P	120.178	L6_G3
L6	DIFFIO_L6_G3_ 19N	T15	IO_92_N	119.955	L6_G3

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L6	DIFFIO_L6_G3_20P_DQS	T17	IO_93_P	148.478	L6_G3_DQS
L6	DIFFIO_L6_G3_20N_DQS	T18	IO_93_N	145.728	L6_G3_DQS
L6	DIFFIO_L6_G3_21P	U15	IO_94_P	107.13	L6_G3
L6	DIFFIO_L6_G3_21N	U16	IO_94_N	104.433	L6_G3
L6	DIFFIO_L6_G3_22P	U14	IO_95_P	97.4643	L6_G3
L6	DIFFIO_L6_G3_22N	V14	IO_95_N	95.9062	L6_G3
L6	DIFFIO_L6_G3_23P	V16	IO_96_P	83.4537	L6_G3
L6	DIFFIO_L6_G3_23N	V17	IO_96_N	85.7451	L6_G3
L6	SIO_L6_01	U17		91.4976	
R4	SIO_R4_00	J8		69.3679	
R4	DIFFIO_R4_G0_00P_VAA4P	E6	IO_97_P	111.56	R4_G0
R4	DIFFIO_R4_G0_00N_VAA4N	D6	IO_97_N	114.509	R4_G0
R4	DIFFIO_R4_G0_01P_VAA6P	H8	IO_98_P	98.2965	R4_G0
R4	DIFFIO_R4_G0_01N_VAA6N	G8	IO_98_N	98.514	R4_G0
R4	DIFFIO_R4_G0_02P_DQS_VAA11P	H7	IO_99_P	113.862	R4_G0_DQS
R4	DIFFIO_R4_G0_02N_DQS_VAA11N	G7	IO_99_N	110.936	R4_G0_DQS
R4	DIFFIO_R4_G0_03P	F8	IO_100_P	105.977	R4_G0
R4	DIFFIO_R4_G0_03N	F7	IO_100_N	120.427	R4_G0
R4	DIFFIO_R4_G0_04P_VAA12P	H6	IO_101_P	103.306	R4_G0
R4	DIFFIO_R4_G0_04N_VAA12N	G6	IO_101_N	99.4996	R4_G0
R4	DIFFIO_R4_G0_05P	H9	IO_102_P	102.405	R4_G0
R4	DIFFIO_R4_G0_05N_VREF	G9	IO_102_N	103.08	R4_G0
R4	DIFFIO_R4_G1_06P_VAA13P	J6	IO_103_P	111.193	R4_G1
R4	DIFFIO_R4_G1_06N_VAA13N	J5	IO_103_N	110.83	R4_G1
R4	DIFFIO_R4_G1_07P_VAA14P	L8	IO_104_P	74.4481	R4_G1
R4	DIFFIO_R4_G1_07N_VAA14N	K8	IO_104_N	77.6664	R4_G1
R4	DIFFIO_R4_G1_08P_DQS_VAA15P	J4	IO_105_P	90.583	R4_G1_DQS
R4	DIFFIO_R4_G1_08N_DQS_VAA15N	H4	IO_105_N	95.7463	R4_G1_DQS
R4	DIFFIO_R4_G1_09P_VAA0P	K7	IO_106_P	72.2844	R4_G1
R4	DIFFIO_R4_G1_09N_VAA0N	K6	IO_106_N	71.2857	R4_G1
R4	DIFFIO_R4_G1_ 10P_GSCLK	G4	IO_107_P	117.361	R4_G1
R4	DIFFIO_R4_G1_ 10N_GSCLK	F4	IO_107_N	122.821	R4_G1
R4	DIFFIO_R4_G1_ 11P_GMCLK	G5	IO_108_P	133.889	R4_G1
R4	DIFFIO_R4_G1_ 11N_GMCLK	F5	IO_108_N	134.948	R4_G1
R4	DIFFIO_R4_G2_ 12P_GMCLK	E5	IO_109_P	147.019	R4_G2
R4	DIFFIO_R4_G2_ 12N_GMCLK	D5	IO_109_N	151.3	R4_G2
R4	DIFFIO_R4_G2_ 13P_GSCLK	D4	IO_110_P	150.775	R4_G2
R4	DIFFIO_R4_G2_ 13N_GSCLK	C4	IO_110_N	163.715	R4_G2

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R4	DIFFIO_R4_G2_ 14P_DQS	B5	IO_ 111_P	173.814	R4_G2_DQS
R4	DIFFIO_R4_G2_ 14N_DQS	A5	IO_ 111_N	177.622	R4_G2_DQS
R4	DIFFIO_R4_G2_ 15P	B4	IO_ 112_P	180.531	R4_G2
R4	DIFFIO_R4_G2_ 15N	A4	IO_ 112_N	183.887	R4_G2
R4	DIFFIO_R4_G2_ 16P	D3	IO_ 113_P	159.297	R4_G2
R4	DIFFIO_R4_G2_ 16N	C3	IO_ 113_N	165.085	R4_G2
R4	DIFFIO_R4_G2_ 17P	F3	IO_ 114_P	151.362	R4_G2
R4	DIFFIO_R4_G2_ 17N	E3	IO_ 114_N	150.977	R4_G2
R4	DIFFIO_R4_G3_ 18P	C2	IO_ 115_P	177.886	R4_G3
R4	DIFFIO_R4_G3_ 18N_VREF	B2	IO_ 115_N	181.286	R4_G3
R4	DIFFIO_R4_G3_ 19P	A3	IO_ 116_P	184.818	R4_G3
R4	DIFFIO_R4_G3_ 19N	A2	IO_ 116_N	201.696	R4_G3
R4	DIFFIO_R4_G3_20P_DQS	C1	IO_ 117_P	179.179	R4_G3_DQS
R4	DIFFIO_R4_G3_20N_DQS	B1	IO_ 117_N	183.611	R4_G3_DQS
R4	DIFFIO_R4_G3_21P	F2	IO_ 118_P	160.634	R4_G3
R4	DIFFIO_R4_G3_21N	E2	IO_ 118_N	161.185	R4_G3
R4	DIFFIO_R4_G3_22P	E1	IO_ 119_P	169.039	R4_G3
R4	DIFFIO_R4_G3_22N	D1	IO_ 119_N	176.531	R4_G3
R4	DIFFIO_R4_G3_23P	G2	IO_ 120_P	144.617	R4_G3
R4	DIFFIO_R4_G3_23N	G1	IO_ 120_N	144.758	R4_G3
R4	SIO_R4_01	H3		119.517	
R5	SIO_R5_00	N8		42.4783	
R5	DIFFIO_R5_G0_00P	K3	IO_ 121_P	136.711	R5_G0
R5	DIFFIO_R5_G0_00N	J3	IO_ 121_N	136.235	R5_G0
R5	DIFFIO_R5_G0_01P	M7	IO_ 122_P	69.8166	R5_G0
R5	DIFFIO_R5_G0_01N	L7	IO_ 122_N	74.2198	R5_G0
R5	DIFFIO_R5_G0_02P_DQS	M4	IO_ 123_P	106.648	R5_G0_DQS
R5	DIFFIO_R5_G0_02N_DQS	L4	IO_ 123_N	112.938	R5_G0_DQS
R5	DIFFIO_R5_G0_03P	L5	IO_ 124_P	95.7912	R5_G0
R5	DIFFIO_R5_G0_03N	K5	IO_ 124_N	102.345	R5_G0
R5	DIFFIO_R5_G0_04P	N7	IO_ 125_P	83.4562	R5_G0
R5	DIFFIO_R5_G0_04N	N6	IO_ 125_N	87.1749	R5_G0
R5	DIFFIO_R5_G0_05P	M6	IO_ 126_P	88.8085	R5_G0
R5	DIFFIO_R5_G0_05N_VREF	M5	IO_ 126_N	85.8427	R5_G0
R5	DIFFIO_R5_G1_06P	K1	IO_ 127_P	135.926	R5_G1
R5	DIFFIO_R5_G1_06N	J1	IO_ 127_N	134.919	R5_G1
R5	DIFFIO_R5_G1_07P	L3	IO_ 128_P	125.983	R5_G1
R5	DIFFIO_R5_G1_07N	K2	IO_ 128_N	126.526	R5_G1
R5	DIFFIO_R5_G1_08P_DQS	N1	IO_ 129_P	125.538	R5_G1_DQS
R5	DIFFIO_R5_G1_08N_DQS	M1	IO_ 129_N	122.671	R5_G1_DQS

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R5	DIFFIO_R5_G1_09P	H2	IO_130_P	150.403	R5_G1
R5	DIFFIO_R5_G1_09N	H1	IO_130_N	165.459	R5_G1
R5	DIFFIO_R5_G1_ 10P_GSCLK	M2	IO_131_P	127.5	R5_G1
R5	DIFFIO_R5_G1_ 10N_GSCLK	L2	IO_131_N	132.002	R5_G1
R5	DIFFIO_R5_G1_ 11P_GMCLK	N3	IO_132_P	110.658	R5_G1
R5	DIFFIO_R5_G1_ 11N_GMCLK	N2	IO_132_N	117.042	R5_G1
R5	DIFFIO_R5_G2_ 12P_GMCLK	R3	IO_133_P	96.8255	R5_G2
R5	DIFFIO_R5_G2_ 12N_GMCLK	P3	IO_133_N	94.8453	R5_G2
R5	DIFFIO_R5_G2_ 13P_GSCLK	P4	IO_134_P	104.582	R5_G2
R5	DIFFIO_R5_G2_ 13N_GSCLK	N4	IO_134_N	110.227	R5_G2
R5	DIFFIO_R5_G2_ 14P_DQS	R1	IO_135_P	117.651	R5_G2_DQS
R5	DIFFIO_R5_G2_ 14N_DQS	P1	IO_135_N	118.355	R5_G2_DQS
R5	DIFFIO_R5_G2_ 15P	T4	IO_136_P	92.7117	R5_G2
R5	DIFFIO_R5_G2_ 15N	T3	IO_136_N	90.6386	R5_G2
R5	DIFFIO_R5_G2_ 16P	T2	IO_137_P	109.517	R5_G2
R5	DIFFIO_R5_G2_ 16N	R2	IO_137_N	97.9471	R5_G2
R5	DIFFIO_R5_G2_ 17P	U2	IO_138_P	116.784	R5_G2
R5	DIFFIO_R5_G2_ 17N	U1	IO_138_N	116.977	R5_G2
R5	DIFFIO_R5_G3_ 18P	P6	IO_139_P	120.168	R5_G3
R5	DIFFIO_R5_G3_ 18N_VREF	P5	IO_139_N	127.667	R5_G3
R5	DIFFIO_R5_G3_ 19P	T5	IO_140_P	89.7103	R5_G3
R5	DIFFIO_R5_G3_ 19N	R5	IO_140_N	90.5703	R5_G3
R5	DIFFIO_R5_G3_20P_DQS	U6	IO_141_P	88.6572	R5_G3_DQS
R5	DIFFIO_R5_G3_20N_DQS	U5	IO_141_N	85.945	R5_G3_DQS
R5	DIFFIO_R5_G3_21P	R8	IO_142_P	78.3254	R5_G3
R5	DIFFIO_R5_G3_21N	P8	IO_142_N	77.347	R5_G3
R5	DIFFIO_R5_G3_22P	R7	IO_143_P	116.232	R5_G3
R5	DIFFIO_R5_G3_22N	R6	IO_143_N	115.816	R5_G3
R5	DIFFIO_R5_G3_23P	T8	IO_144_P	58.8664	R5_G3
R5	DIFFIO_R5_G3_23N	T7	IO_144_N	64.9885	R5_G3
R5	SIO_R5_01	U4		77.4033	
	HSSTREFCLK0N_QR3	E13	IO_145_N	104.183	
	HSSTREFCLK0P_QR3	F13	IO_145_P	106.875	
	HSSTREFCLK0N_QR6	AB11	IO_146_N	81.0902	
	HSSTREFCLK0P_QR6	AA11	IO_146_P	71.1694	
	HSSTREFCLK1N_QR3	E11	IO_147_N	82.3449	
	HSSTREFCLK1P_QR3	F11	IO_147_P	86.4402	
	HSSTREFCLK1N_QR6	AB13	IO_148_N	105.23	
	HSSTREFCLK1P_QR6	AA13	IO_148_P	101.018	
	HSSTRX0N_QR3	C12	IO_149_N	76.681	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	HSSTRX0P_QR3	D12	IO_149_P	80.3249	
	HSSTRX0N_QR6	AF11	IO_150_N	97.0534	
	HSSTRX0P_QR6	AE11	IO_150_P	98.7391	
	HSSTRX1N_QR3	A13	IO_151_N	97.7642	
	HSSTRX1P_QR3	B13	IO_151_P	98.2849	
	HSSTRX1N_QR6	AD14	IO_152_N	102.555	
	HSSTRX1P_QR6	AC14	IO_152_P	103.941	
	HSSTRX2N_QR3	C14	IO_153_N	100.902	
	HSSTRX2P_QR3	D14	IO_153_P	100.675	
	HSSTRX2N_QR6	AF13	IO_154_N	106.913	
	HSSTRX2P_QR6	AE13	IO_154_P	107.684	
	HSSTRX3N_QR3	A11	IO_155_N	97.3944	
	HSSTRX3P_QR3	B11	IO_155_P	96.845	
	HSSTRX3N_QR6	AD12	IO_156_N	84.7545	
	HSSTRX3P_QR6	AC12	IO_156_P	84.7457	
	HSSTTX0N_QR3	C10	IO_157_N	91.4607	
	HSSTTX0P_QR3	D10	IO_157_P	91.1702	
	HSSTTX0N_QR6	AF7	IO_158_N	117.152	
	HSSTTX0P_QR6	AE7	IO_158_P	117.734	
	HSSTTX1N_QR3	A9	IO_159_N	110.435	
	HSSTTX1P_QR3	B9	IO_159_P	109.722	
	HSSTTX1N_QR6	AD8	IO_160_N	95.8421	
	HSSTTX1P_QR6	AC8	IO_160_P	96.8362	
	HSSTTX2N_QR3	C8	IO_161_N	97.917	
	HSSTTX2P_QR3	D8	IO_161_P	97.2994	
	HSSTTX2N_QR6	AF9	IO_162_N	108.362	
	HSSTTX2P_QR6	AE9	IO_162_P	109.3	
	HSSTTX3N_QR3	A7	IO_163_N	119.566	
	HSSTTX3P_QR3	B7	IO_163_P	117.978	
	HSSTTX3N_QR6	AD10	IO_164_N	93.1679	
	HSSTTX3P_QR6	AC10	IO_164_P	93.5698	
	HSSTRREF_QR3	A15		140.254	
	HSSTRREF_QR6	AF15		139.201	
	TSDN	R11	IO_165_N	101.113	
	TSDP	R12	IO_165_P	101.392	
	VAADC_N	P11	IO_166_N	98.4142	
	VAADC_P	N12	IO_166_P	92.4892	
	VREFADC_N	N11	IO_167_N	98.4643	
	VREFADC_P	P12	IO_167_P	99.9586	
	CFG_CLK	H13		36.0088	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	CFG_DONE	W10		65.6999	
	INIT_FLAG_N	V11		61.1675	
	MODE_0	AB7		122.373	
	MODE_1	Y9		101.852	
	MODE_2	W9		102.145	
	RSTN	AE16		87.2256	
	SCBV	AB15		65.8023	
	TCK	H12		81.0687	
	TDI	H10		86.1601	
	TDO	J10		67.5321	
	TMS	H11		76.9366	
	HSSTAVCC_QR3	D9			
	HSSTAVCC_QR3	D11			
	HSSTAVCC_QR3	D13			
	HSSTAVCC_QR3	F10			
	HSSTAVCC_QR3	F12			
	HSSTAVCC_QR6	AA10			
	HSSTAVCC_QR6	AA12			
	HSSTAVCC_QR6	AC9			
	HSSTAVCC_QR6	AC11			
	HSSTAVCC_QR6	AC13			
	HSSTAVCCPLL_QR3	B8			
	HSSTAVCCPLL_QR3	B10			
	HSSTAVCCPLL_QR3	B12			
	HSSTAVCCPLL_QR3	B14			
	HSSTAVCCPLL_QR3	C7			
	HSSTAVCCPLL_QR3	C15			
	HSSTAVCCPLL_QR6	AD7			
	HSSTAVCCPLL_QR6	AD15			
	HSSTAVCCPLL_QR6	AE8			
	HSSTAVCCPLL_QR6	AE10			
	HSSTAVCCPLL_QR6	AE12			
	HSSTAVCCPLL_QR6	AE14			
	VCC	J11			
	VCC	J13			
	VCC	K10			
	VCC	K12			
	VCC	L11			
	VCC	L13			
	VCC	M10			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCC	P10			
	VCC	T10			
	VCC	T12			
	VCC	U11			
	VCC	V10			
	VCC	V12			
	VCC_DRM	N13			
	VCC_DRM	R13			
	VCC_DRM	U13			
	VCC_DRM	W13			
	VCCA	J9			
	VCCA	L9			
	VCCA	N9			
	VCCA	R9			
	VCCA	U9			
	VCCADC	M12			
	VCCB	G14			
	VCCIO_CFG	W11			
	VCCIO_CFG	Y14			
	VCCIO_L3	A21			
	VCCIO_L3	B18			
	VCCIO_L3	C25			
	VCCIO_L3	D22			
	VCCIO_L3	E19			
	VCCIO_L3	F16			
	VCCIO_L4	F26			
	VCCIO_L4	G23			
	VCCIO_L4	H20			
	VCCIO_L4	J17			
	VCCIO_L4	K14			
	VCCIO_L4	M18			
	VCCIO_L5	K24			
	VCCIO_L5	L21			
	VCCIO_L5	N15			
	VCCIO_L5	N25			
	VCCIO_L5	P22			
	VCCIO_L5	R19			
	VCCIO_L6	T16			
	VCCIO_L6	T26			
	VCCIO_L6	U23			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCCIO_L6	V20			
	VCCIO_L6	Y24			
	VCCIO_L6	AC25			
	VCCIO_R4	A1			
	VCCIO_R4	C5			
	VCCIO_R4	D2			
	VCCIO_R4	F6			
	VCCIO_R4	G3			
	VCCIO_R4	J7			
	VCCIO_R5	K4			
	VCCIO_R5	L1			
	VCCIO_R5	M8			
	VCCIO_R5	N5			
	VCCIO_R5	P2			
	VCCIO_R5	T6			
	VSSADC	M11			
	VSS	A6			
	VSS	A8			
	VSS	A10			
	VSS	A12			
	VSS	A14			
	VSS	A16			
	VSS	A26			
	VSS	B3			
	VSS	B6			
	VSS	B15			
	VSS	B16			
	VSS	B23			
	VSS	C6			
	VSS	C9			
	VSS	C11			
	VSS	C13			
	VSS	C16			
	VSS	C20			
	VSS	D7			
	VSS	D15			
	VSS	D17			
	VSS	E4			
	VSS	E7			
	VSS	E8			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	E9			
	VSS	E10			
	VSS	E12			
	VSS	E14			
	VSS	E15			
	VSS	E24			
	VSS	F1			
	VSS	F9			
	VSS	F14			
	VSS	F21			
	VSS	G10			
	VSS	G11			
	VSS	G12			
	VSS	G13			
	VSS	G18			
	VSS	H5			
	VSS	H25			
	VSS	J2			
	VSS	J12			
	VSS	J22			
	VSS	K9			
	VSS	K11			
	VSS	K13			
	VSS	K19			
	VSS	L6			
	VSS	L10			
	VSS	L12			
	VSS	L16			
	VSS	L26			
	VSS	M3			
	VSS	M9			
	VSS	M13			
	VSS	M23			
	VSS	N10			
	VSS	N20			
	VSS	P7			
	VSS	P9			
	VSS	P13			
	VSS	P17			
	VSS	R4			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	R10			
	VSS	R24			
	VSS	T1			
	VSS	T9			
	VSS	T11			
	VSS	T13			
	VSS	T21			
	VSS	U8			
	VSS	U10			
	VSS	U12			
	VSS	U18			
	VSS	V5			
	VSS	V13			
	VSS	V15			
	VSS	V25			
	VSS	W2			
	VSS	W12			
	VSS	W22			
	VSS	Y10			
	VSS	Y11			
	VSS	Y12			
	VSS	Y13			
	VSS	Y19			
	VSS	AA6			
	VSS	AA9			
	VSS	AA14			
	VSS	AA16			
	VSS	AA26			
	VSS	AB3			
	VSS	AB8			
	VSS	AB9			
	VSS	AB10			
	VSS	AB12			
	VSS	AB14			
	VSS	AB23			
	VSS	AC7			
	VSS	AC15			
	VSS	AC20			
	VSS	AD6			
	VSS	AD9			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	AD11			
	VSS	AD13			
	VSS	AD16			
	VSS	AE4			
	VSS	AE6			
	VSS	AE15			
	VSS	AE24			
	VSS	AF1			
	VSS	AF6			
	VSS	AF8			
	VSS	AF10			
	VSS	AF12			
	VSS	AF14			
	VSS	AF16			
	VSS	AF21			
	NC1	AE17			
	NC2	AF18			
	NC	U3			
	NC	U7			
	NC	V1			
	NC	V2			
	NC	V3			
	NC	V4			
	NC	V6			
	NC	V7			
	NC	V8			
	NC	V9			
	NC	W1			
	NC	W3			
	NC	W4			
	NC	W5			
	NC	W6			
	NC	W7			
	NC	W8			
	NC	W14			
	NC	W15			
	NC	W16			
	NC	W17			
	NC	Y1			
	NC	Y2			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	NC	Y3			
	NC	Y4			
	NC	Y5			
	NC	Y6			
	NC	Y7			
	NC	Y8			
	NC	Y15			
	NC	Y16			
	NC	Y17			
	NC	Y18			
	NC	AA1			
	NC	AA2			
	NC	AA3			
	NC	AA4			
	NC	AA5			
	NC	AA7			
	NC	AA8			
	NC	AA15			
	NC	AA17			
	NC	AA18			
	NC	AA19			
	NC	AA20			
	NC	AA21			
	NC	AB1			
	NC	AB2			
	NC	AB4			
	NC	AB5			
	NC	AB6			
	NC	AB16			
	NC	AB17			
	NC	AB18			
	NC	AB19			
	NC	AB20			
	NC	AB21			
	NC	AB22			
	NC	AC1			
	NC	AC2			
	NC	AC3			
	NC	AC4			
	NC	AC5			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	NC	AC6			
	NC	AC16			
	NC	AC17			
	NC	AC18			
	NC	AC19			
	NC	AC21			
	NC	AC22			
	NC	AC23			
	NC	AD1			
	NC	AD2			
	NC	AD3			
	NC	AD4			
	NC	AD5			
	NC	AD17			
	NC	AD18			
	NC	AD19			
	NC	AD20			
	NC	AD21			
	NC	AD22			
	NC	AD23			
	NC	AD24			
	NC	AD25			
	NC	AD26			
	NC	AE1			
	NC	AE2			
	NC	AE3			
	NC	AE5			
	NC	AE18			
	NC	AE19			
	NC	AE20			
	NC	AE21			
	NC	AE22			
	NC	AE23			
	NC	AE25			
	NC	AE26			
	NC	AF2			
	NC	AF3			
	NC	AF4			
	NC	AF5			
	NC	AF17			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	NC	AF19			
	NC	AF20			
	NC	AF22			
	NC	AF23			
	NC	AF24			
	NC	AF25			
	NC	AF26			

2.2.2 Thermal Resistance

Table 2-4 Thermal Resistance

θJA(°C/W) (Flow: 0m/s)	θJB(°C/W)	θJC(°C/W)	θJA(°C/W) (Flow: 1m/s)	θJA(°C/W) (Flow: 2m/s)
12.5	6.6	3.9	10.9	9.9

2.2.3 Pressure value

1. Short term pressure (within 5 minutes): 100g/ball, 676 balls, short term pressure can meet 67.6kg.
2. Long term pressure: 30g/ball, 676 balls, long term pressure can meet 20.28kg.

Chapter 3 Welding Requirements

Table 3-1 Welding Requirements

Preheat (150 °–200 ℃)time	60–120 S
Heating rate (T_L to T_P)	≤ 3 ℃/S
Temperature above T_L (217℃) time	60-150 S
Package peak temperature/T_P	Reflow soldering:250℃ Rewelding:260℃
T_P -5℃ temperature range duration time	≤30S
Rate of temperature fail (T_P to T_L)	≤ 6 ℃/S
25℃ rise to T_P time	≤8 minutes

Note: Reference J-STD-020 standard.

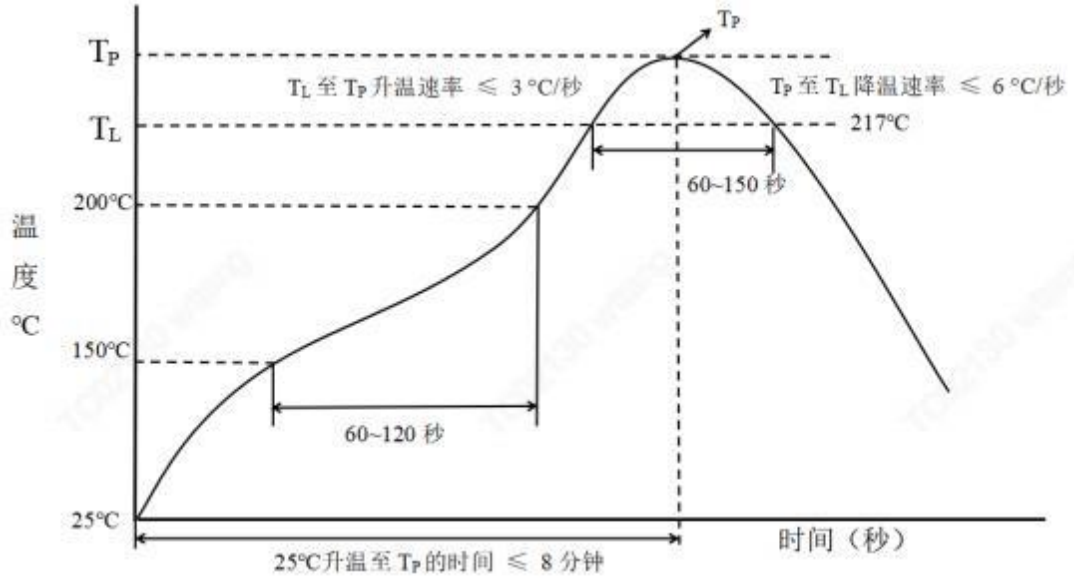


Figure 3-1 Welding Temperature Curve

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