PG2L200H_FFBG1156

(PK04007, V1.0)

(10.11.2022)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	10.11.2022	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Full Spelling
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

PG2L200H_FFBG1156 uses a Flip chip BGA with radiating fin type of packaging. Package size: 35x35mm; Number of balls: 1156; Ball pitch: 1.0mm; Maximum package thickness: 3.10mm

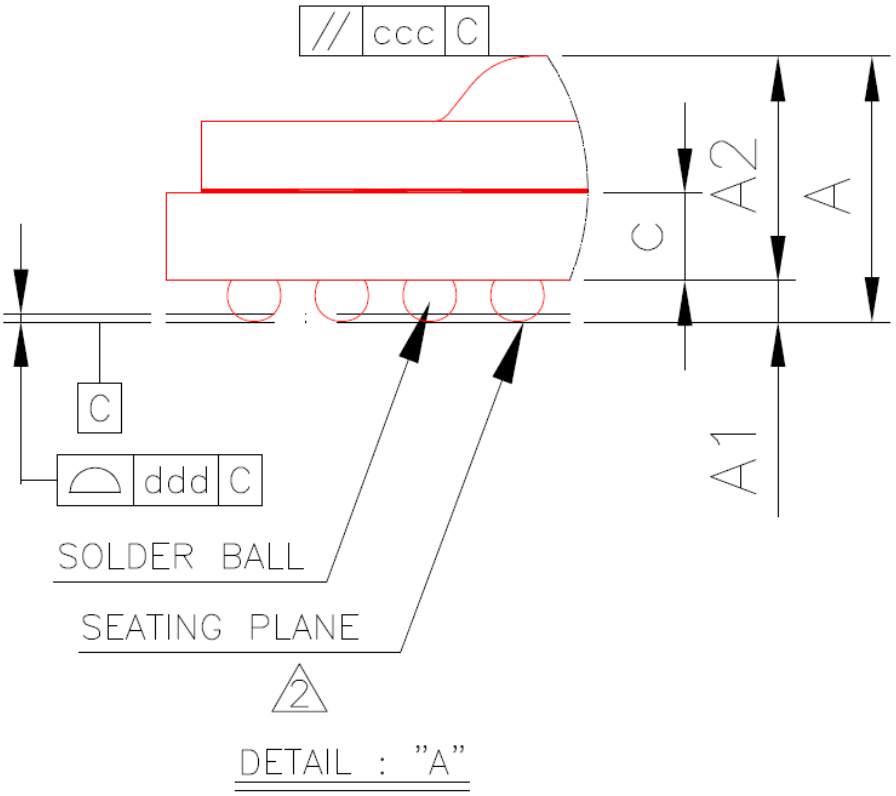
Chapter 2 Package Dimension and Pin

2.1 Package Dimension

Table 2-1 Dimensional Values

Unit：millimeter

Dimension Symbol	Value			Dimension Symbol	Value		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	2.70	2.90	3.10	e	-	1.00	-
A1	0.40	0.50	0.60	b	0.50	0.60	0.70
A2	2.30	2.40	2.50	aaa	-	0.20	-
C	1.07	1.19	1.31	ccc	-	0.35	-
D	34.80	35.00	35.20	ddd	-	0.15	-
E	34.80	35.00	35.20	eee	-	0.25	-
D1	-	33.00	-	fff	-	0.10	-
E1	-	33.00	-	Ball Diam	-	0.60	-



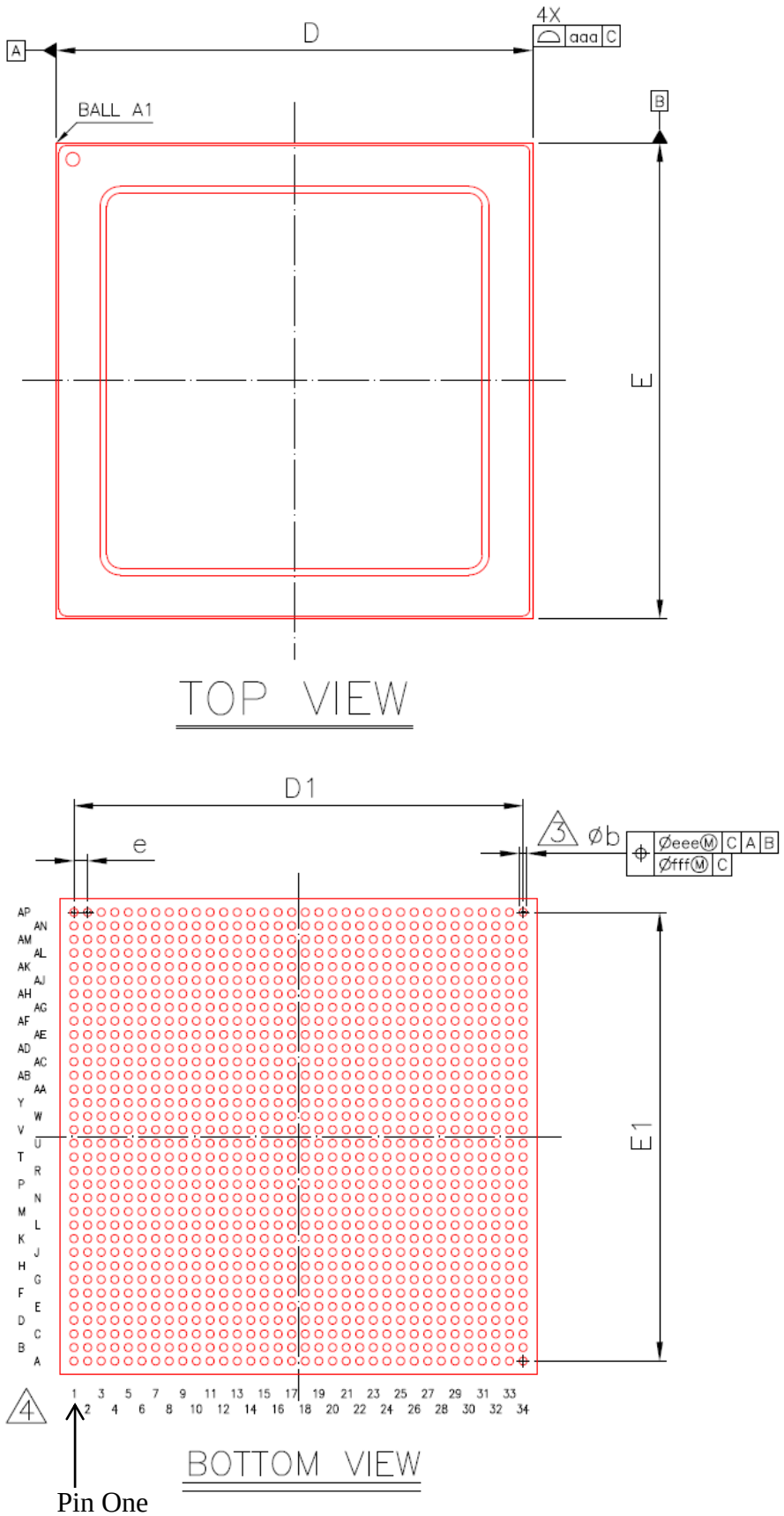


Figure 2-1 Package Outline Dimension (POD)

2.2 Pin Definitions

PG2L200H _ FFBG1156 has 500 user IOs.

Table 2-2 Product Pin Definitions

PIN Name	PIN Type	PIN Direction	PIN Description
General PIN			
DIFFIO_XX_GY_NN[P,N]	General	Input/Output	General pin; (1) "DIFFIO" indicates the pin supports differential input/output and can be used for transmitting and receiving LVDS signals; (2) " XX " indicates bank numbers, which can be L3, L4, L5, L6, L7, R3, R4, R5, R6, R7; (3) " G " indicates belonging to a memory group; (4) " Y " indicates the group number in a bank, each of which contains four groups; (5) "NN" indicates the sequence number of programmable IO pairs in a bank, increasing from 0, a bank contains 24 difference pairs; (6) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end。 During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri-state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.
SIO_XX_NN	General	Input/Output	General pin; (1) " SIO " indicates the pin only supports single ended input/output; (2) " XX " indicates bank numbers, which can be L3, L4, L5, L6, L7, R3, R4, R5, R6, R7; (3) "NN" indicates the sequence number of programmable IO in a bank, increasing from 0, a bank contains 2 single ended IOs; During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri- state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.

PIN Name	PIN Type	PIN Direction	PIN Description
Configuration PIN			
INIT_FLAG_N	Dedicated	Bidirectional (open-drain)	Initialization and configuration status dedicated pin: When it is low, it indicates that the FPGA is being initialized (clear configuration memory) or a configuration error has occurred. The pin has an internal weak pull-up resistor that is enabled during configuration; When the FPGA powers up completion, the pin is driven to low level. Once the FPGA completes initialization, the pin is released. During the power up and initialization process, this pin can accept an external low level input to delay the configuration process. When the FPGA detects high level input on this pin after initialization, the FPGA starts the configuration process.During configuration, this pin serves as an output for the configuration error indication state, and low level indicates that an error occurred. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. After the configuration is complete, user can configure weak pull-up or float state for this pin.
CFG_DONE	Dedicated	Bidirectional (open-drain)	Dedicated configuration status pin, built in weak pull-up resistor about 10K. Output as the configuration completion indicator, high level indicates that the configuration is complete. This pin is an open-drain output. When the FPGA powers up completion, the pin is driven to low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released. After the configuration is complete, the pin can be driven externally to low level, Once the internal start-up timing finds that the external DONE pin is low and the internal start-up circuit stops until the external pin is high. After the configuration is complete, user can configure weak pull-up or float state for this pin.
RSTN	Dedicated	Input	Dedicated configuration reset pin, built in weak pull-up resistor and always effective. For restarting configuration logic and configuration memory, active-low. When this pin is low, the FPGA configuration memory is emptied and a

PIN Name	PIN Type	PIN Direction	PIN Description
			new configuration process begins. The configuration logic reset begins with the falling edge of the pin, and the configuration process begins with the rising edge of the pin. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. Keeping this pin low during power up does not put the FPGA configuration logic in a reset state. After the configuration is complete, user can configure weak pull-up or float state for this pin.
CFG_CLK	Dedicated	Input/Output	Configuration clock pin. Except for the JTAG configuration mode, the configuration process of the FPGA is synchronizing by this clock in other modes. In the slave serial and slave parallel configuration modes, the pin serves as a clock input to obtain configuration data from external sources. In the master SPI configuration mode, the pin serves as a clock output to obtain configuration data from external sources and an external pull-up resistor of 1K is required. When the clock is not needed (such as in the JTAG mode), this pin is in the High-Z state. After the configuration is complete, user can configure weak pull-up or float state for this pin.
TCK	Dedicated	Input	Test clock input pin compliant with IEEE STD 1149.1 and provides a clock for the JTAG chain of the FPGA. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TMS	Dedicated	Input	Dedicated JTAG test mode selection input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDI	Dedicated	Input	Dedicated JTAG test data input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDO	Dedicated	Iutput	Dedicated JTAG test data output pin Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
MODE_2	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.

PIN Name	PIN Type	PIN Direction	PIN Description
MODE_1	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_0	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
SCBV	Dedicated	Input	The pin is always effective on BANKCFG, but only on BANK which the multiplexing configuration pins is located during configuration. When the voltage of VCCIOCFG is 2.5V or 3.3V, the pin must be connected to high level and can be connected directly to the VCCIOCFG. When the voltage of VCCIOCFG is 1.8V or lower, the pin must be connected to low level and can be connected directly to the ground. Note: The pin must be used in conjunction with the software, and the SCBV selection in the bitstream setting must be consistent with the hardware setting. For details about the SCBV pin pull-up/pull-down level corresponds to the configured BANK power, see “UG040012_Logos2 Family Hardware Design Guide”.
FCS_N	Multiplexed	Output	Multi-function configuration pin, used for the Master SPI configuration mode. (1) In the Master SPI X1, X2 and X4 modes, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
MOSI_D0	Multiplexed	Input/Output	Multi-function configuration data pin. (1) “MOSI”, in the master SPI X1 mode; this pin used for serial data output and connects to the data input pin of the external SPI flash (such as DQ0, D, SI, IO0, etc). After the command and address are sent to the external SPI flash, the pin

PIN Name	PIN Type	PIN Direction	PIN Description
			output high-Z or weak pull-up, depending on the state of the IO_STATUS_C pin. (2) In the master SPI X2, X4 and X8 modes, the pin is bidirectional data port, as command and address output to the external SPI flash. Receive the lowest bit data from the external SPI flash. The pin connects to the bidirectional data pin of the external SPI flash (such as DQ0, D, SI, IO0, etc). (3) " D0" , in the slave parallel mode, this pin serves as the D[0] bit of the data bus. (4) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (5) After the configuration is complete, the pin serves as a general pin.
MISO_D1_DI	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X1 mode, " MISO" serves as data input and connects to the data output pin of the external SPI flash (such as DQ1, Q, SO, IO1, etc). (2) In the master SPI X2, X4 and X8 modes, "D1" connects to the second serial data output pin of the external SPI flash (such as DQ1, Q, SO, IO1, etc). (3) In the slave parallel mode, this pin serves as the D[1] bit of the data bus. (4) In the slave serial mode, "D1" serves as data input pin. (5) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. In the other configuration modes(such as JTAG), the state on the pin is ignored (6) After the configuration is complete, the pin serves as a general pin.
D[2，3]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X4 and X8 modes, serve as data input and connects to the data output pin of the external SPI flash. "D2" connects to the third bit data output pin of the external SPI flash (such as DQ2, W#, WP#, IO2, etc). "D3" connects to the fourth bit data output pin of the external SPI flash (such as DQ3, HOLD#, IO3, etc). These pins should be connected to VCCIO via an external weak pull-up resistor of 4.7K. (2) In the slave parallel mode, these pins serve as the D[3:2] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up

PIN Name	PIN Type	PIN Direction	PIN Description
			state. (4) After the configuration is complete, these pins serve as general pins.
D[4，5，6，7]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X8 mode, connect to the second flash in the same way as D[3:0]. (2) In the slave parallel mode, these pins serve as the D[7:4] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[8,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1)In the slave parallel X16 and X32 modes, serve as the D[15:8] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
D[16,…,31]_A[0,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the slave parallel X32 mode, serve as the D[31:16] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
A[16,…,28]	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (2) After the configuration is complete, these pins serve as general pins.
CS_N	Multiplexed	Input	Multi-function configuration pin. For chip select input. Active low. (1) When it is low level, this pin enables the slave parallel mode configuration interface. In the slave parallel configuration mode, the external controller can select the slave parallel bus of the FPGA by controlling this pin. Or this pin connected to the previous FPGA CSO_DOUT pin in the slave parallel configuration chain. (2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.

PIN Name	PIN Type	PIN Direction	PIN Description
RWSEL	Multiplexed	Input	Multi-function configuration pin. For selecting the read/write input in the slave parallel configuration mode (high for read and low for write). (1) When it is high level, the slave parallel configuration mode reads data from the data bus. (2) When it is low level, the slave parallel configuration mode writes data to the data bus. (3) Read and write can be switched only when CS_N is high level. (4) After the configuration is complete, the pin serves as a general pin. (5) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state.
CSO_DOUT	Multiplexed	Output(OD）、Output	Multi-function configuration pin. Needed for cascade. (1) In the master SPI X1 mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2) In the slave serial configuration mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (3) In the slave parallel cascade configuration mode, this pin serves as a chip select signal open-drain output, connects to downstream chip CS_N pin and should be connected to VCCIO via an external pull-up resistor of 330Ω. (4) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state.
VS[0、1]	Multiplexed	Output	Multi-function configuration pin. After the configuration is complete, these pins as general pins.
IO_STATUS_C	Multiplexed	Input	Multi-function configuration pin, used for controlling whether the weak pull-up resistors for all general pins are enabled during the configuration process. (1) When it is set to "0", the internal pull-up resistors for all general pins are enabled. (2) When it is set to "1", the internal pull-up resistors for all general pins are disabled. (3)It is recommended that the pin connects to VCCIO via an external weak

PIN Name	PIN Type	PIN Direction	PIN Description
			pull-up resistor. (4)The pin can connect to VCCIO or VSS, either directly or via an external resistor of no more than 1K. (5) This pin must not be left floating before or during configuration.
ECCLKIN	Multiplexed	Input	The external clock input for the Master configuration mode, which is an optional external clock input to the configuration logic. (1) In the master SPI mode, the FPGA can select this clock input as the configuration clock for the configuration logic. This clock can be divided (Depends on the settings in the bitstream) and output from the CFG_CLK pin. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.
BFOE_N	Multiplexed	Output	Multi-function configuration pin. After the configuration is complete, the pin as a general pin.
BFWE_FCS2_N	Multiplexed	Output	Multi-function configuration pin used for the master SPI X8 configuration modes. (1) In the Master SPI X8 mode, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin acts as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin as a general pin.
BADRVO_N	Multiplexed	Output	Multi-function configuration pin. After the configuration is complete, the pin as a general pin.
Clock PIN			
GMCLK	Multiplexed	Input	Multiplexing global multi-regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL, PPLL, and also drive the multi-regional clock buffer. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. When these pins serve as single regional clock sources, they are able to drive all the IO clock buffers and regional clock buffers of the BANK.
GSCLK	Multiplexed	Input	Multiplexing global single regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer,

PIN Name	PIN Type	PIN Direction	PIN Description
			global clock buffer, GPLL and PPLL. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. They are able to drive all the IO clock buffers and regional clock buffers of the BANK.
Memory Interface PIN			
DQS	Multiplexed	N/A	DDR DQS PIN, each memory group contains two pins.
Reference PIN			
VREF	Multiplexed	N/A	Input reference voltage pins,. When not used as external reference voltage pins, these pins serve as general pins,
Power/ Ground PIN			
VCC	Dedicated	Power	Core logic power, 1.0V. Power supply for core logic.
VCC_DRM	Dedicated	Power	DRM power, 1.0V. Dedicated power supply for DRM. If the voltage is the same as VCC, it can be connected to VCC at the board.
VCCA	Dedicated	Power	Analog power, 1.8V. Power supply for internal analog circuit.
VCCIO[L3、L4、L5、L6、L7、R3、R4、R5、R6、R7、CFG]	Dedicated	Power	IO BANK power.
VCCB	Dedicated	Power	Key memory backup battery power supply voltage, 1.0V~1.9V. When the key function is not used, the pin needs to be connected to the VCCA or ground.
VSS	Dedicated	Ground	Ground
ADC PIN			
VCCADC	Dedicated	Power	ADC analog power, 1.8V. Power supply for ADC analog circuit.
VSSADC	Dedicated	Ground	GND relative to VCCADC
VAADC_P	Dedicated	Input	ADC dedicated analog differential input (Positive).
VAADC_N	Dedicated	Input	ADC dedicated analog differential input (Negative).
VREFADC_P	Dedicated	N/A	1.255V ADC reference voltage pin.
VREFADC_N	Dedicated	N/A	ADC reference voltage ground.
VAA[0,..,15]P,VAA[0,..,15]N	Multiplexed	Input	ADC differential analog input signals.
TSDP	Dedicated	N/A	Positive pin of the temperature sensor diode. When not used temperature diode, the pin needs to be connected to the VSS. When temperature sensor diode is to be used, then appropriate external temperature monitoring chip is required.
TSDN	Dedicated	N/A	Negative pin of the temperature sensor diode.

PIN Name	PIN Type	PIN Direction	PIN Description
HSST PIN			
HSSTAVCC_G[3、7]	Dedicated	Power	1.0V analog power pin, power supply for HSST internal transmits and receives circuit.
HSSTAVCCPLL_ G[3、7]	Dedicated	Power	1.2V analog power pin, power supply for HSST internal PLL.
HSSTRREF_Q[L3、L7、R3、R7]	Dedicated	Input	Calibration resistance input pin of the terminal resistance calibration circuit.
HSSTREFCLK[0,1]P_Q[L3、L7、R3、R7]	Dedicated	Input	Positive end of differential clock input pin, provide a reference clock to HSST.
HSSTREFCLK[0,1]N_Q[L3、L7、R3、R7]	Dedicated	Input	Negative end of differential clock input pin, provide a reference clock to HSST.
HSSTTX[0,1,2,3][P,N]_Q[L3、L7、R3、R7]	Dedicated	Output	Channel differential outputs of HSST. Each HSST has 4 pairs.
HSSTRX[0,1,2,3][P,N]_Q[L3、L7、R3、R7]	Dedicated	Input	Channel differential inputs of HSST. Each HSST has 4 pairs.

2.2.1 Pin Name list

Table 2-1 Pin Name List

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L3	SIO_L3_00	L23		5.9906	
L3	DIFFIO_L3_G0_00P	M24	IO_1_P	10.3938	BANKL3_G0_DQS
L3	DIFFIO_L3_G0_00N	L24	IO_1_N	11.1470	
L3	DIFFIO_L3_G0_01P	K23	IO_2_P	26.3626	
L3	DIFFIO_L3_G0_01N	J23	IO_2_N	27.0639	
L3	DIFFIO_L3_G0_02P_DQS	G24	IO_3_P	42.9972	
L3	DIFFIO_L3_G0_02N_DQS	G25	IO_3_N	43.3700	
L3	DIFFIO_L3_G0_03P	K25	IO_4_P	30.2572	
L3	DIFFIO_L3_G0_03N	J25	IO_4_N	30.9406	
L3	DIFFIO_L3_G0_04P	M25	IO_5_P	18.4761	
L3	DIFFIO_L3_G0_04N	L25	IO_5_N	18.9497	
L3	DIFFIO_L3_G0_05P	J24	IO_6_P	50.1774	
L3	DIFFIO_L3_G0_05N_VREF	H24	IO_6_N	50.8549	
L3	DIFFIO_L3_G1_06P	H27	IO_7_P	50.9229	BANKL3_G1_DQS
L3	DIFFIO_L3_G1_06N	G27	IO_7_N	51.7390	
L3	DIFFIO_L3_G1_07P	H26	IO_8_P	53.3634	
L3	DIFFIO_L3_G1_07N	G26	IO_8_N	53.6639	
L3	DIFFIO_L3_G1_08P_DQS	L27	IO_9_P	38.5597	
L3	DIFFIO_L3_G1_08N_DQS	K27	IO_9_N	38.8868	
L3	DIFFIO_L3_G1_09P	K26	IO_10_P	39.1563	
L3	DIFFIO_L3_G1_09N	J26	IO_10_N	39.7829	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L3	DIFFIO_L3_G1_10P_GSCLK	L28	IO_11_P	45.0663	
L3	DIFFIO_L3_G1_10N_GSCLK	K28	IO_11_N	45.5366	
L3	DIFFIO_L3_G1_11P_GMCLK	J28	IO_12_P	51.8406	
L3	DIFFIO_L3_G1_11N_GMCLK	H28	IO_12_N	52.2982	
L3	DIFFIO_L3_G2_12P_GMCLK	J29	IO_13_P	62.1153	BANKL3_G2_DQS
L3	DIFFIO_L3_G2_12N_GMCLK	H29	IO_13_N	62.3642	
L3	DIFFIO_L3_G2_13P_GSCLK	K30	IO_14_P	70.7656	
L3	DIFFIO_L3_G2_13N_GSCLK	J30	IO_14_N	71.7142	
L3	DIFFIO_L3_G2_14P_DQS	G29	IO_15_P	72.8913	
L3	DIFFIO_L3_G2_14N_DQS	G30	IO_15_N	73.3433	
L3	DIFFIO_L3_G2_15P	K31	IO_16_P	75.9126	
L3	DIFFIO_L3_G2_15N	J31	IO_16_N	76.5039	
L3	DIFFIO_L3_G2_16P	H31	IO_17_P	79.7300	
L3	DIFFIO_L3_G2_16N	G31	IO_17_N	80.2222	
L3	DIFFIO_L3_G2_17P	L29	IO_18_P	54.9670	
L3	DIFFIO_L3_G2_17N	L30	IO_18_N	56.5394	
L3	DIFFIO_L3_G3_18P	H32	IO_19_P	85.2280	BANKL3_G3_DQS
L3	DIFFIO_L3_G3_18N_VREF	G32	IO_19_N	85.8061	
L3	DIFFIO_L3_G3_19P	K33	IO_20_P	95.5137	
L3	DIFFIO_L3_G3_19N	J34	IO_20_N	96.3150	
L3	DIFFIO_L3_G3_20P_DQS	H33	IO_21_P	88.2804	
L3	DIFFIO_L3_G3_20N_DQS	G34	IO_21_N	88.7745	
L3	DIFFIO_L3_G3_21P	L32	IO_22_P	83.8552	
L3	DIFFIO_L3_G3_21N	K32	IO_22_N	84.3929	
L3	DIFFIO_L3_G3_22P	J33	IO_23_P	87.6283	
L3	DIFFIO_L3_G3_22N	H34	IO_23_N	87.8120	
L3	DIFFIO_L3_G3_23P	L33	IO_24_P	88.7468	
L3	DIFFIO_L3_G3_23N	L34	IO_24_N	89.4123	
L3	SIO_L3_01	M26		2.9892	
L4	SIO_L4_00	T24		13.5213	
L4	DIFFIO_L4_G0_00P_VAA1P	R26	IO_25_P	39.0011	BANKL4_G0_DQS
L4	DIFFIO_L4_G0_00N_VAA1N	P26	IO_25_N	37.4960	
L4	DIFFIO_L4_G0_01P_VAA2P	N26	IO_26_P	31.8368	
L4	DIFFIO_L4_G0_01N_VAA2N	M27	IO_26_N	33.2041	
L4	DIFFIO_L4_G0_02P_DQS_VAA3P	U25	IO_27_P	41.6266	
L4	DIFFIO_L4_G0_02N_DQS_VAA3N	T25	IO_27_N	41.3969	
L4	DIFFIO_L4_G0_03P	P24	IO_28_P	28.2962	
L4	DIFFIO_L4_G0_03N	N24	IO_28_N	28.2681	
L4	DIFFIO_L4_G0_04P_VAA5P	U26	IO_29_P	47.2699	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L4	DIFFIO_L4_G0_04N_VAA5N	U27	IO_29_N	46.5001	
L4	DIFFIO_L4_G0_05P	R25	IO_30_P	26.4479	
L4	DIFFIO_L4_G0_05N_VREF	P25	IO_30_N	26.9457	
L4	DIFFIO_L4_G1_06P_VAA7P	T27	IO_31_P	43.4940	BANKL4_G1_DQS
L4	DIFFIO_L4_G1_06N_VAA7N	R27	IO_31_N	44.7465	
L4	DIFFIO_L4_G1_07P_VAA8P	N27	IO_32_P	39.2863	
L4	DIFFIO_L4_G1_07N_VAA8N	N28	IO_32_N	40.3874	
L4	DIFFIO_L4_G1_08P_DQS_VAA9P	T28	IO_33_P	48.6673	
L4	DIFFIO_L4_G1_08N_DQS_VAA9N	R28	IO_33_N	48.9400	
L4	DIFFIO_L4_G1_09P_VAA10P	N29	IO_34_P	55.3670	
L4	DIFFIO_L4_G1_09N_VAA10N	M29	IO_34_N	55.9251	
L4	DIFFIO_L4_G1_10P_GSCLK	U29	IO_35_P	55.6422	
L4	DIFFIO_L4_G1_10N_GSCLK	T29	IO_35_N	57.3063	
L4	DIFFIO_L4_G1_11P_GMCLK	P28	IO_36_P	45.3125	
L4	DIFFIO_L4_G1_11N_GMCLK	P29	IO_36_N	45.7115	
L4	DIFFIO_L4_G2_12P_GMCLK	R30	IO_37_P	57.3162	BANKL4_G2_DQS
L4	DIFFIO_L4_G2_12N_GMCLK	P30	IO_37_N	57.7219	
L4	DIFFIO_L4_G2_13P_GSCLK	U30	IO_38_P	64.9321	
L4	DIFFIO_L4_G2_13N_GSCLK	T30	IO_38_N	65.2158	
L4	DIFFIO_L4_G2_14P_DQS	M30	IO_39_P	72.2345	
L4	DIFFIO_L4_G2_14N_DQS_BADRVO_N	M31	IO_39_N	72.6796	
L4	DIFFIO_L4_G2_15P_A28	R31	IO_40_P	86.4570	
L4	DIFFIO_L4_G2_15N_A27	P31	IO_40_N	86.8566	
L4	DIFFIO_L4_G2_16P_A26	N31	IO_41_P	76.4069	
L4	DIFFIO_L4_G2_16N_A25	M32	IO_41_N	76.9861	
L4	DIFFIO_L4_G2_17P_A24	U31	IO_42_P	70.8909	
L4	DIFFIO_L4_G2_17N_A23	U32	IO_42_N	71.4303	
L4	DIFFIO_L4_G3_18P_A22	T32	IO_43_P	67.6856	BANKL4_G3_DQS
L4	DIFFIO_L4_G3_18N_VREF_A21	R32	IO_43_N	68.0445	
L4	DIFFIO_L4_G3_19P_A20	N32	IO_44_P	106.0729	
L4	DIFFIO_L4_G3_19N_A19	N33	IO_44_N	106.9365	
L4	DIFFIO_L4_G3_20P_DQS	T33	IO_45_P	77.8659	
L4	DIFFIO_L4_G3_20N_DQS_A18	R33	IO_45_N	78.2795	
L4	DIFFIO_L4_G3_21P_A17	N34	IO_46_P	122.2171	
L4	DIFFIO_L4_G3_21N_A16	M34	IO_46_N	122.8693	
L4	DIFFIO_L4_G3_22P_BFOE_N	U34	IO_47_P	83.2508	
L4	DIFFIO_L4_G3_22N_BFWE_FCS2_N	T34	IO_47_N	83.3946	
L4	DIFFIO_L4_G3_23P_VS1	P33	IO_48_P	108.0392	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L4	DIFFIO_L4_G3_23N_VS0	P34	IO_48_N	108.6706	
L4	SIO_L4_01	U24		7.8804	
L5	SIO_L5_00	V24		12.0567	
L5	DIFFIO_L5_G0_00P_MOSI_D0	V28	IO_49_P	48.7008	BANKL5_G0_DQS
L5	DIFFIO_L5_G0_00N_MISO_D1_DI	V29	IO_49_N	49.7704	
L5	DIFFIO_L5_G0_01P_D2	V26	IO_50_P	47.1097	
L5	DIFFIO_L5_G0_01N_D3	V27	IO_50_N	48.3017	
L5	DIFFIO_L5_G0_02P_DQS_IO_STATUS_C	W26	IO_51_P	62.7419	
L5	DIFFIO_L5_G0_02N_DQS_ECCLKIN	Y26	IO_51_N	60.8385	
L5	DIFFIO_L5_G0_03P_D4	W28	IO_52_P	48.9852	
L5	DIFFIO_L5_G0_03N_D5	W29	IO_52_N	49.4089	
L5	DIFFIO_L5_G0_04P_D6	W25	IO_53_P	66.1457	
L5	DIFFIO_L5_G0_04N_D7	Y25	IO_53_N	66.7726	
L5	DIFFIO_L5_G0_05P_FCS_N	Y27	IO_54_P	44.5231	
L5	DIFFIO_L5_G0_05N_VREF_D8	Y28	IO_54_N	45.1525	
L5	DIFFIO_L5_G1_06P_D9	V31	IO_55_P	63.1274	BANKL5_G1_DQS
L5	DIFFIO_L5_G1_06N_D10	V32	IO_55_N	63.3892	
L5	DIFFIO_L5_G1_07P_D11	W33	IO_56_P	95.9506	
L5	DIFFIO_L5_G1_07N_D12	W34	IO_56_N	96.8204	
L5	DIFFIO_L5_G1_08P_DQS_N	V33	IO_57_P	77.1834	
L5	DIFFIO_L5_G1_08N_DQS_D13	V34	IO_57_N	77.6797	
L5	DIFFIO_L5_G1_09P_D14	Y32	IO_58_P	87.1965	
L5	DIFFIO_L5_G1_09N_D15	Y33	IO_58_N	87.9456	
L5	DIFFIO_L5_G1_10P_GSCLK	W30	IO_59_P	56.9969	
L5	DIFFIO_L5_G1_10N_GSCLK	W31	IO_59_N	57.5326	
L5	DIFFIO_L5_G1_11P_GMCLK	Y30	IO_60_P	70.6908	
L5	DIFFIO_L5_G1_11N_GMCLK	Y31	IO_60_N	71.4832	
L5	DIFFIO_L5_G2_12P_GMCLK	AA30	IO_61_P	67.2278	BANKL5_G2_DQS
L5	DIFFIO_L5_G2_12N_GMCLK	AB30	IO_61_N	67.4694	
L5	DIFFIO_L5_G2_13P_GSCLK	AB31	IO_62_P	82.8624	
L5	DIFFIO_L5_G2_13N_GSCLK	AB32	IO_62_N	83.6180	
L5	DIFFIO_L5_G2_14P_DQS_RWSEL	AC33	IO_63_P	86.1526	
L5	DIFFIO_L5_G2_14N_DQS_CSO_DOUT	AC34	IO_63_N	86.1451	
L5	DIFFIO_L5_G2_15P_CS_N	AA32	IO_64_P	98.4433	
L5	DIFFIO_L5_G2_15N_D31_A15	AA33	IO_64_N	99.0166	
L5	DIFFIO_L5_G2_16P_D30_A14	AC31	IO_65_P	69.9712	
L5	DIFFIO_L5_G2_16N_D29_A13	AC32	IO_65_N	70.6093	
L5	DIFFIO_L5_G2_17P_D28_A12	AA34	IO_66_P	102.9328	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L5	DIFFIO_L5_G2_17N_D27_A11	AB34	IO_66_N	103.3230	
L5	DIFFIO_L5_G3_18P_D26_A10	AC28	IO_67_P	62.4102	BANKL5_G3_DQS
L5	DIFFIO_L5_G3_18N_VREF_D25_A9	AC29	IO_67_N	61.8825	
L5	DIFFIO_L5_G3_19P_D24_A8	AA27	IO_68_P	45.3593	
L5	DIFFIO_L5_G3_19N_D23_A7	AA28	IO_68_N	45.8130	
L5	DIFFIO_L5_G3_20P_DQS	AB26	IO_69_P	60.9523	
L5	DIFFIO_L5_G3_20N_DQS_D22_A6	AB27	IO_69_N	59.3962	
L5	DIFFIO_L5_G3_21P_D21_A5	AA29	IO_70_P	59.9042	
L5	DIFFIO_L5_G3_21N_D20_A4	AB29	IO_70_N	59.7090	
L5	DIFFIO_L5_G3_22P_D19_A3	AA24	IO_71_P	38.3043	
L5	DIFFIO_L5_G3_22N_D18_A2	AA25	IO_71_N	37.7963	
L5	DIFFIO_L5_G3_23P_D17_A1	AB24	IO_72_P	44.7973	
L5	DIFFIO_L5_G3_23N_D16_A0	AB25	IO_72_N	45.7768	
L5	SIO_L5_01	W24		6.3070	
L6	SIO_L6_00	AD23		35.6346	
L6	DIFFIO_L6_G0_00P	AF34	IO_73_P	94.9735	BANKL6_G0_DQS
L6	DIFFIO_L6_G0_00N	AG34	IO_73_N	95.6237	
L6	DIFFIO_L6_G0_01P	AD33	IO_74_P	97.3435	
L6	DIFFIO_L6_G0_01N	AD34	IO_74_N	97.9947	
L6	DIFFIO_L6_G0_02P_DQS	AH33	IO_75_P	99.2909	
L6	DIFFIO_L6_G0_02N_DQS	AH34	IO_75_N	99.3252	
L6	DIFFIO_L6_G0_03P	AE33	IO_76_P	94.0030	
L6	DIFFIO_L6_G0_03N	AF33	IO_76_N	94.4024	
L6	DIFFIO_L6_G0_04P	AG32	IO_77_P	91.2689	
L6	DIFFIO_L6_G0_04N	AH32	IO_77_N	91.7124	
L6	DIFFIO_L6_G0_05P	AE32	IO_78_P	86.1215	
L6	DIFFIO_L6_G0_05N_VREF	AF32	IO_78_N	86.3922	
L6	DIFFIO_L6_G1_06P	AD31	IO_79_P	65.6966	BANKL6_G1_DQS
L6	DIFFIO_L6_G1_06N	AE31	IO_79_N	65.9983	
L6	DIFFIO_L6_G1_07P	AD30	IO_80_P	67.0805	
L6	DIFFIO_L6_G1_07N	AE30	IO_80_N	67.5461	
L6	DIFFIO_L6_G1_08P_DQS	AD28	IO_81_P	51.8442	
L6	DIFFIO_L6_G1_08N_DQS	AD29	IO_81_N	52.3246	
L6	DIFFIO_L6_G1_09P	AG31	IO_82_P	91.2615	
L6	DIFFIO_L6_G1_09N	AH31	IO_82_N	91.6959	
L6	DIFFIO_L6_G1_10P_GSCLK	AF29	IO_83_P	70.3119	
L6	DIFFIO_L6_G1_10N_GSCLK	AF30	IO_83_N	71.0164	
L6	DIFFIO_L6_G1_11P_GMCLK	AG29	IO_84_P	85.1048	
L6	DIFFIO_L6_G1_11N_GMCLK	AG30	IO_84_N	85.7138	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L6	DIFFIO_L6_G2_12P_GMCLK	AH28	IO_85_P	77.5940	BANKL6_G2_DQS
L6	DIFFIO_L6_G2_12N_GMCLK	AH29	IO_85_N	77.8791	
L6	DIFFIO_L6_G2_13P_GSCLK	AE28	IO_86_P	61.5884	
L6	DIFFIO_L6_G2_13N_GSCLK	AF28	IO_86_N	62.1533	
L6	DIFFIO_L6_G2_14P_DQS	AD26	IO_87_P	57.6781	
L6	DIFFIO_L6_G2_14N_DQS	AE26	IO_87_N	58.0884	
L6	DIFFIO_L6_G2_15P	AC26	IO_88_P	31.2818	
L6	DIFFIO_L6_G2_15N	AC27	IO_88_N	30.4293	
L6	DIFFIO_L6_G2_16P	AG27	IO_89_P	66.9910	
L6	DIFFIO_L6_G2_16N	AH27	IO_89_N	67.1840	
L6	DIFFIO_L6_G2_17P	AE27	IO_90_P	55.5341	
L6	DIFFIO_L6_G2_17N	AF27	IO_90_N	55.8797	
L6	DIFFIO_L6_G3_18P	AG26	IO_91_P	70.5974	BANKL6_G3_DQS
L6	DIFFIO_L6_G3_18N_VREF	AH26	IO_91_N	70.7708	
L6	DIFFIO_L6_G3_19P	AE23	IO_92_P	69.8657	
L6	DIFFIO_L6_G3_19N	AF23	IO_92_N	70.6824	
L6	DIFFIO_L6_G3_20P_DQS	AG24	IO_93_P	75.1843	
L6	DIFFIO_L6_G3_20N_DQS	AH24	IO_93_N	76.9405	
L6	DIFFIO_L6_G3_21P	AC24	IO_94_P	40.9524	
L6	DIFFIO_L6_G3_21N	AD24	IO_94_N	41.0431	
L6	DIFFIO_L6_G3_22P	AF25	IO_95_P	65.1025	
L6	DIFFIO_L6_G3_22N	AG25	IO_95_N	65.7567	
L6	DIFFIO_L6_G3_23P	AD25	IO_96_P	40.4669	
L6	DIFFIO_L6_G3_23N	AE25	IO_96_N	40.5384	
L6	SIO_L6_01	AF24		45.2892	
L7	SIO_L7_00	AJ24		54.4630	
L7	DIFFIO_L7_G0_00P	AL34	IO_97_P	118.7298	BANKL7_G0_DQS
L7	DIFFIO_L7_G0_00N	AM34	IO_97_N	118.5196	
L7	DIFFIO_L7_G0_01P	AJ33	IO_98_P	116.7644	
L7	DIFFIO_L7_G0_01N	AJ34	IO_98_N	117.5146	
L7	DIFFIO_L7_G0_02P_DQS	AN34	IO_99_P	128.7677	
L7	DIFFIO_L7_G0_02N_DQS	AP34	IO_99_N	129.1194	
L7	DIFFIO_L7_G0_03P	AK33	IO_100_P	113.8186	
L7	DIFFIO_L7_G0_03N	AL33	IO_100_N	114.3547	
L7	DIFFIO_L7_G0_04P	AN33	IO_101_P	124.2905	
L7	DIFFIO_L7_G0_04N	AP33	IO_101_N	124.9188	
L7	DIFFIO_L7_G0_05P	AL32	IO_102_P	109.1862	
L7	DIFFIO_L7_G0_05N_VREF	AM32	IO_102_N	109.4393	
L7	DIFFIO_L7_G1_06P	AJ31	IO_103_P	92.8072	BANKL7_G1_D

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L7	DIFFIO_L7_G1_06N	AK32	IO_103_N	93.3457	QS
L7	DIFFIO_L7_G1_07P	AM31	IO_104_P	117.0847	
L7	DIFFIO_L7_G1_07N	AN32	IO_104_N	117.4558	
L7	DIFFIO_L7_G1_08P_DQS	AJ30	IO_105_P	85.0648	
L7	DIFFIO_L7_G1_08N_DQS	AK31	IO_105_N	85.7286	
L7	DIFFIO_L7_G1_09P	AN31	IO_106_P	117.5531	
L7	DIFFIO_L7_G1_09N	AP31	IO_106_N	117.7167	
L7	DIFFIO_L7_G1_10P_GSCLK	AJ29	IO_107_P	78.8038	
L7	DIFFIO_L7_G1_10N_GSCLK	AK30	IO_107_N	78.9830	
L7	DIFFIO_L7_G1_11P_GMCLK	AL30	IO_108_P	94.1997	
L7	DIFFIO_L7_G1_11N_GMCLK	AM30	IO_108_N	94.7388	
L7	DIFFIO_L7_G2_12P_GMCLK	AL28	IO_109_P	78.0067	BANKL7_G2_DQS
L7	DIFFIO_L7_G2_12N_GMCLK	AL29	IO_109_N	78.6176	
L7	DIFFIO_L7_G2_13P_GSCLK	AJ28	IO_110_P	70.4536	
L7	DIFFIO_L7_G2_13N_GSCLK	AK28	IO_110_N	71.0400	
L7	DIFFIO_L7_G2_14P_DQS	AP29	IO_111_P	101.2565	
L7	DIFFIO_L7_G2_14N_DQS	AP30	IO_111_N	101.4975	
L7	DIFFIO_L7_G2_15P	AM29	IO_112_P	96.8844	
L7	DIFFIO_L7_G2_15N	AN29	IO_112_N	97.1968	
L7	DIFFIO_L7_G2_16P	AN28	IO_113_P	86.4285	
L7	DIFFIO_L7_G2_16N	AP28	IO_113_N	86.8689	
L7	DIFFIO_L7_G2_17P	AK27	IO_114_P	73.0685	
L7	DIFFIO_L7_G2_17N	AL27	IO_114_N	73.5988	
L7	DIFFIO_L7_G3_18P	AJ25	IO_115_P	50.7261	BANKL7_G3_DQS
L7	DIFFIO_L7_G3_18N_VREF	AK25	IO_115_N	50.8171	
L7	DIFFIO_L7_G3_19P	AJ26	IO_116_P	61.2737	
L7	DIFFIO_L7_G3_19N	AK26	IO_116_N	61.9470	
L7	DIFFIO_L7_G3_20P_DQS	AM26	IO_117_P	70.9964	
L7	DIFFIO_L7_G3_20N_DQS	AN26	IO_117_N	71.4913	
L7	DIFFIO_L7_G3_21P	AM27	IO_118_P	120.6415	
L7	DIFFIO_L7_G3_21N	AN27	IO_118_N	120.1158	
L7	DIFFIO_L7_G3_22P	AL25	IO_119_P	60.6455	
L7	DIFFIO_L7_G3_22N	AM25	IO_119_N	60.9643	
L7	DIFFIO_L7_G3_23P	AP25	IO_120_P	95.0278	
L7	DIFFIO_L7_G3_23N	AP26	IO_120_N	95.4125	
L7	SIO_L7_01	AL24		51.7443	
R3	SIO_R3_00	H12		22.9102	
R3	DIFFIO_R3_G0_00P	L12	IO_121_P	10.2919	BANKR3_G0_DQS
R3	DIFFIO_R3_G0_00N	K12	IO_121_N	10.9249	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R3	DIFFIO_R3_G0_01P	G10	IO_122_P	47.1688	
R3	DIFFIO_R3_G0_01N	G9	IO_122_N	47.6300	
R3	DIFFIO_R3_G0_02P_DQS	K11	IO_123_P	24.5356	
R3	DIFFIO_R3_G0_02N_DQS	J11	IO_123_N	25.0773	
R3	DIFFIO_R3_G0_03P	H11	IO_124_P	74.2231	
R3	DIFFIO_R3_G0_03N	G11	IO_124_N	74.1215	
R3	DIFFIO_R3_G0_04P	L10	IO_125_P	28.0246	
R3	DIFFIO_R3_G0_04N	L9	IO_125_N	28.8045	
R3	DIFFIO_R3_G0_05P	K10	IO_126_P	28.9187	
R3	DIFFIO_R3_G0_05N_VREF	J10	IO_126_N	29.1562	
R3	DIFFIO_R3_G1_06P	J9	IO_127_P	35.9567	BANKR3_G1_DQS
R3	DIFFIO_R3_G1_06N	J8	IO_127_N	36.3910	
R3	DIFFIO_R3_G1_07P	H9	IO_128_P	47.8740	
R3	DIFFIO_R3_G1_07N	H8	IO_128_N	48.4519	
R3	DIFFIO_R3_G1_08P_DQS	L8	IO_129_P	41.5959	
R3	DIFFIO_R3_G1_08N_DQS	K8	IO_129_N	41.8420	
R3	DIFFIO_R3_G1_09P	G7	IO_130_P	65.4576	
R3	DIFFIO_R3_G1_09N	G6	IO_130_N	65.9094	
R3	DIFFIO_R3_G1_10P_GSCLK	K7	IO_131_P	37.7981	
R3	DIFFIO_R3_G1_10N_GSCLK	K6	IO_131_N	36.6493	
R3	DIFFIO_R3_G1_11P_GMCLK	H7	IO_132_P	63.4492	
R3	DIFFIO_R3_G1_11N_GMCLK	H6	IO_132_N	63.9619	
R3	DIFFIO_R3_G2_12P_GMCLK	G5	IO_133_P	65.4329	BANKR3_G2_DQS
R3	DIFFIO_R3_G2_12N_GMCLK	G4	IO_133_N	65.9556	
R3	DIFFIO_R3_G2_13P_GSCLK	J6	IO_134_P	67.5900	
R3	DIFFIO_R3_G2_13N_GSCLK	J5	IO_134_N	68.3513	
R3	DIFFIO_R3_G2_14P_DQS	F3	IO_135_P	82.3509	
R3	DIFFIO_R3_G2_14N_DQS	F2	IO_135_N	82.9470	
R3	DIFFIO_R3_G2_15P	L5	IO_136_P	68.6106	
R3	DIFFIO_R3_G2_15N	K5	IO_136_N	68.2327	
R3	DIFFIO_R3_G2_16P	H4	IO_137_P	69.8103	
R3	DIFFIO_R3_G2_16N	H3	IO_137_N	69.9082	
R3	DIFFIO_R3_G2_17P	J4	IO_138_P	83.0618	
R3	DIFFIO_R3_G2_17N	J3	IO_138_N	83.4339	
R3	DIFFIO_R3_G3_18P	L4	IO_139_P	65.2281	BANKR3_G3_DQS
R3	DIFFIO_R3_G3_18N_VREF	L3	IO_139_N	65.6403	
R3	DIFFIO_R3_G3_19P	H2	IO_140_P	105.7033	
R3	DIFFIO_R3_G3_19N	G2	IO_140_N	106.0858	
R3	DIFFIO_R3_G3_20P_DQS	K1	IO_141_P	91.5870	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R3	DIFFIO_R3_G3_20N_DQS	J1	IO_141_N	92.0398	
R3	DIFFIO_R3_G3_21P	H1	IO_142_P	113.9876	
R3	DIFFIO_R3_G3_21N	G1	IO_142_N	114.5915	
R3	DIFFIO_R3_G3_22P	M2	IO_143_P	71.4309	
R3	DIFFIO_R3_G3_22N	L2	IO_143_N	71.8066	
R3	DIFFIO_R3_G3_23P	K3	IO_144_P	87.2829	
R3	DIFFIO_R3_G3_23N	K2	IO_144_N	88.0170	
R3	SIO_R3_01	L7		36.5683	
R4	SIO_R4_00	R11		7.3260	
R4	DIFFIO_R4_G0_00P_VAA4P	M7	IO_145_P	44.1512	
R4	DIFFIO_R4_G0_00N_VAA4N	M6	IO_145_N	44.6421	
R4	DIFFIO_R4_G0_01P_VAA6P	N9	IO_146_P	38.4953	
R4	DIFFIO_R4_G0_01N_VAA6N	M9	IO_146_N	39.5325	
R4	DIFFIO_R4_G0_02P_DQS_VAA11P	N8	IO_147_P	35.0341	
R4	DIFFIO_R4_G0_02N_DQS_VAA11N	N7	IO_147_N	35.4469	BANKR4_G0_DQS
R4	DIFFIO_R4_G0_03P	M11	IO_148_P	40.7249	
R4	DIFFIO_R4_G0_03N	M10	IO_148_N	41.8401	
R4	DIFFIO_R4_G0_04P_VAA12P	P9	IO_149_P	25.7443	
R4	DIFFIO_R4_G0_04N_VAA12N	P8	IO_149_N	26.3249	
R4	DIFFIO_R4_G0_05P	P6	IO_150_P	55.4370	
R4	DIFFIO_R4_G0_05N_VREF	N6	IO_150_N	55.6926	
R4	DIFFIO_R4_G1_06P_VAA13P	N1	IO_151_P	80.1054	
R4	DIFFIO_R4_G1_06N_VAA13N	M1	IO_151_N	79.6403	
R4	DIFFIO_R4_G1_07P_VAA14P	M5	IO_152_P	71.6764	
R4	DIFFIO_R4_G1_07N_VAA14N	M4	IO_152_N	71.8368	
R4	DIFFIO_R4_G1_08P_DQS_VAA15P	R1	IO_153_P	77.7346	
R4	DIFFIO_R4_G1_08N_DQS_VAA15N	P1	IO_153_N	77.6917	BANKR4_G1_DQS
R4	DIFFIO_R4_G1_09P_VAA0P	N3	IO_154_P	86.5177	
R4	DIFFIO_R4_G1_09N_VAA0N	N2	IO_154_N	86.3828	
R4	DIFFIO_R4_G1_10P_GSCLK	P4	IO_155_P	59.8178	
R4	DIFFIO_R4_G1_10N_GSCLK	P3	IO_155_N	60.2451	
R4	DIFFIO_R4_G1_11P_GMCLK	P5	IO_156_P	65.7829	
R4	DIFFIO_R4_G1_11N_GMCLK	N4	IO_156_N	66.2350	
R4	DIFFIO_R4_G2_12P_GMCLK	R6	IO_157_P	45.6605	
R4	DIFFIO_R4_G2_12N_GMCLK	R5	IO_157_N	46.1373	
R4	DIFFIO_R4_G2_13P_GSCLK	T5	IO_158_P	62.0413	BANKR4_G2_DQS
R4	DIFFIO_R4_G2_13N_GSCLK	T4	IO_158_N	62.3115	
R4	DIFFIO_R4_G2_14P_DQS	R3	IO_159_P	64.4959	
R4	DIFFIO_R4_G2_14N_DQS	R2	IO_159_N	65.0426	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R4	DIFFIO_R4_G2_15P	U2	IO_160_P	86.9156	
R4	DIFFIO_R4_G2_15N	U1	IO_160_N	87.1805	
R4	DIFFIO_R4_G2_16P	T3	IO_161_P	63.3573	
R4	DIFFIO_R4_G2_16N	T2	IO_161_N	63.4649	
R4	DIFFIO_R4_G2_17P	U5	IO_162_P	63.0623	
R4	DIFFIO_R4_G2_17N	U4	IO_162_N	63.5945	
R4	DIFFIO_R4_G3_18P	R8	IO_163_P	70.5724	BANKR4_G3_DQS
R4	DIFFIO_R4_G3_18N_VREF	R7	IO_163_N	71.5377	
R4	DIFFIO_R4_G3_19P	R10	IO_164_P	24.8281	
R4	DIFFIO_R4_G3_19N	P10	IO_164_N	25.6766	
R4	DIFFIO_R4_G3_20P_DQS	U10	IO_165_P	37.2777	
R4	DIFFIO_R4_G3_20N_DQS	T10	IO_165_N	36.4741	
R4	DIFFIO_R4_G3_21P	U7	IO_166_P	46.7299	
R4	DIFFIO_R4_G3_21N	U6	IO_166_N	47.2301	
R4	DIFFIO_R4_G3_22P	T8	IO_167_P	33.5989	
R4	DIFFIO_R4_G3_22N	T7	IO_167_N	34.1151	
R4	DIFFIO_R4_G3_23P	U9	IO_168_P	23.1180	
R4	DIFFIO_R4_G3_23N	T9	IO_168_N	23.0918	
R4	SIO_R4_01	U11		9.2855	
R5	SIO_R5_00	Y11		24.5102	
R5	DIFFIO_R5_G0_00P	W10	IO_169_P	52.6348	BANKR5_G0_DQS
R5	DIFFIO_R5_G0_00N	Y10	IO_169_N	54.2749	
R5	DIFFIO_R5_G0_01P	V9	IO_170_P	40.7367	
R5	DIFFIO_R5_G0_01N	V8	IO_170_N	41.1004	
R5	DIFFIO_R5_G0_02P_DQS	W9	IO_171_P	28.1311	
R5	DIFFIO_R5_G0_02N_DQS	W8	IO_171_N	27.3266	
R5	DIFFIO_R5_G0_03P	V7	IO_172_P	50.8076	
R5	DIFFIO_R5_G0_03N	V6	IO_172_N	51.3839	
R5	DIFFIO_R5_G0_04P	Y8	IO_173_P	44.8736	
R5	DIFFIO_R5_G0_04N	Y7	IO_173_N	45.4234	
R5	DIFFIO_R5_G0_05P	W6	IO_174_P	50.2178	
R5	DIFFIO_R5_G0_05N_VREF	Y6	IO_174_N	50.8556	
R5	DIFFIO_R5_G1_06P	W1	IO_175_P	81.0837	BANKR5_G1_DQS
R5	DIFFIO_R5_G1_06N	Y1	IO_175_N	81.4207	
R5	DIFFIO_R5_G1_07P	V2	IO_176_P	98.3151	
R5	DIFFIO_R5_G1_07N	V1	IO_176_N	98.9195	
R5	DIFFIO_R5_G1_08P_DQS	Y3	IO_177_P	75.5375	
R5	DIFFIO_R5_G1_08N_DQS	Y2	IO_177_N	75.7759	
R5	DIFFIO_R5_G1_09P	V3	IO_178_P	81.5723	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R5	DIFFIO_R5_G1_09N	W3	IO_178_N	81.8622	
R5	DIFFIO_R5_G1_10P_GSCLK	V4	IO_179_P	55.9327	
R5	DIFFIO_R5_G1_10N_GSCLK	W4	IO_179_N	56.1122	
R5	DIFFIO_R5_G1_11P_GMCLK	W5	IO_180_P	64.1412	
R5	DIFFIO_R5_G1_11N_GMCLK	Y5	IO_180_N	64.3977	
R5	DIFFIO_R5_G2_12P_GMCLK	AA5	IO_181_P	61.2910	BANKR5_G2_DQS
R5	DIFFIO_R5_G2_12N_GMCLK	AA4	IO_181_N	61.4696	
R5	DIFFIO_R5_G2_13P_GSCLK	AB5	IO_182_P	71.5238	
R5	DIFFIO_R5_G2_13N_GSCLK	AB4	IO_182_N	72.1529	
R5	DIFFIO_R5_G2_14P_DQS	AB2	IO_183_P	86.8251	
R5	DIFFIO_R5_G2_14N_DQS	AB1	IO_183_N	87.3885	
R5	DIFFIO_R5_G2_15P	AA3	IO_184_P	90.6771	
R5	DIFFIO_R5_G2_15N	AA2	IO_184_N	91.3477	
R5	DIFFIO_R5_G2_16P	AC2	IO_185_P	89.6629	
R5	DIFFIO_R5_G2_16N	AC1	IO_185_N	90.0014	
R5	DIFFIO_R5_G2_17P	AC4	IO_186_P	81.9282	
R5	DIFFIO_R5_G2_17N	AC3	IO_186_N	82.4083	
R5	DIFFIO_R5_G3_18P	AA8	IO_187_P	96.2775	BANKR5_G3_DQS
R5	DIFFIO_R5_G3_18N_VREF	AA7	IO_187_N	95.8916	
R5	DIFFIO_R5_G3_19P	AC7	IO_188_P	65.4212	
R5	DIFFIO_R5_G3_19N	AC6	IO_188_N	65.5989	
R5	DIFFIO_R5_G3_20P_DQS	AB7	IO_189_P	45.0278	
R5	DIFFIO_R5_G3_20N_DQS	AB6	IO_189_N	45.5990	
R5	DIFFIO_R5_G3_21P	AC9	IO_190_P	60.1979	
R5	DIFFIO_R5_G3_21N	AC8	IO_190_N	62.8780	
R5	DIFFIO_R5_G3_22P	AA10	IO_191_P	59.8192	
R5	DIFFIO_R5_G3_22N	AA9	IO_191_N	60.8862	
R5	DIFFIO_R5_G3_23P	AB10	IO_192_P	52.1872	
R5	DIFFIO_R5_G3_23N	AB9	IO_192_N	55.1577	
R5	SIO_R5_01	AB11		2.0135	
R6	SIO_R6_00	AC11		28.9480	
R6	DIFFIO_R6_G0_00P	AG1	IO_193_P	98.3912	BANKR6_G0_DQS
R6	DIFFIO_R6_G0_00N	AH1	IO_193_N	98.3967	
R6	DIFFIO_R6_G0_01P	AD1	IO_194_P	104.5474	
R6	DIFFIO_R6_G0_01N	AE1	IO_194_N	105.1775	
R6	DIFFIO_R6_G0_02P_DQS	AH2	IO_195_P	104.1754	
R6	DIFFIO_R6_G0_02N_DQS	AJ1	IO_195_N	104.6440	
R6	DIFFIO_R6_G0_03P	AE2	IO_196_P	108.2718	
R6	DIFFIO_R6_G0_03N	AF2	IO_196_N	108.1912	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R6	DIFFIO_R6_G0_04P	AF3	IO_197_P	87.5195	
R6	DIFFIO_R6_G0_04N	AG2	IO_197_N	87.4692	
R6	DIFFIO_R6_G0_05P	AH3	IO_198_P	128.4458	
R6	DIFFIO_R6_G0_05N_VREF	AJ3	IO_198_N	128.8448	
R6	DIFFIO_R6_G1_06P	AF4	IO_199_P	76.8488	BANKR6_G1_DQS
R6	DIFFIO_R6_G1_06N	AG4	IO_199_N	76.9053	
R6	DIFFIO_R6_G1_07P	AD5	IO_200_P	77.6380	
R6	DIFFIO_R6_G1_07N	AD4	IO_200_N	78.0165	
R6	DIFFIO_R6_G1_08P_DQS	AH4	IO_201_P	86.5230	
R6	DIFFIO_R6_G1_08N_DQS	AJ4	IO_201_N	86.7651	
R6	DIFFIO_R6_G1_09P	AD3	IO_202_P	88.8303	
R6	DIFFIO_R6_G1_09N	AE3	IO_202_N	89.4960	
R6	DIFFIO_R6_G1_10P_GSCLK	AG6	IO_203_P	75.3905	
R6	DIFFIO_R6_G1_10N_GSCLK	AG5	IO_203_N	75.8221	
R6	DIFFIO_R6_G1_11P_GMCLK	AE5	IO_204_P	75.1470	
R6	DIFFIO_R6_G1_11N_GMCLK	AF5	IO_204_N	75.3209	
R6	DIFFIO_R6_G2_12P_GMCLK	AD6	IO_205_P	52.8694	BANKR6_G2_DQS
R6	DIFFIO_R6_G2_12N_GMCLK	AE6	IO_205_N	52.8791	
R6	DIFFIO_R6_G2_13P_GSCLK	AF7	IO_206_P	71.5675	
R6	DIFFIO_R6_G2_13N_GSCLK	AG7	IO_206_N	71.5093	
R6	DIFFIO_R6_G2_14P_DQS	AD9	IO_207_P	59.8296	
R6	DIFFIO_R6_G2_14N_DQS	AD8	IO_207_N	60.3431	
R6	DIFFIO_R6_G2_15P	AE8	IO_208_P	55.1830	
R6	DIFFIO_R6_G2_15N	AE7	IO_208_N	54.9593	
R6	DIFFIO_R6_G2_16P	AH7	IO_209_P	71.1399	
R6	DIFFIO_R6_G2_16N	AH6	IO_209_N	70.0239	
R6	DIFFIO_R6_G2_17P	AF9	IO_210_P	57.8275	
R6	DIFFIO_R6_G2_17N	AF8	IO_210_N	57.8973	
R6	DIFFIO_R6_G3_18P	AH9	IO_211_P	80.3500	BANKR6_G3_DQS
R6	DIFFIO_R6_G3_18N_VREF	AH8	IO_211_N	79.1296	
R6	DIFFIO_R6_G3_19P	AF12	IO_212_P	80.4357	
R6	DIFFIO_R6_G3_19N	AG12	IO_212_N	81.4490	
R6	DIFFIO_R6_G3_20P_DQS	AG10	IO_213_P	51.9551	
R6	DIFFIO_R6_G3_20N_DQS	AG9	IO_213_N	52.3580	
R6	DIFFIO_R6_G3_21P	AD11	IO_214_P	58.7731	
R6	DIFFIO_R6_G3_21N	AE11	IO_214_N	59.0685	
R6	DIFFIO_R6_G3_22P	AG11	IO_215_P	58.2682	
R6	DIFFIO_R6_G3_22N	AH11	IO_215_N	57.8466	
R6	DIFFIO_R6_G3_23P	AD10	IO_216_P	40.0237	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R6	DIFFIO_R6_G3_23N	AE10	IO_216_N	40.6857	
R6	SIO_R6_01	AF10		38.2516	
R7	SIO_R7_00	AJ9		65.3764	
R7	DIFFIO_R7_G0_00P	AN1	IO_217_P	63.9393	BANKR7_G0_DQS
R7	DIFFIO_R7_G0_00N	AP1	IO_217_N	64.2100	
R7	DIFFIO_R7_G0_01P	AK2	IO_218_P	120.9729	
R7	DIFFIO_R7_G0_01N	AK1	IO_218_N	121.6065	
R7	DIFFIO_R7_G0_02P_DQS	AM2	IO_219_P	109.4156	
R7	DIFFIO_R7_G0_02N_DQS	AN2	IO_219_N	109.3346	
R7	DIFFIO_R7_G0_03P	AL2	IO_220_P	126.4148	
R7	DIFFIO_R7_G0_03N	AM1	IO_220_N	127.1959	
R7	DIFFIO_R7_G0_04P	AN3	IO_221_P	111.4911	
R7	DIFFIO_R7_G0_04N	AP3	IO_221_N	111.6056	
R7	DIFFIO_R7_G0_05P	AK3	IO_222_P	107.3154	
R7	DIFFIO_R7_G0_05N_VREF	AL3	IO_222_N	108.3905	
R7	DIFFIO_R7_G1_06P	AN4	IO_223_P	105.3397	BANKR7_G1_DQS
R7	DIFFIO_R7_G1_06N	AP4	IO_223_N	105.4798	
R7	DIFFIO_R7_G1_07P	AJ5	IO_224_P	86.3160	
R7	DIFFIO_R7_G1_07N	AK5	IO_224_N	86.4451	
R7	DIFFIO_R7_G1_08P_DQS	AP6	IO_225_P	102.3121	
R7	DIFFIO_R7_G1_08N_DQS	AP5	IO_225_N	101.7895	
R7	DIFFIO_R7_G1_09P	AL4	IO_226_P	103.5644	
R7	DIFFIO_R7_G1_09N	AM4	IO_226_N	103.6055	
R7	DIFFIO_R7_G1_10P_GSCLK	AL5	IO_227_P	82.1984	
R7	DIFFIO_R7_G1_10N_GSCLK	AM5	IO_227_N	83.6934	
R7	DIFFIO_R7_G1_11P_GMCLK	AJ6	IO_228_P	76.4717	
R7	DIFFIO_R7_G1_11N_GMCLK	AK6	IO_228_N	76.4700	
R7	DIFFIO_R7_G2_12P_GMCLK	AK7	IO_229_P	69.7744	BANKR7_G2_DQS
R7	DIFFIO_R7_G2_12N_GMCLK	AL7	IO_229_N	69.9660	
R7	DIFFIO_R7_G2_13P_GSCLK	AM7	IO_230_P	99.8852	
R7	DIFFIO_R7_G2_13N_GSCLK	AM6	IO_230_N	100.1428	
R7	DIFFIO_R7_G2_14P_DQS	AJ8	IO_231_P	58.9918	
R7	DIFFIO_R7_G2_14N_DQS	AK8	IO_231_N	59.1351	
R7	DIFFIO_R7_G2_15P	AN8	IO_232_P	97.2405	
R7	DIFFIO_R7_G2_15N	AP8	IO_232_N	97.3274	
R7	DIFFIO_R7_G2_16P	AN7	IO_233_P	91.9414	
R7	DIFFIO_R7_G2_16N	AN6	IO_233_N	92.3974	
R7	DIFFIO_R7_G2_17P	AN9	IO_234_P	92.4617	
R7	DIFFIO_R7_G2_17N	AP9	IO_234_N	92.7722	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R7	DIFFIO_R7_G3_18P	AJ10	IO_235_P	50.7793	BANKR7_G3_DQS
R7	DIFFIO_R7_G3_18N_VREF	AK10	IO_235_N	51.3729	
R7	DIFFIO_R7_G3_19P	AP11	IO_236_P	94.8506	
R7	DIFFIO_R7_G3_19N	AP10	IO_236_N	95.0379	
R7	DIFFIO_R7_G3_20P_DQS	AL9	IO_237_P	64.5797	
R7	DIFFIO_R7_G3_20N_DQS	AM9	IO_237_N	65.1912	
R7	DIFFIO_R7_G3_21P	AM11	IO_238_P	76.1441	
R7	DIFFIO_R7_G3_21N	AN11	IO_238_N	76.0906	
R7	DIFFIO_R7_G3_22P	AJ11	IO_239_P	44.7085	
R7	DIFFIO_R7_G3_22N	AK11	IO_239_N	45.3327	
R7	DIFFIO_R7_G3_23P	AL10	IO_240_P	68.9170	
R7	DIFFIO_R7_G3_23N	AM10	IO_240_N	69.4224	
R7	SIO_R7_01	AL8		74.7803	
	INIT_FLAG_N	V11		67.5734	
	CFG_DONE	P11		91.7846	
	RSTN	N11		94.4851	
	CFG_CLK	W11		64.7374	
	TCK	AE12		80.8653	
	TMS	AE13		81.9464	
	TDI	AE14		78.0237	
	TDO	AD13		92.5979	
	MODE_0	L22		51.7586	
	MODE_1	K22		57.1618	
	MODE_2	K21		60.3684	
	SCBV	M12		95.6893	
	VAADC_N	V17	IO_241_N		
	VAADC_P	U18	IO_241_P		
	VCCADC	T18			
	VREFADC_N	U17	IO_242_N		
	VREFADC_P	V18	IO_242_P		
	VSSADC	T17			
	TSDN	W17	IO_243_N	42.0887	
	TSDP	W18	IO_243_P	46.3090	
	VCCB	K13			
	VCCIOCFG	L13			
	VCCIOCFG	T11			
	NC1	F25		73.6566	
	NC2	E25		80.4540	
	HSSTRX0N_QL3	E21	IO_244_N	46.1406	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	HSSTRX0P_QL3	F21	IO_244_P	46.2105	
	HSSTRX1N_QL3	C20	IO_245_N	103.5958	
	HSSTRX1P_QL3	D20	IO_245_P	103.7807	
	HSSTRX2N_QL3	E19	IO_246_N	125.6540	
	HSSTRX2P_QL3	F19	IO_246_P	125.8628	
	HSSTRX3N_QL3	C18	IO_247_N	152.9268	
	HSSTRX3P_QL3	D18	IO_247_P	152.9196	
	HSSTTX0N_QL3	A23	IO_248_N	73.3394	
	HSSTTX0P_QL3	B23	IO_248_P	73.4814	
	HSSTTX1N_QL3	C22	IO_249_N	70.7550	
	HSSTTX1P_QL3	D22	IO_249_P	71.0088	
	HSSTTX2N_QL3	A21	IO_250_N	99.7216	
	HSSTTX2P_QL3	B21	IO_250_P	99.4398	
	HSSTTX3N_QL3	A19	IO_251_N	125.7455	
	HSSTTX3P_QL3	B19	IO_251_P	125.7173	
	HSSTREFCLK0P_QL3	H18	IO_252_P	37.3972	
	HSSTREFCLK0N_QL3	G18	IO_252_N	38.7211	
	HSSTREFCLK1N_QL3	G20	IO_253_N	47.1297	
	HSSTREFCLK1P_QL3	H20	IO_253_P	47.7480	
	HSSTRREF_QL3	G22		48.6120	
	HSSTRX0N_QR3	E13	IO_254_N	48.5561	
	HSSTRX0P_QR3	F13	IO_254_P	48.6401	
	HSSTRX1N_QR3	E15	IO_255_N	54.4930	
	HSSTRX1P_QR3	F15	IO_255_P	54.2124	
	HSSTRX2N_QR3	C16	IO_256_N	115.7209	
	HSSTRX2P_QR3	D16	IO_256_P	115.6983	
	HSSTRX3N_QR3	E17	IO_257_N	156.5306	
	HSSTRX3P_QR3	F17	IO_257_P	156.5862	
	HSSTTX0N_QR3	A13	IO_258_N	74.7326	
	HSSTTX0P_QR3	B13	IO_258_P	74.5563	
	HSSTTX1N_QR3	C14	IO_259_N	73.4706	
	HSSTTX1P_QR3	D14	IO_259_P	73.2796	
	HSSTTX2N_QR3	A15	IO_260_N	97.9489	
	HSSTTX2P_QR3	B15	IO_260_P	97.6667	
	HSSTTX3N_QR3	A17	IO_261_N	124.1523	
	HSSTTX3P_QR3	B17	IO_261_P	124.1072	
	HSSTREFCLK0N_QR3	G16	IO_262_N	43.9398	
	HSSTREFCLK0P_QR3	H16	IO_262_P	41.6814	
	HSSTREFCLK1P_QR3	H14	IO_263_P	47.7882	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	HSSTREFCLK1N_QR3	G14	IO_263_N	45.3637	
	HSSTRX0N_QL7	AM18	IO_264_N	152.5734	
	HSSTRX0P_QL7	AL18	IO_264_P	152.5167	
	HSSTRX1N_QL7	AK19	IO_265_N	125.1076	
	HSSTRX1P_QL7	AJ19	IO_265_P	125.1657	
	HSSTRX2N_QL7	AM20	IO_266_N	103.5314	
	HSSTRX2P_QL7	AL20	IO_266_P	103.4843	
	HSSTRX3N_QL7	AK21	IO_267_N	46.1255	
	HSSTRX3P_QL7	AJ21	IO_267_P	45.9551	
	HSSTTX0N_QL7	AP19	IO_268_N	125.4135	
	HSSTTX0P_QL7	AN19	IO_268_P	125.2077	
	HSSTTX1N_QL7	AP21	IO_269_N	99.5489	
	HSSTTX1P_QL7	AN21	IO_269_P	99.6536	
	HSSTTX2N_QL7	AM22	IO_270_N	70.7361	
	HSSTTX2P_QL7	AL22	IO_270_P	70.6908	
	HSSTTX3N_QL7	AP23	IO_271_N	73.4568	
	HSSTTX3P_QL7	AN23	IO_271_P	73.3509	
	HSSTREFCLK0P_QL7	AG20	IO_272_P	47.2547	
	HSSTREFCLK0N_QL7	AH20	IO_272_N	48.6360	
	HSSTREFCLK1N_QL7	AH18	IO_273_N	37.6151	
	HSSTREFCLK1P_QL7	AG18	IO_273_P	39.1363	
	HSSTRREF_QL7	AH22		48.1842	
	HSSTRX0N_QR7	AK17	IO_274_N	156.2460	
	HSSTRX0P_QR7	AJ17	IO_274_P	156.0954	
	HSSTRX1N_QR7	AM16	IO_275_N	115.4592	
	HSSTRX1P_QR7	AL16	IO_275_P	115.2993	
	HSSTRX2N_QR7	AK15	IO_276_N	54.5376	
	HSSTRX2P_QR7	AJ15	IO_276_P	54.5598	
	HSSTRX3N_QR7	AK13	IO_277_N	48.5826	
	HSSTRX3P_QR7	AJ13	IO_277_P	48.5189	
	HSSTTX0N_QR7	AP17	IO_278_N	122.0601	
	HSSTTX0P_QR7	AN17	IO_278_P	121.9780	
	HSSTTX1N_QR7	AP15	IO_279_N	98.2625	
	HSSTTX1P_QR7	AN15	IO_279_P	98.3243	
	HSSTTX2N_QR7	AM14	IO_280_N	73.4932	
	HSSTTX2P_QR7	AL14	IO_280_P	73.3369	
	HSSTTX3N_QR7	AP13	IO_281_N	75.1422	
	HSSTTX3P_QR7	AN13	IO_281_P	75.2332	
	HSSTREFCLK0N_QR7	AH14	IO_282_N	49.5202	

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	HSSTREFCLK0P_QR7	AG14	IO_282_P	48.0219	
	HSSTREFCLK1P_QR7	AG16	IO_283_P	43.4378	
	HSSTREFCLK1N_QR7	AH16	IO_283_N	41.0260	
	HSSTAVCC_G3	F14			
	HSSTAVCC_G3	F16			
	HSSTAVCC_G3	F18			
	HSSTAVCC_G3	F20			
	HSSTAVCC_G3	H15			
	HSSTAVCC_G3	H17			
	HSSTAVCC_G3	H19			
	HSSTAVCC_G3	H21			
	HSSTAVCCPLL_G3	B14			
	HSSTAVCCPLL_G3	B16			
	HSSTAVCCPLL_G3	B18			
	HSSTAVCCPLL_G3	B20			
	HSSTAVCCPLL_G3	B22			
	HSSTAVCCPLL_G3	D13			
	HSSTAVCCPLL_G3	D15			
	HSSTAVCCPLL_G3	D17			
	HSSTAVCCPLL_G3	D19			
	HSSTAVCCPLL_G3	D21			
	HSSTAVCCPLL_G3	F22			
	HSSTAVCC_G7	AG15			
	HSSTAVCC_G7	AG17			
	HSSTAVCC_G7	AG19			
	HSSTAVCC_G7	AG21			
	HSSTAVCC_G7	AJ14			
	HSSTAVCC_G7	AJ16			
	HSSTAVCC_G7	AJ18			
	HSSTAVCC_G7	AJ20			
	HSSTAVCCPLL_G7	AJ22			
	HSSTAVCCPLL_G7	AL13			
	HSSTAVCCPLL_G7	AL15			
	HSSTAVCCPLL_G7	AL17			
	HSSTAVCCPLL_G7	AL19			
	HSSTAVCCPLL_G7	AL21			
	HSSTAVCCPLL_G7	AN14			
	HSSTAVCCPLL_G7	AN16			
	HSSTAVCCPLL_G7	AN18			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	HSSTAVCCPLL_G7	AN20			
	HSSTAVCCPLL_G7	AN22			
	VCC	AA15			
	VCC	AA17			
	VCC	AA19			
	VCC	AB14			
	VCC	AB16			
	VCC	AB18			
	VCC	AC15			
	VCC	AC17			
	VCC	AC19			
	VCC	AD14			
	VCC	AD16			
	VCC	AD18			
	VCC	AD20			
	VCC	AD22			
	VCC	AE15			
	VCC	AE17			
	VCC	AE19			
	VCC	AE21			
	VCC	K14			
	VCC	K16			
	VCC	K18			
	VCC	K20			
	VCC	L15			
	VCC	L17			
	VCC	L19			
	VCC	L21			
	VCC	M14			
	VCC	M16			
	VCC	M18			
	VCC	N15			
	VCC	N17			
	VCC	N19			
	VCC	P14			
	VCC	P16			
	VCC	P18			
	VCC	R15			
	VCC	R17			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCC	R19			
	VCC	T14			
	VCC	T16			
	VCC	U15			
	VCC	U19			
	VCC	V14			
	VCC	V16			
	VCC	W15			
	VCC	W19			
	VCC	Y14			
	VCC	Y16			
	VCC	Y18			
	VCCA	M22			
	VCCA	N13			
	VCCA	N23			
	VCCA	P12			
	VCCA	P22			
	VCCA	R13			
	VCCA	R23			
	VCCA	T12			
	VCCA	T22			
	VCCA	U13			
	VCCA	U23			
	VCCA	V12			
	VCCA	V22			
	VCCA	W13			
	VCCA	W23			
	VCCA	Y12			
	VCCA	Y22			
	VCCA	AA13			
	VCCA	AA23			
	VCCA	AB12			
	VCCA	AB22			
	VCCA	AC13			
	VCCA	AC23			
	VCCA	AD12			
	VCC_DRM	M20			
	VCC_DRM	N21			
	VCC_DRM	P20			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCC_DRM	R21			
	VCC_DRM	T20			
	VCC_DRM	U21			
	VCC_DRM	V20			
	VCC_DRM	W21			
	VCC_DRM	Y20			
	VCC_DRM	AA21			
	VCC_DRM	AB20			
	VCC_DRM	AC21			
	VCCIO_L3	G33			
	VCCIO_L3	H30			
	VCCIO_L3	J27			
	VCCIO_L3	K24			
	VCCIO_L3	K34			
	VCCIO_L3	L31			
	VCCIO_L4	M28			
	VCCIO_L4	N25			
	VCCIO_L4	P32			
	VCCIO_L4	R29			
	VCCIO_L4	T26			
	VCCIO_L4	U33			
	VCCIO_L5	AA31			
	VCCIO_L5	AB28			
	VCCIO_L5	V30			
	VCCIO_L5	W27			
	VCCIO_L5	Y24			
	VCCIO_L5	Y34			
	VCCIO_L6	AC25			
	VCCIO_L6	AD32			
	VCCIO_L6	AE29			
	VCCIO_L6	AF26			
	VCCIO_L6	AG33			
	VCCIO_L6	AH30			
	VCCIO_L7	AJ27			
	VCCIO_L7	AK34			
	VCCIO_L7	AL31			
	VCCIO_L7	AM28			
	VCCIO_L7	AN25			
	VCCIO_L7	AP32			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCCIO_R3	F1			
	VCCIO_R3	G8			
	VCCIO_R3	H5			
	VCCIO_R3	J2			
	VCCIO_R3	J12			
	VCCIO_R3	K9			
	VCCIO_R3	L6			
	VCCIO_R4	M3			
	VCCIO_R4	N10			
	VCCIO_R4	P7			
	VCCIO_R4	R4			
	VCCIO_R4	T1			
	VCCIO_R4	U8			
	VCCIO_R5	AA6			
	VCCIO_R5	AB3			
	VCCIO_R5	AC10			
	VCCIO_R5	V5			
	VCCIO_R5	W2			
	VCCIO_R5	Y9			
	VCCIO_R6	AD7			
	VCCIO_R6	AE4			
	VCCIO_R6	AF1			
	VCCIO_R6	AF11			
	VCCIO_R6	AG8			
	VCCIO_R6	AH5			
	VCCIO_R7	AJ2			
	VCCIO_R7	AK9			
	VCCIO_R7	AL6			
	VCCIO_R7	AM3			
	VCCIO_R7	AN10			
	VCCIO_R7	AP7			
	VSS	A1			
	VSS	A11			
	VSS	A12			
	VSS	A14			
	VSS	A16			
	VSS	A18			
	VSS	A20			
	VSS	A22			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	A24			
	VSS	A26			
	VSS	AA1			
	VSS	AA11			
	VSS	AA12			
	VSS	AA14			
	VSS	AA16			
	VSS	AA18			
	VSS	AA20			
	VSS	AA22			
	VSS	AA26			
	VSS	AB8			
	VSS	AB13			
	VSS	AB15			
	VSS	AB17			
	VSS	AB19			
	VSS	AB21			
	VSS	AB23			
	VSS	AB33			
	VSS	AC5			
	VSS	AC12			
	VSS	AC14			
	VSS	AC16			
	VSS	AC18			
	VSS	AC20			
	VSS	AC22			
	VSS	AC30			
	VSS	AD2			
	VSS	AD15			
	VSS	AD17			
	VSS	AD19			
	VSS	AD21			
	VSS	AD27			
	VSS	AE9			
	VSS	AE16			
	VSS	AE18			
	VSS	AE20			
	VSS	AE22			
	VSS	AE24			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	AE34			
	VSS	AF6			
	VSS	AF13			
	VSS	AF14			
	VSS	AF15			
	VSS	AF16			
	VSS	AF17			
	VSS	AF18			
	VSS	AF19			
	VSS	AF20			
	VSS	AF21			
	VSS	AF22			
	VSS	AF31			
	VSS	AG3			
	VSS	AG13			
	VSS	AG22			
	VSS	AG23			
	VSS	AG28			
	VSS	AH10			
	VSS	AH12			
	VSS	AH13			
	VSS	AH15			
	VSS	AH17			
	VSS	AH19			
	VSS	AH21			
	VSS	AH23			
	VSS	AH25			
	VSS	AJ7			
	VSS	AJ12			
	VSS	AJ23			
	VSS	AJ32			
	VSS	AK4			
	VSS	AK12			
	VSS	AK14			
	VSS	AK16			
	VSS	AK18			
	VSS	AK20			
	VSS	AK22			
	VSS	AK23			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	AK24			
	VSS	AK29			
	VSS	AL1			
	VSS	AL11			
	VSS	AL12			
	VSS	AL23			
	VSS	AL26			
	VSS	AM8			
	VSS	AM12			
	VSS	AM13			
	VSS	AM15			
	VSS	AM17			
	VSS	AM19			
	VSS	AM21			
	VSS	AM23			
	VSS	AM24			
	VSS	AM33			
	VSS	AN5			
	VSS	AN12			
	VSS	AN24			
	VSS	AN30			
	VSS	AP2			
	VSS	AP12			
	VSS	AP14			
	VSS	AP16			
	VSS	AP18			
	VSS	AP20			
	VSS	AP22			
	VSS	AP24			
	VSS	AP27			
	VSS	B8			
	VSS	B12			
	VSS	B24			
	VSS	B33			
	VSS	C5			
	VSS	C12			
	VSS	C13			
	VSS	C15			
	VSS	C17			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	C19			
	VSS	C21			
	VSS	C23			
	VSS	C24			
	VSS	C30			
	VSS	D2			
	VSS	D12			
	VSS	D23			
	VSS	D27			
	VSS	E9			
	VSS	E12			
	VSS	E14			
	VSS	E16			
	VSS	E18			
	VSS	E20			
	VSS	E22			
	VSS	E23			
	VSS	E24			
	VSS	E34			
	VSS	F6			
	VSS	F12			
	VSS	F23			
	VSS	F31			
	VSS	G3			
	VSS	G12			
	VSS	G13			
	VSS	G15			
	VSS	G17			
	VSS	G19			
	VSS	G21			
	VSS	G23			
	VSS	G28			
	VSS	H10			
	VSS	H13			
	VSS	H22			
	VSS	H23			
	VSS	H25			
	VSS	J7			
	VSS	J13			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	J14			
	VSS	J15			
	VSS	J16			
	VSS	J17			
	VSS	J18			
	VSS	J19			
	VSS	J20			
	VSS	J21			
	VSS	J22			
	VSS	J32			
	VSS	K4			
	VSS	K15			
	VSS	K17			
	VSS	K19			
	VSS	K29			
	VSS	L1			
	VSS	L11			
	VSS	L14			
	VSS	L16			
	VSS	L18			
	VSS	L20			
	VSS	L26			
	VSS	M8			
	VSS	M13			
	VSS	M15			
	VSS	M17			
	VSS	M19			
	VSS	M21			
	VSS	M23			
	VSS	M33			
	VSS	N5			
	VSS	N12			
	VSS	N14			
	VSS	N16			
	VSS	N18			
	VSS	N20			
	VSS	N22			
	VSS	N30			
	VSS	P2			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	P13			
	VSS	P15			
	VSS	P17			
	VSS	P19			
	VSS	P21			
	VSS	P23			
	VSS	P27			
	VSS	R9			
	VSS	R12			
	VSS	R14			
	VSS	R16			
	VSS	R18			
	VSS	R20			
	VSS	R22			
	VSS	R24			
	VSS	R34			
	VSS	T6			
	VSS	T13			
	VSS	T15			
	VSS	T19			
	VSS	T21			
	VSS	T23			
	VSS	T31			
	VSS	U3			
	VSS	U12			
	VSS	U14			
	VSS	U16			
	VSS	U20			
	VSS	U22			
	VSS	U28			
	VSS	V10			
	VSS	V13			
	VSS	V15			
	VSS	V19			
	VSS	V21			
	VSS	V23			
	VSS	V25			
	VSS	W7			
	VSS	W12			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	W14			
	VSS	W16			
	VSS	W20			
	VSS	W22			
	VSS	W32			
	VSS	Y4			
	VSS	Y13			
	VSS	Y15			
	VSS	Y17			
	VSS	Y19			
	VSS	Y21			
	VSS	Y23			
	VSS	Y29			
	<DUMMY_NET>	A2			
	<DUMMY_NET>	A3			
	<DUMMY_NET>	A4			
	<DUMMY_NET>	A5			
	<DUMMY_NET>	A6			
	<DUMMY_NET>	A7			
	<DUMMY_NET>	A8			
	<DUMMY_NET>	A9			
	<DUMMY_NET>	A10			
	<DUMMY_NET>	A25			
	<DUMMY_NET>	A27			
	<DUMMY_NET>	A28			
	<DUMMY_NET>	A29			
	<DUMMY_NET>	A30			
	<DUMMY_NET>	A31			
	<DUMMY_NET>	A32			
	<DUMMY_NET>	A33			
	<DUMMY_NET>	A34			
	<DUMMY_NET>	B1			
	<DUMMY_NET>	B2			
	<DUMMY_NET>	B3			
	<DUMMY_NET>	B4			
	<DUMMY_NET>	B5			
	<DUMMY_NET>	B6			
	<DUMMY_NET>	B7			
	<DUMMY_NET>	B9			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	<DUMMY_NET>	B10			
	<DUMMY_NET>	B11			
	<DUMMY_NET>	B25			
	<DUMMY_NET>	B26			
	<DUMMY_NET>	B27			
	<DUMMY_NET>	B28			
	<DUMMY_NET>	B29			
	<DUMMY_NET>	B30			
	<DUMMY_NET>	B31			
	<DUMMY_NET>	B32			
	<DUMMY_NET>	B34			
	<DUMMY_NET>	C1			
	<DUMMY_NET>	C2			
	<DUMMY_NET>	C3			
	<DUMMY_NET>	C4			
	<DUMMY_NET>	C6			
	<DUMMY_NET>	C7			
	<DUMMY_NET>	C8			
	<DUMMY_NET>	C9			
	<DUMMY_NET>	C10			
	<DUMMY_NET>	C11			
	<DUMMY_NET>	C25			
	<DUMMY_NET>	C26			
	<DUMMY_NET>	C27			
	<DUMMY_NET>	C28			
	<DUMMY_NET>	C29			
	<DUMMY_NET>	C31			
	<DUMMY_NET>	C32			
	<DUMMY_NET>	C33			
	<DUMMY_NET>	C34			
	<DUMMY_NET>	D1			
	<DUMMY_NET>	D3			
	<DUMMY_NET>	D4			
	<DUMMY_NET>	D5			
	<DUMMY_NET>	D6			
	<DUMMY_NET>	D7			
	<DUMMY_NET>	D8			
	<DUMMY_NET>	D9			
	<DUMMY_NET>	D10			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	<DUMMY_NET>	D11			
	<DUMMY_NET>	D24			
	<DUMMY_NET>	D25			
	<DUMMY_NET>	D26			
	<DUMMY_NET>	D28			
	<DUMMY_NET>	D29			
	<DUMMY_NET>	D30			
	<DUMMY_NET>	D31			
	<DUMMY_NET>	D32			
	<DUMMY_NET>	D33			
	<DUMMY_NET>	D34			
	<DUMMY_NET>	E1			
	<DUMMY_NET>	E2			
	<DUMMY_NET>	E3			
	<DUMMY_NET>	E4			
	<DUMMY_NET>	E5			
	<DUMMY_NET>	E6			
	<DUMMY_NET>	E7			
	<DUMMY_NET>	E8			
	<DUMMY_NET>	E10			
	<DUMMY_NET>	E11			
	<DUMMY_NET>	E26			
	<DUMMY_NET>	E27			
	<DUMMY_NET>	E28			
	<DUMMY_NET>	E29			
	<DUMMY_NET>	E30			
	<DUMMY_NET>	E31			
	<DUMMY_NET>	E32			
	<DUMMY_NET>	E33			
	<DUMMY_NET>	F4			
	<DUMMY_NET>	F5			
	<DUMMY_NET>	F7			
	<DUMMY_NET>	F8			
	<DUMMY_NET>	F9			
	<DUMMY_NET>	F10			
	<DUMMY_NET>	F11			
	<DUMMY_NET>	F24			
	<DUMMY_NET>	F26			
	<DUMMY_NET>	F27			

Bank Name	Pin Name (Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	<DUMMY_NET>	F28			
	<DUMMY_NET>	F29			
	<DUMMY_NET>	F30			
	<DUMMY_NET>	F32			
	<DUMMY_NET>	F33			
	<DUMMY_NET>	F34			

2.2.2 Thermal Resistance

Table 2-2 Thermal Resistance

θJA(℃/W) (Flow: 0m/s)	θJB(℃/W)	θJC(℃/W)	θJA(℃/W) (Flow: 1m/s)	θJA(℃/W) (Flow: 2m/s)
8.2	3.7	0.18	6.8	6.1

2.2.3 Pressure Value

1. Short term pressure (within 5 minutes): 100g/ball, 1156 balls, short term pressure can meet 115.6kg.
2. Long term pressure: 30g/ball, 1156 balls, long term pressure can meet 34.68kg.

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