PK02003_PGL12G_FBG256

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.4	09.10.2020	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

PGL12G_FBG256 products are packaged with a Wire Bond Ball Grid Array (BGA). Package size: 17x17mm; Number of balls: 256; Ball pitch: 1.0mm; Maximum package thickness: 1.43mm

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Values

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
D	16.9	17.0	17.1	A	1.23	1.33	1.43
D1	n/a	15.0	n/a	A1	0.32	0.37	0.42
E	16.9	17.0	17.1	A2	0.91	0.96	1.01
E1	n/a	15.0	n/a	c	0.22	0.26	0.3
b	0.45	0.5	0.55	e	n/a	1.0	n/a

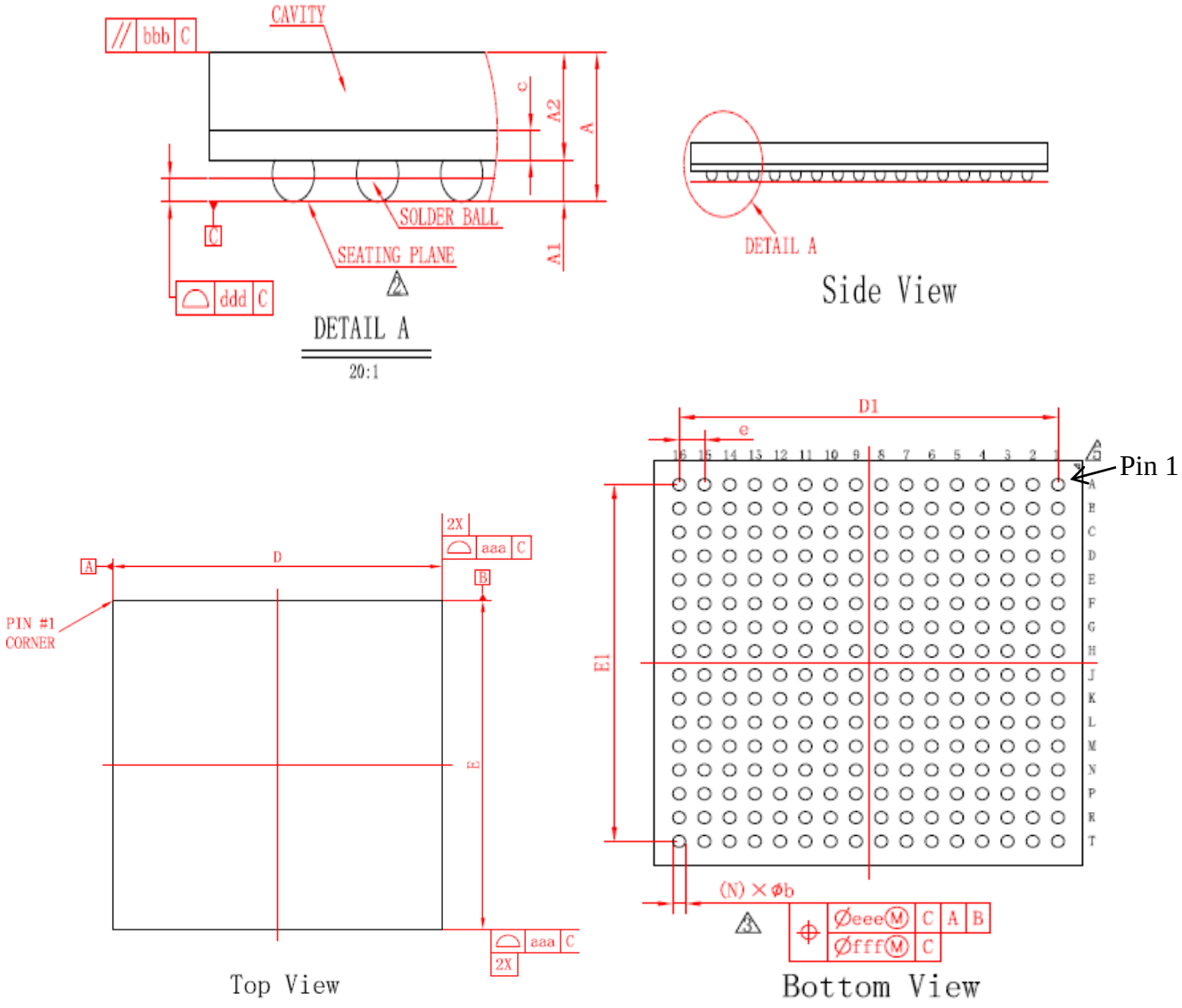


Figure 2-1 Package Outline Dimension (POD)

Note: PIN #1 indicates the position of the first pin

2.2 Pin Description

Table 2-2 Product Pin Definitions

PIN name	PIN type	PIN description
General PIN		
DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]	input/output	All general IOs are marked as DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]. DIFFIO: indicates that all general IOs support differential input/output, such as LVDS; [L0, L1, L2, R0, R1, R2]: indicates BANK names [0…n]: indicates the unique differential pair number in the BANK; [N, P]: N indicates the negative end of the differential pair and P represents the positive end.
Multiplexed Pin		
DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]		Multiplexed pins are marked as

PIN name	PIN type	PIN description
_[N,P]/XXX		DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]/XXX, where XXX indicates one or more of the functions described below. When the multiplexed pin is not used for special applications, it can serve as a general IO
--Configuration Pin		
MODE_2, MODE_1, MODE_0	input	They are used for configuration mode selection during configuration, as follows: 000: JTAG 001: Master SPI (X1, X2, X4, X8) 010: Master BPI (X8, X16) 011: Slave Serial (X1) 100: Slave Parallel (X8, X16, X32) 101: Slave SPI (X1) 111: Internal Master SPI (X1, X2, X4)
INIT_FLAG_N	Bidirectional (open-drain)	When the FPGA powers up completion during configuration, the pin is driven to a low level. Once the FPGA completes initialization, the pin is released. During configuration, this pin serves as an output for the configuration error indication state. During the configuration or initialization process, this pin can also accept an external low-level input to indicate an error or delay the configuration.
CFG_CLK	input/output	Configuration Clock Pin. In the slave mode, the pin serves as a clock input to obtain configuration data from external sources; In the master mode, the pin serves as a clock output to obtain configuration data from external sources;
D[31, 30…1, 0]	I input/output	32-bit configuration data bus input/output pins: (1) In the Master SPI X1 configuration mode, pin D[0], as command output, is connected to the data input of the SPI flash, and pin D[1], as data input, is connected to the data output of the SPI flash. (2) In the Master SPI X2 configuration mode, pins D[1:0] serve as the data bus. (3) In the Master SPI X4 configuration mode, pins D[3:0] serve as the data bus. (4) In the Master SPI X8 configuration mode, pins D[3:0] serve as the data bus for the first SPI FLASH, and pins D[7:4] serve as the data bus for the second SPI FLASH. (5) In the Slave Serial configuration mode, pin D[1] serves as the data bus. (6) In the Slave SPI configuration mode, pin D[0] is for the master device output and slave device input, pin D[1] is for the master device input and slave device output, and pin D[3] is for chip hold. (7) In the Master BPI configuration X8 asynchronous mode, pins D[7:0] serve as an 8-bit data bus. (8) In the Master BPI configuration X16 asynchronous/synchronous mode, pins D[15:0] serve as a 16-bit data bus. (9) In the Slave Parallel X8 configuration mode, pins D[7:0] are an 8-bit data bus. (10) In the Slave Parallel X16 configuration mode, pins D[15:0] are a 16-bit data bus. (11) In the Slave Parallel X32 configuration mode, pins D[31:0] are a 32-bit data bus.
CS_N	input	Multi-function Configuration Pin. for chip select input. Active low. (1) When it is low level, this pin enables the Slave Parallel mode configuration interface. (2) In other configuration modes, this pin is high-z. (3) To make this pin continue playing its configuration function after configuration is complete, users need to set the configuration register to preserve its configuration function.

PIN name	PIN type	PIN description
RWSEL	input	Multi-function Configuration Pin. For selecting the read/write input in the Slave Parallel configuration mode (high for read and low for write). (1) When it is high level, the Slave Parallel configuration mode reads data from the data bus; (2) When it is low level, the Slave Parallel configuration mode writes data to the data bus; (3) Read and write can be switched only when CS_N is high level. (4) To make this pin continue playing its configuration function after configuration is complete, users need to set the configuration register to preserve its configuration function. (5) In other configuration modes, this pin is high-z.
BUSY	output	Multi-function Configuration Pin. (1) During readback in the Slave Parallel mode, a high level output indicates that the data read from the bus is invalid. (2)To make this pin continue playing its configuration function in the user mode, users need to set the configuration register to preserve its configuration function. (3) In other configuration modes, this pin is in the high-z state.
CSO_DOUT	output	Multi-function Configuration Pin. Needed for cascade. (1) In the Master SPI and X1 mode, this pin serves as cascaded data output; (2) In the Slave Serial configuration mode, this pin serves as cascaded data output; (3) In the Slave Parallel configuration mode, this pin serves as a chip select signal output;
FCS_N	output	Multi-function configuration pin, used for the external Master SPI configuration mode. (1) In the Master SPI mode, this pin outputs a chip select signal to external flash , active-low
VS1, VS0	input	Multi-function configuration pins, used in the Master SPI or internal Master SPI mode. (1) It is used for selecting the bitstream version: 00 for the first set of bitstreams, 01 for the second set, 10 for the third set, 11 for the fourth set; (2) Enable the internal pull-down resistors during configuration.
IO_STATUS_C	input	Multi-function pin, used for inputting signals and controlling the state of all general IOs during the configuration process. (1) "1" keeps all general IOs in a pull-up state during configuration. (2) "0" keeps all general IOs in a tri-state during configuration.
ADR[25:0]	output	Multi-function configuration pins, used for outputting addresses in the BPI configuration mode.
BFOE_N	output	Multi-function configuration pin , used for providing a low-level output enable control signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, this PIN should be connected to the flash's output enable input and to VCCIO via a 4.7K resistor.
BADRVO_N	output	Multi-function configuration pin, used for providing a low-level address valid control signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, if the external FLASH supports address valid signal input, then this pin should be connected to the FLASH's address valid input pin and to VCCIO via a 4.7K resistor. If the external flash does not support address valid signal input, then there is no need to connect this PIN.
BFWE_N	output	Multi-function configuration pin, used for providing a low-level write enable signal for parallel NOR FLASH in the BPI configuration

PIN name	PIN type	PIN description
		mode. (1) In the BPI configuration mode, this pin should be connected to the flash's write enable input and to VCCIO via a 4.7K resistor;
BFCE_N	output	Multi-function configuration pin, used for providing a low-level chip select control signal for parallel NOR FLASH in the BPI configuration mode; (1) In the BPI configuration mode, this pin should be connected to the flash's chip select input and to VCCIO via a 4.7K resistor.
FCS2_N	output	Multi-function configuration pin, used for the external Master SPI X8 configuration mode. (1) In the Master SPI X8 mode, this pin outputs a chip select signal to external flash , active-low.. The pin should be connected to VCCIO via an external pull-up resistor not more than 4.7K.
ECCLKIN	input	Multi-function configuration pin, used for inputting signals and serves as clock input for the Master configuration mode.
-- Clock, PLL, Crystal Oscillator Multi-function Pin		
CLK[0,1,2,3]_[L0,L1,L2,R0,R1,R2]	input	Dedicated global clock input pins, 4 pins for each bank
DIFFCLK[0,1]_[L0,L1,L2,R0,R1,R2]_[N,P]	input	Dedicated global differential clock input pins, 2 pairs for each bank
PLL[0,1,2,…10]_CLKOUT_[P,N]	output	Direct selection of PLL[0, 1, …, 19] output to these pins are possible
PLL[0,1,2,…10]_CLKIN[0,1,2,3]	input	Optional PLL input, PLL can select directly the input clock from these pins
PLL[0,1,2,…10]_CLKFB_[P,N]	input	Optional PLL feedback clock input, PLL can input external feedback clock from these pins
XTALA_[L0,L1,L2,R0,R1,R2]	input	Dedicated external crystal input at port A. Input for the on-die inverter, 1 pin for each bank
XTALB_[L0,L1,L2,R0,R1,R2]	output	Dedicated external crystal output at port B. Output for the on-die inverter, 1 pin for each bank
-- External Memory Interface Pin		
DQS[0,1,2][#]_[L0,L1,L2,R0,R1,R2]	input/output	Used to connect to the DQS/DQS# signal pins of external memory
DQ[0,1,2]_[L0,L1,L2,R0,R1,R2]	input/output	Can connect to the DQ signal pins of external memory
--HMEMC Memory Interface Pin		
[R,L]_A[0,..,15]	output	DDR memory address
[R,L]_CS_N	output	DDR memory chip selection signal, active-low, depends on whether the memory is in use.
[R,L]_RAS_N	output	RAS, active-low
[R,L]_CAS_N	output	CAS, active-low
[R,L]_WE_N	output	Write enable, active-low
[R,L]_BA[0,1,2]	output	DDR BANK address
[R,L]_ODT	output	ODT, on-die terminal
[R,L]_CK	output	P side of DDR memory
[R,L]_CK_N	output	N side of DDR memory
[R,L]_CKE	output	DDR memory clock enable signal, active-high
[R,L]_RESET_N	output	DDR memory reset, active-low

PIN name	PIN type	PIN description
[R,L]_DML	output	Write data mask signals of DQ0-DQ7
[R,L]_DQSL	input/output	DQS signals related to DQ0-DQ7
[R,L]_DQSL_N	input/output	DQS# signals related to DQ0-DQ7
[R,L]_DQ[0,…,15]	input/output	Memory data bus
[R,L]_DMU	output	Write data mask signals of DQ8-DQ15
[R,L]_DQSU	input/output	DQS signals related to DQ8-DQ15
[R,L]_DQSU_N	input/output	DQS# signals related to DQ8-DQ15
[R,L]_DQSL_GATE_IN	input	DQS gate window signal feedback (low bit) after compensating for read command path delay
[R,L]_DQSL_GATE_OUT	output	DQS gate window signal output (low bit) after compensating for read command path delay
[R,L]_DQSU_GATE_IN	input	DQS gate window signal feedback (high bit) after compensating for read command path delay
[R,L]_DQSU_GATE_OUT	output	DQS gate window signal output (high bit) after compensating for read command path delay
--Reference Pin		
RRP_[L0,L1,L2,R0,R1,R2]	input	External reference resistor pins, one for each bank. Provides a reference resistor to the power supply for on-die terminal resistor adjustment.
RRN_[L0,L1,L2,R0,R1,R2]	input	External reference resistor pins, one for each bank. Provides a reference resistor to the ground for on-die terminal resistor adjustment.
VREF_[L0,L1,L2,R0,R1,R2]	input	External reference voltage pins, one for each bank. Provides reference voltage input for each BANK
--ADC Pin		
VAUX[9,8,7,..0]	input	Input analog signals
Dedicated Pin		
--Configuration Pin, JTAG Pin		
CFG_DONE	Bidirectional (open-drain)	Dedicated pin for configuration state. Serves as a status output, driven low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.
RST_N	input	Dedicated configuration input pin, internally weak pull-up, for restarting the configuration process, active-low. It is recommended that users externally pull up the RST_N with a resistor when using this pin. When this pin is low level, the FPGA enters a reset state, and all IOs are in the high-z state.
TCK	input	Dedicated JTAG test clock input pin
TMS	input	Dedicated JTAG test mode selection input pin
TDI	input	Dedicated JTAG test data input pin.
TDO	output	Dedicated JTAG test data output pin.

PIN name	PIN type	PIN description
--Reference Pin		
REXT	input	Dedicated external high-precision resistor pin, with a resistance of 10k and an accuracy of 1%. Provides resistance for the bandgap.
--ADC Pin		
VA[1,0]	input	Dedicated analog input signals
VREF_EXT	input	Dedicated external reference 2.5V voltage.
Power Pin, Ground Pin		
VCC	POWER	Core power, 1.1V. Power supply for core logic
VCCAUX	POWER	3.3V auxiliary power supply for IOB, LDO, and other modules
VDDIO[L0,L1,L2,R0,R1,R2]	POWER	IO BANK power, the banks on the left are BANKL0, BANKL1, BANKL2, and so on from top to down; the banks on the right side are BANKR0, BANKR1, BANKR2, and so on from top to down
VCCAUX_A	POWER	Power supply for ADC, BANDGAP, and POR
VSS	GROUND	GND relative to VCC&VCCAUX
VSSA	GROUND	GND relative to VCCAUX_A
VDDEFUSE	POWER	Efuse programming voltage
VDDIOCFG	POWER	BANKCFG power supply

Note: The user IO count for PGL12G_FBG256 products is 160.

2.2.1 Pinout Diagram

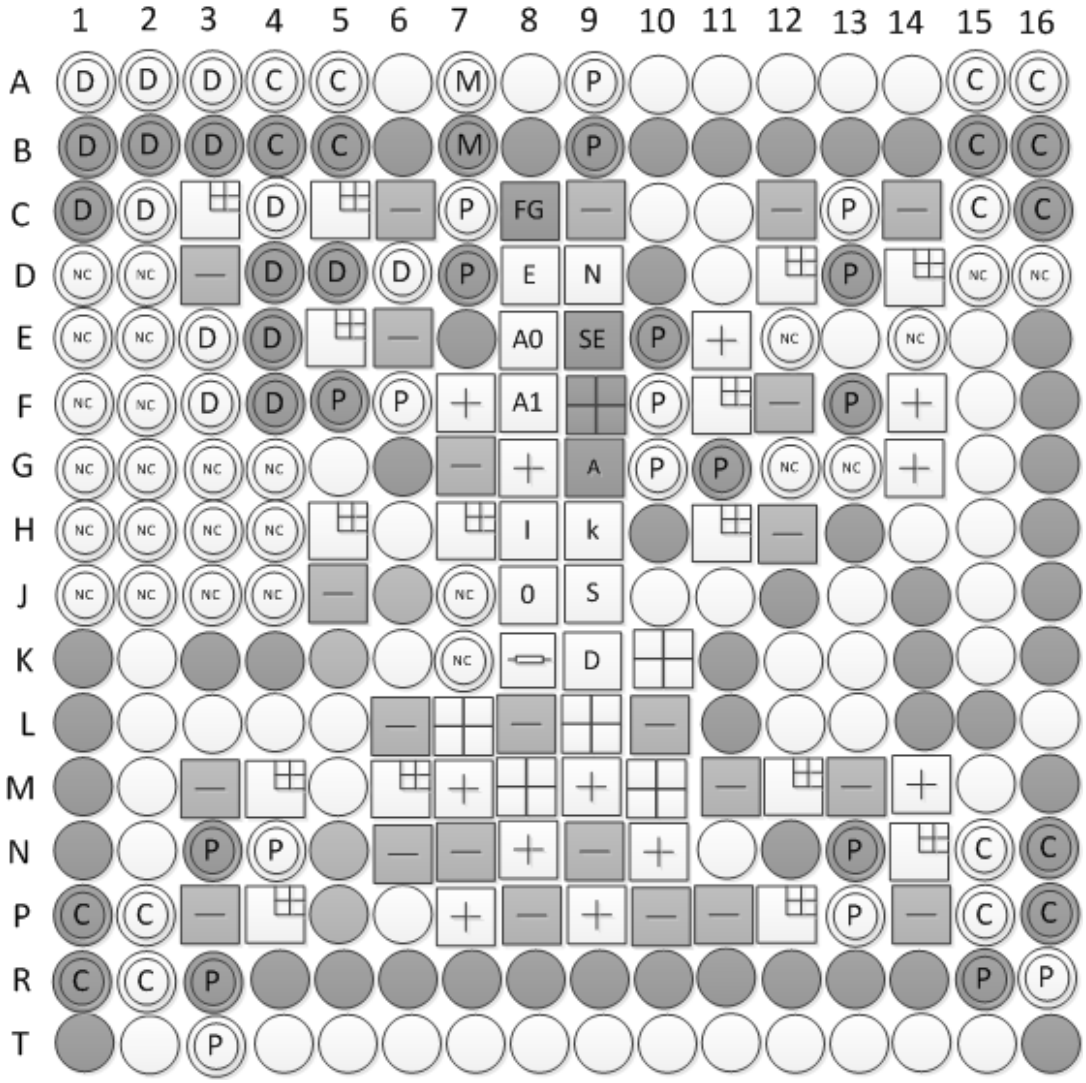
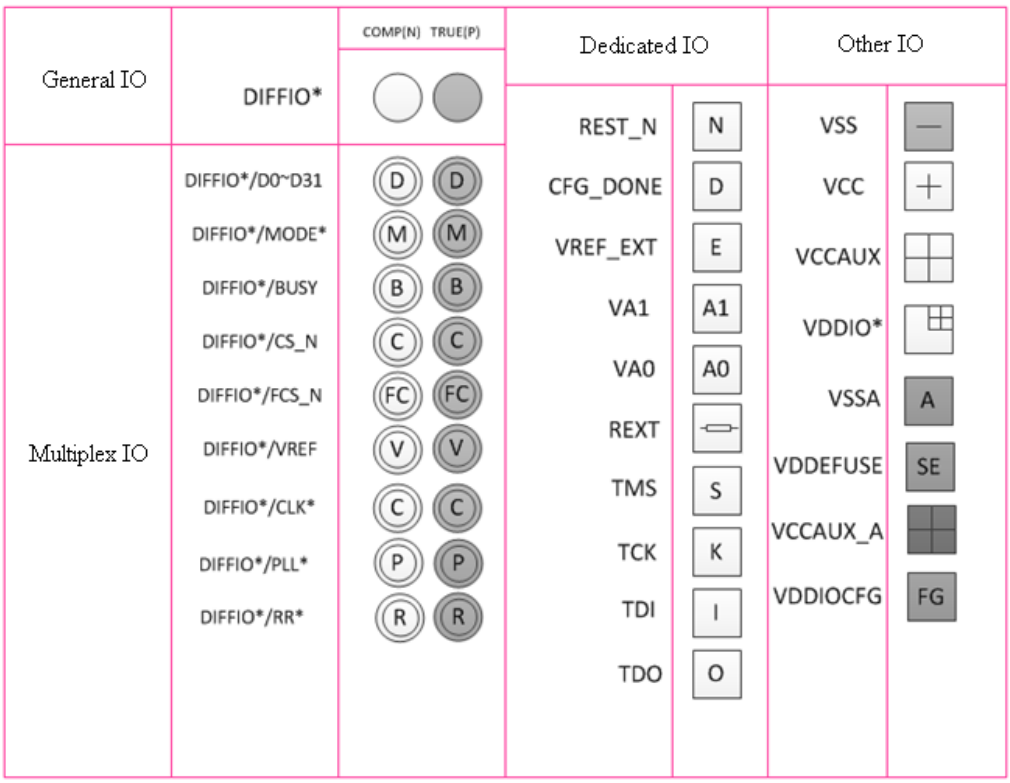


Figure 2-1 Pinout Diagram

Note: The Pinout symbols have the following meanings:


General IO
DIFFIO*
COMP(N) TRUE(P)
Dedicated IO
Other IO
Multiplex IO
DIFFIO*/D0~D31
DIFFIO*/MODE*
DIFFIO*/BUSY
DIFFIO*/CS_N
DIFFIO*/FCS_N
DIFFIO*/VREF
DIFFIO*/CLK*
DIFFIO*/PLL*
DIFFIO*/RR*
REST_N
CFG_DONE
VREF_EXT
VA1
VA0
REXT
TMS
TCK
TDI
TDO
N
D
E
A1
A0
S
K
I
O
VSS
VCC
VCCAUX
VDDIO*
VSSA
VDDEFUSE
VCCAUX_A
VDDIOCFG
A
SE
FG

2.2.2 IO Banks

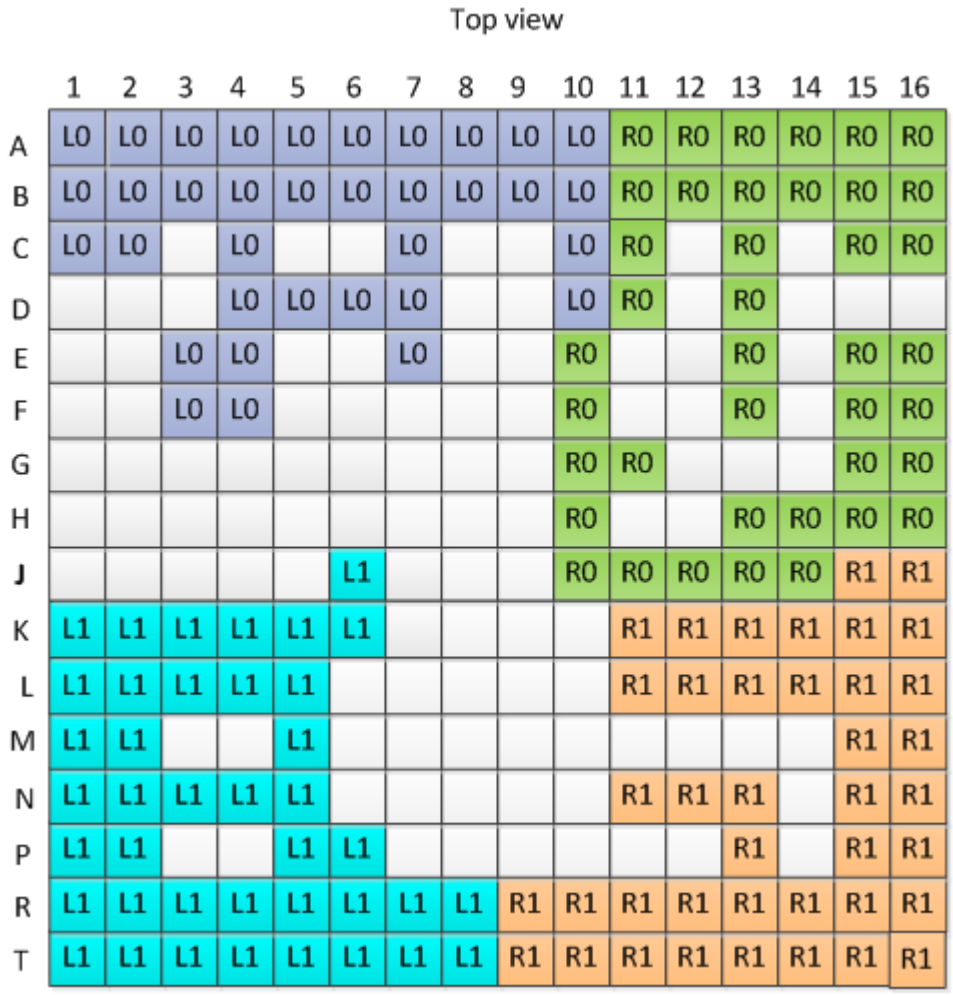


Figure 2-2 IO Banks

2.2.3 Power and GND Placement

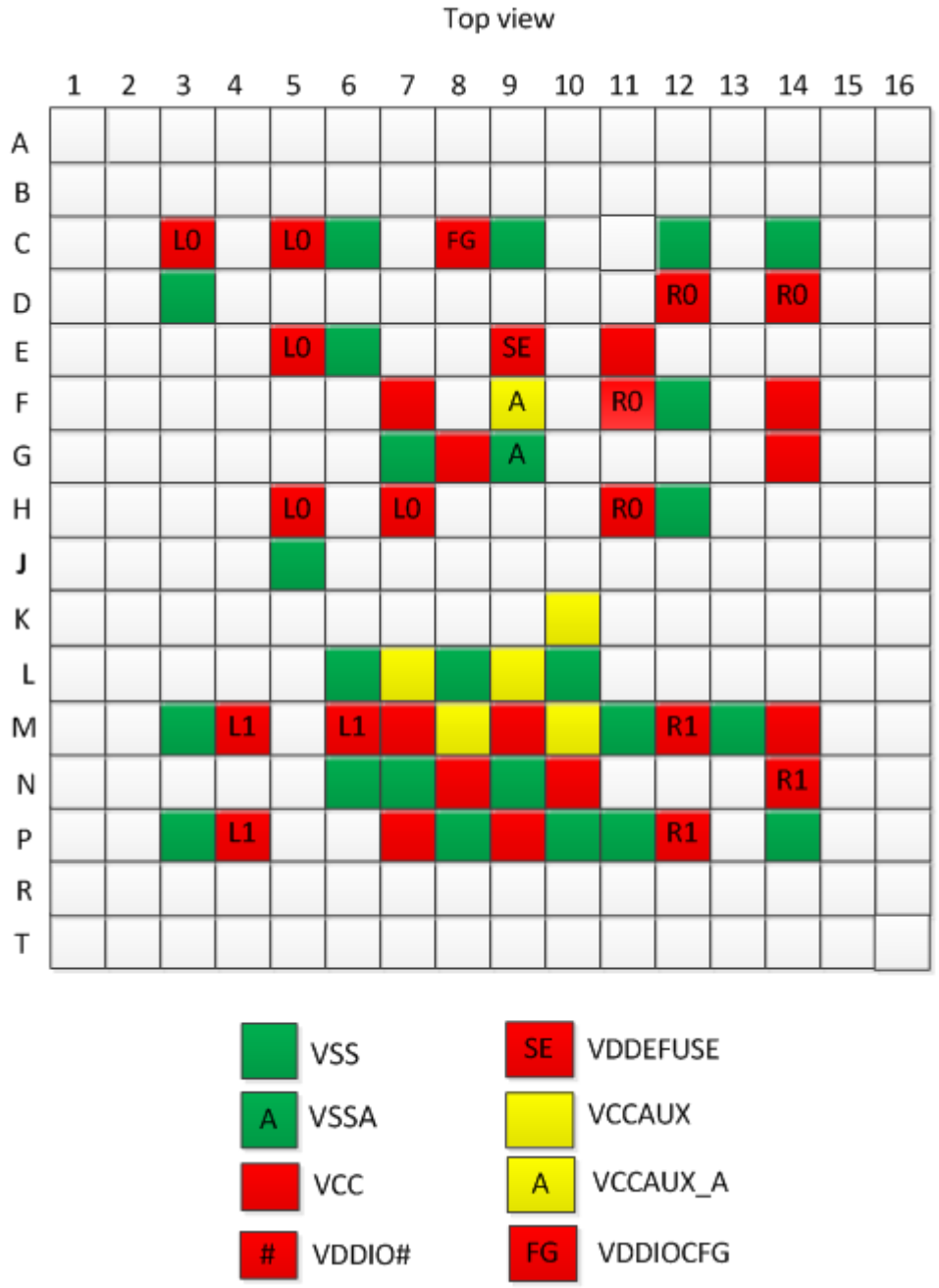


Figure 2-3 Power and GND Placement

2.2.4 Ball Name List

Table 2-3 Ball Name List

Bank Name	Ball Name (Function Name)	Ball Number	Time Delay (ps)	DQS Group
BANKCFG	RST_N	D9		
BANKCFG	CFG_DONE	K9		
BANKCFG	TCK	H9		
BANKCFG	TMS	J9		
BANKCFG	TDI	H8		
BANKCFG	TDO	J8		
BANKCFG	VREF_EXT	D8		
BANKCFG	VA0	E8		
BANKCFG	VA1	F8		
BANKCFG	REXT	K8		
BANKL0	DIFFIO_L0_0_P/BUSY	E7	40.45	DQ0_L0
BANKL0	DIFFIO_L0_0_N	F6	38.15	DQ0_L0
BANKL0	DIFFIO_L0_1_P/VAUX9	G6	31.23	DQ0_L0
BANKL0	DIFFIO_L0_1_N/VAUX8	H6	31.27	DQ0_L0
BANKL0	DIFFIO_L0_2_P/VAUX7	F5	35.98	DQ0_L0
BANKL0	DIFFIO_L0_2_N/VAUX6	G5	37.52	DQ0_L0
BANKL0	DIFFIO_L0_3_P/IO_STATUS_C	B8	115.38	DQ0_L0
BANKL0	DIFFIO_L0_3_N/CFG_CLK	A8	109.71	DQ0_L0
BANKL0	DIFFIO_L0_4_P/FCS_N	D10	109.97	DQS0_L0
BANKL0	DIFFIO_L0_4_N/CS_N	C10	108.67	DQS0#_L0
BANKL0	DIFFIO_L0_5_P/MODE_0	B7	116.79	DQ0_L0
BANKL0	DIFFIO_L0_5_N/MODE_1	A7	115.74	DQ0_L0
BANKL0	DIFFIO_L0_6_P/MODE_2	B10	114.22	DQ0_L0
BANKL0	DIFFIO_L0_6_N/VREF_L0/CSO_DOUT	A10	110.05	DQ0_L0
BANKL0	DIFFIO_L0_7_P/RWSEL	B6	114.38	DQ1_L0
BANKL0	DIFFIO_L0_7_N/INIT_FLAG_N	A6	118.27	DQ1_L0
BANKL0	DIFFIO_L0_8_P/PLL0_CLKOUT_P	D7	81.75	DQ1_L0
BANKL0	DIFFIO_L0_8_N/PLL0_CLKOUT_N	C7	72.1	DQ1_L0
BANKL0	DIFFIO_L0_9_P/CLK0_L0/DIFFCLK0_L0_P/PLL0_CLKFB_P/XTALA_L0	B5	111.73	DQ1_L0
BANKL0	DIFFIO_L0_9_N/CLK1_L0/DIFFCLK0_L0_N/PLL0_CLKFB_N/XTALB_L0	A5	104.32	DQ1_L0
BANKL0	DIFFIO_L0_10_P/CLK2_L0/DIFFCLK1_L0_P/PLL1_CLKIN0	B4	111.22	DQS1_L0
BANKL0	DIFFIO_L0_10_N/CLK3_L0/DIFFCLK1_L0_N/PLL1_CLKIN1	A4	105.36	DQS1#_L0

Bank Name	Ball Name (Function Name)	Ball Number	Time Delay (ps)	DQS Group
BANKL0	DIFFIO_L0_11_P/PLL1_CLKIN2	B9	120.55	DQ1_L0
BANKL0	DIFFIO_L0_11_N/PLL1_CLKIN3	A9	115.77	DQ1_L0
BANKL0	DIFFIO_L0_12_P/D0	B3	109.32	DQ1_L0
BANKL0	DIFFIO_L0_12_N/RRN_L0/D1	A3	102.25	DQ1_L0
BANKL0	DIFFIO_L0_13_P/RRP_L0/D2	D5	72.89	DQ2_L0
BANKL0	DIFFIO_L0_13_N/D3	D6	75.17	DQ2_L0
BANKL0	DIFFIO_L0_14_P/D4	B2	110.59	DQ2_L0
BANKL0	DIFFIO_L0_14_N/D5	A2	114.69	DQ2_L0
BANKL0	DIFFIO_L0_15_P/D6	D4	75.22	DQS2_L0
BANKL0	DIFFIO_L0_15_N/D7	C4	72.53	DQS2#_L0
BANKL0	DIFFIO_L0_16_P/D8	B1	113.29	DQ2_L0
BANKL0	DIFFIO_L0_16_N/D9	A1	116.05	DQ2_L0
BANKL0	DIFFIO_L0_17_P/D10	E4	65.74	DQ2_L0
BANKL0	DIFFIO_L0_17_N/D11	E3	70.64	DQ2_L0
BANKL0	DIFFIO_L0_18_P/D12	C1	115.28	DQ2_L0
BANKL0	DIFFIO_L0_18_N/D13	C2	119.18	DQ2_L0
BANKL0	DIFFIO_L0_19_P/D14	F4	60.25	DQ2_L0
BANKL0	DIFFIO_L0_19_N/D15	F3	60.61	DQ2_L0
BANKL1	DIFFIO_L1_0_P	K3	53.67	DQ0_L1
BANKL1	DIFFIO_L1_0_N	L3	53.94	DQ0_L1
BANKL1	DIFFIO_L1_1_P	K1	65.74	DQ0_L1
BANKL1	DIFFIO_L1_1_N	K2	68.15	DQ0_L1
BANKL1	DIFFIO_L1_2_P	J6	41.68	DQ0_L1
BANKL1	DIFFIO_L1_2_N	K6	42.37	DQ0_L1
BANKL1	DIFFIO_L1_3_P	L1	75.39	DQ0_L1
BANKL1	DIFFIO_L1_3_N	L2	73.4	DQ0_L1
BANKL1	DIFFIO_L1_4_P	M1	82.35	DQS0_L1
BANKL1	DIFFIO_L1_4_N	M2	79.37	DQS0#_L1
BANKL1	DIFFIO_L1_5_P	K4	110.29	DQ0_L1
BANKL1	DIFFIO_L1_5_N	L4	106.23	DQ0_L1
BANKL1	DIFFIO_L1_6_P	K5	42.81	DQ0_L1
BANKL1	DIFFIO_L1_6_N/VREF_L1	L5	42.07	DQ0_L1
BANKL1	DIFFIO_L1_7_P	N1	96.25	DQ1_L1
BANKL1	DIFFIO_L1_7_N	N2	98.39	DQ1_L1
BANKL1	DIFFIO_L1_8_P/PLL2_CLKOUT_P	R3	90.78	DQ1_L1
BANKL1	DIFFIO_L1_8_N/PLL2_CLKOUT_N	T3	90.27	DQ1_L1
BANKL1	DIFFIO_L1_9_P/CLK0_L1/DIFFCLK0_L1_P/PLL2_CLKFB_P/XTALA_L1	P1	99.46	DQ1_L1
BANKL1	DIFFIO_L1_9_N/CLK1_L1/DIFFCL	P2	103.68	DQ1_L1

Bank Name	Ball Name (Function Name)	Ball Number	Time Delay (ps)	DQS Group
	K0_L1_N/PLL2_CLKFB_N/XTALB_L1			
BANKL1	DIFFIO_L1_10_P/CLK2_L1/DIFFCLK1_L1_P/PLL3_CLKIN0	R1	102.58	DQS1_L1
BANKL1	DIFFIO_L1_10_N/CLK3_L1/DIFFCLK1_L1_N/PLL3_CLKIN1	R2	105.1	DQS1#_L1
BANKL1	DIFFIO_L1_11_P/PLL3_CLKIN2	N3	69.43	DQ1_L1
BANKL1	DIFFIO_L1_11_N/PLL3_CLKIN3	N4	70.21	DQ1_L1
BANKL1	DIFFIO_L1_12_P	T1	93.28	DQ1_L1
BANKL1	DIFFIO_L1_12_N/RRN_L1	T2	93.62	DQ1_L1
BANKL1	DIFFIO_L1_13_P/RRP_L1	R7	81.5	DQ2_L1
BANKL1	DIFFIO_L1_13_N	T7	91.65	DQ2_L1
BANKL1	DIFFIO_L1_14_P	R4	113.21	DQ2_L1
BANKL1	DIFFIO_L1_14_N	T4	109.87	DQ2_L1
BANKL1	DIFFIO_L1_15_P	P5	66.4	DQS2_L1
BANKL1	DIFFIO_L1_15_N	P6	65.3	DQS2#_L1
BANKL1	DIFFIO_L1_16_P	R5	114.65	DQ2_L1
BANKL1	DIFFIO_L1_16_N	T5	112.82	DQ2_L1
BANKL1	DIFFIO_L1_17_P	R8	76.05	DQ2_L1
BANKL1	DIFFIO_L1_17_N	T8	87.32	DQ2_L1
BANKL1	DIFFIO_L1_18_P	R6	117.78	DQ2_L1
BANKL1	DIFFIO_L1_18_N	T6	113.92	DQ2_L1
BANKL1	DIFFIO_L1_19_P	N5	45.56	DQ2_L1
BANKL1	DIFFIO_L1_19_N	M5	45.73	DQ2_L1
BANKR0	DIFFIO_R0_0_P/VAUX5	D11	42.81	DQ0_R0
BANKR0	DIFFIO_R0_0_N/VAUX4	C11	45.18	DQ0_R0
BANKR0	DIFFIO_R0_1_P/VAUX3	B13	74.39	DQ0_R0
BANKR0	DIFFIO_R0_1_N/VAUX2	A13	80.09	DQ0_R0
BANKR0	DIFFIO_R0_2_P/VAUX1	B11	69.33	DQ0_R0
BANKR0	DIFFIO_R0_2_N/VAUX0	A11	74.19	DQ0_R0
BANKR0	DIFFIO_R0_3_P	F13	75.15	DQ0_R0
BANKR0	DIFFIO_R0_3_N/ECCLKIN	E13	71.87	DQ0_R0
BANKR0	DIFFIO_R0_4_P/FCS2_N	B12	75.49	DQS0_R0
BANKR0	DIFFIO_R0_4_N/BFCE_N	A12	65.96	DQS0#_R0
BANKR0	DIFFIO_R0_5_P/BFOE_N	G11	95.89	DQ0_R0
BANKR0	DIFFIO_R0_5_N/BADRVO_N	G10	98.67	DQ0_R0
BANKR0	DIFFIO_R0_6_P/BFWE_N	C16	85.57	DQ0_R0
BANKR0	DIFFIO_R0_6_N/VREF_R0	C15	85.55	DQ0_R0
BANKR0	DIFFIO_R0_7_P/VS1	B14	80.67	DQ1_R0
BANKR0	DIFFIO_R0_7_N/VS0	A14	98.01	DQ1_R0
BANKR0	DIFFIO_R0_8_P/PLL0_CLKIN0	D13	73.42	DQ1_R0

Bank Name	Ball Name (Function Name)	Ball Number	Time Delay (ps)	DQS Group
BANKR0	DIFFIO_R0_8_N/PLL0_CLKIN1	C13	72.95	DQ1_R0
BANKR0	DIFFIO_R0_9_P/CLK0_R0/DIFFCLK0_R0_P/PLL0_CLKIN2/XTALA_R0	B15	99.29	DQ1_R0
BANKR0	DIFFIO_R0_9_N/CLK1_R0/DIFFCLK0_R0_N/PLL0_CLKIN3/XTALB_R0	A15	89.57	DQ1_R0
BANKR0	DIFFIO_R0_10_P/CLK2_R0/DIFFCLK1_R0_P/PLL1_CLKFB_P	B16	96.75	DQS1_R0
BANKR0	DIFFIO_R0_10_N/CLK3_R0/DIFFCLK1_R0_N/PLL1_CLKFB_N	A16	92.44	DQS1#_R0
BANKR0	DIFFIO_R0_11_P/PLL1_CLKOUT_P	E10	61.97	DQ1_R0
BANKR0	DIFFIO_R0_11_N/PLL1_CLKOUT_N	F10	61.49	DQ1_R0
BANKR0	DIFFIO_R0_12_P/D16/ADR0	E16	83.76	DQ1_R0
BANKR0	DIFFIO_R0_12_N/RRN_R0/D17/ADR1	E15	85.09	DQ1_R0
BANKR0	DIFFIO_R0_13_P/RRP_R0/D18/ADR2	H13	44.31	DQ2_R0
BANKR0	DIFFIO_R0_13_N/D19/ADR3	H14	45.73	DQ2_R0
BANKR0	DIFFIO_R0_14_P/D20/ADR4	F16	74.28	DQ2_R0
BANKR0	DIFFIO_R0_14_N/D21/ADR5	F15	77.86	DQ2_R0
BANKR0	DIFFIO_R0_15_P/D22/ADR6	J14	48.59	DQS2_R0
BANKR0	DIFFIO_R0_15_N/D23/ADR7	J13	48.76	DQS2#_R0
BANKR0	DIFFIO_R0_16_P/D24/ADR8	G16	52.43	DQ2_R0
BANKR0	DIFFIO_R0_16_N/D25/ADR9	G15	58.29	DQ2_R0
BANKR0	DIFFIO_R0_17_P/D26/ADR10	H10	59.05	DQ2_R0
BANKR0	DIFFIO_R0_17_N/D27/ADR11	J10	59.68	DQ2_R0
BANKR0	DIFFIO_R0_18_P/D28/ADR12	H16	62.44	DQ2_R0
BANKR0	DIFFIO_R0_18_N/D29/ADR13	H15	61.27	DQ2_R0
BANKR0	DIFFIO_R0_19_P/D30/ADR14	J12	53.79	DQ2_R0
BANKR0	DIFFIO_R0_19_N/D31/ADR15	J11	55.95	DQ2_R0
BANKR1	DIFFIO_R1_0_P/ADR16	K14	53.03	DQ0_R1
BANKR1	DIFFIO_R1_0_N	K13	54.42	DQ0_R1
BANKR1	DIFFIO_R1_1_P/ADR17	J16	68.24	DQ0_R1
BANKR1	DIFFIO_R1_1_N/ADR18	J15	68.22	DQ0_R1
BANKR1	DIFFIO_R1_2_P/ADR19	K11	48.06	DQ0_R1
BANKR1	DIFFIO_R1_2_N/ADR20	K12	46.28	DQ0_R1
BANKR1	DIFFIO_R1_3_P/ADR21	K16	72.63	DQ0_R1
BANKR1	DIFFIO_R1_3_N/ADR22	K15	67.51	DQ0_R1
BANKR1	DIFFIO_R1_4_P/ADR23	L15	74.43	DQS0_R1
BANKR1	DIFFIO_R1_4_N/ADR24	L16	73.94	DQS0#_R1
BANKR1	DIFFIO_R1_5_P/ADR25	L11	95.42	DQ0_R1
BANKR1	DIFFIO_R1_5_N	L12	91.66	DQ0_R1

Bank Name	Ball Name (Function Name)	Ball Number	Time Delay (ps)	DQS Group
BANKR1	DIFFIO_R1_6_P	L14	61.75	DQ0_R1
BANKR1	DIFFIO_R1_6_N/VREF_R1	L13	58.85	DQ0_R1
BANKR1	DIFFIO_R1_7_P	M16	95.71	DQ1_R1
BANKR1	DIFFIO_R1_7_N	M15	99.53	DQ1_R1
BANKR1	DIFFIO_R1_8_P/PLL2_CLKIN0	N13	71.24	DQ1_R1
BANKR1	DIFFIO_R1_8_N/PLL2_CLKIN1	P13	71.84	DQ1_R1
BANKR1	DIFFIO_R1_9_P/CLK0_R1/DIFFCLK0_R1_P/PLL2_CLKIN2/XTALA_R1	N16	99.02	DQ1_R1
BANKR1	DIFFIO_R1_9_N/CLK1_R1/DIFFCLK0_R1_N/PLL2_CLKIN3/XTALB_R1	N15	96.77	DQ1_R1
BANKR1	DIFFIO_R1_10_P/CLK2_R1/DIFFCLK1_R1_P/PLL3_CLKFB_P	P16	105.31	DQS1_R1
BANKR1	DIFFIO_R1_10_N/CLK3_R1/DIFFCLK1_R1_N/PLL3_CLKFB_N	P15	105.47	DQS1#_R1
BANKR1	DIFFIO_R1_11_P/PLL3_CLKOUT_P	R15	106.29	DQ1_R1
BANKR1	DIFFIO_R1_11_N/PLL3_CLKOUT_N	R16	109.36	DQ1_R1
BANKR1	DIFFIO_R1_12_P	T16	106.57	DQ1_R1
BANKR1	DIFFIO_R1_12_N/RRN_R1	T15	105.2	DQ1_R1
BANKR1	DIFFIO_R1_13_P/RRP_R1	R11	75.56	DQ2_R1
BANKR1	DIFFIO_R1_13_N	T11	88.38	DQ2_R1
BANKR1	DIFFIO_R1_14_P	R14	104.17	DQ2_R1
BANKR1	DIFFIO_R1_14_N	T14	107	DQ2_R1
BANKR1	DIFFIO_R1_15_P	R10	73	DQS2_R1
BANKR1	DIFFIO_R1_15_N	T10	88.57	DQS2#_R1
BANKR1	DIFFIO_R1_16_P	R13	101.03	DQ2_R1
BANKR1	DIFFIO_R1_16_N	T13	102.25	DQ2_R1
BANKR1	DIFFIO_R1_17_P	R9	88.02	DQ2_R1
BANKR1	DIFFIO_R1_17_N	T9	92.02	DQ2_R1
BANKR1	DIFFIO_R1_18_P	R12	92.17	DQ2_R1
BANKR1	DIFFIO_R1_18_N	T12	102.74	DQ2_R1
BANKR1	DIFFIO_R1_19_P	N12	39.38	DQ2_R1
BANKR1	DIFFIO_R1_19_N	N11	45.72	DQ2_R1
	VDDIOL0	C3		
	VDDIOL0	C5		
	VDDIOCFG	C8		
	VDDIOR0	D12		
	VDDIOR0	D14		
	VDDIOL0	E5		
	VDDEFUSE	E9		
	VCC	E11		

Bank Name	Ball Name (Function Name)	Ball Number	Time Delay (ps)	DQS Group
	VCC	F7		
	VCCAUX_A	F9		
	VDDIOR0	F11		
	VCC	F14		
	VCC	G8		
	VCC	G14		
	VDDIOL0	H5		
	VDDIOL0	H7		
	VDDIOR0	H11		
	VCCAUX	K10		
	VCCAUX	L7		
	VCCAUX	L9		
	VDDIOL1	M4		
	VDDIOL1	M6		
	VCC	M7		
	VCCAUX	M8		
	VCC	M9		
	VCCAUX	M10		
	VDDIOR1	M12		
	VCC	M14		
	VCC	N8		
	VCC	N10		
	VDDIOR1	N14		
	VDDIOL1	P4		
	VCC	P7		
	VCC	P9		
	VDDIOR1	P12		
	VSS	C6		
	VSS	C9		
	VSS	C12		
	VSS	C14		
	VSS	D3		
	VSS	E6		
	VSS	F12		
	VSS	G7		
	VSSA	G9		
	VSS	H12		
	VSS	J5		
	VSS	L6		

Bank Name	Ball Name (Function Name)	Ball Number	Time Delay (ps)	DQS Group
	VSS	L8		
	VSS	L10		
	VSS	M3		
	VSS	M11		
	VSS	M13		
	VSS	N6		
	VSS	N7		
	VSS	N9		
	VSS	P3		
	VSS	P8		
	VSS	P10		
	VSS	P11		
	VSS	P14		
	NC	D1		
	NC	D2		
	NC	D15		
	NC	D16		
	NC	E1		
	NC	E2		
	NC	E12		
	NC	E14		
	NC	F1		
	NC	F2		
	NC	G1		
	NC	G2		
	NC	G3		
	NC	G4		
	NC	G12		
	NC	G13		
	NC	H1		
	NC	H2		
	NC	H3		
	NC	H4		
	NC	J1		
	NC	J2		
	NC	J3		
	NC	J4		
	NC	J7		
	NC	K7		

2.2.5 Thermal Resistance

Table 2-4 Thermal Resistance Values

θJA(°C/W) (Flow: 0m/s)	**θJB (°C/W)**	**θJC (°C/W)**	**θJA(°C/W) (Flow: 1m/s)**	**θJA(°C/W) (Flow: 2m/s)**
30.7	22.6	14.5	27	25.9

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