PK02006_PGL25G_FBG256

(V1.5)

(28.01.2021)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.5	28.01.2021	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

PGL25G_FBG256 uses a Wire-Bond BGA type of packaging. Package size: 17x17mm; Number of balls: 256; Ball pitch: 1.0mm; Maximum package thickness: 1.43mm

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Values

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	1.23	1.33	1.43	c	0.22	0.26	0.30
A1	0.32	0.37	0.42	e	-	1.0	-
A2	0.91	0.96	1.01	b	0.45	0.50	0.55
D	16.9	17.0	17.1	aaa	-	-	0.20
E	16.9	17.0	17.1	bbb	-	-	0.25
D1	-	15.0	-	ddd	-	-	0.20
E1	-	15.0	-	eee	-	-	0.25

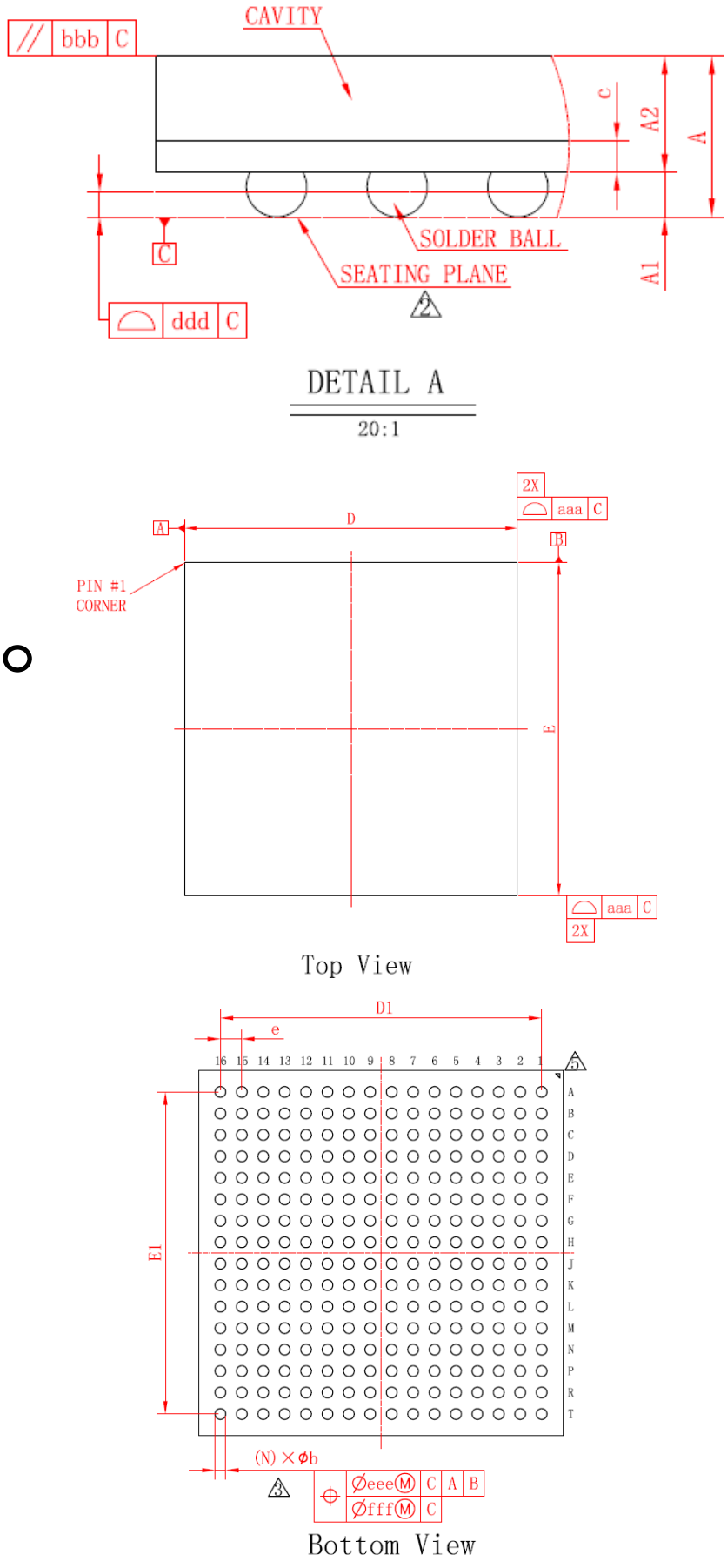

Figure 2-1 Package Outline Dimension (POD)

Pin #1 is the pin 1 position of the pin

2.2 Pin Description

PGL25G_FBG256 has 186 user IOs.

Table 2-2 Product Pin Definitions

PIN name	PIN type	PIN description
General PIN		
IO	I/O	**General** IO Before or during configuration, when IO_STATUS_C=0, enable internal pull-up; when IO_STATUS_C=1, disable internal pull-up In user mode, unused IOs default to pull-down, but can also be configured by the user as pull-up, pull-down, or float via bitstream
-- Multi-function Configuration Pin		
MODE_1	input	Multi-function configuration input pin, used for selecting between master and slave configuration modes; MODE_1=0,master mode; MODE_1=1,slave mode
MODE_0	input	Multi-function configuration input PAD, used for selecting between parallel and serial configuration modes MODE_0=0 parallel configuration; MODE_0=1 serial configuration
INIT_FLAG_N	Bidirectional (open-drain)	When it is low, it indicates that the FPGA's internal CRAM is being cleared, and this pin will be released by internal control upon completion. If this pin is pulled low externally, it will delay the configuration process If this pin is low during configuration, it indicates an internal configuration error occurred
CFG_CLK	inpu, output	Configuration clock pin. In the slave mode, this pin serves as a clock input to obtain configuration data from external sources; In the master mode, this pin serves as a clock output to obtain configuration data from external sources; When the clock is not needed (such as in the JTAG mode), this pin is high-z.
ECCLK	input	Optional external configuration clock input pin in the master mode
CS_N	inpu, output	Multi-function configuration pin. (1) In the Slave Parallel configuration mode, this pin enables the parallel configuration mode data interface at a low level; (2) In the SPI x1 mode, when this pin is connected to the Slave Data input interface of the SPI Flash, FPGA will send instructions and initial address to the SPI Flash; (3) In the SPI x2 and x4 modes, it is connected to the SPI flash's IO0 as the [0]th bit of the data bus.
CSO_N	output	Multi-function configuration pin (1) In the slave parallel configuration mode, it serves as the cascaded chip select signal output (2) In the master SPI mode, it serves as the chip select signal output
D0	input	Multi-function configuration pin (1) In the SPI x1 mode, this pin connects to the Slave Data output interface of the SPI Flash, and FPGA receives serial data from the SPI Flash, i.e., Master Input/Slave Output

PIN name	PIN type	PIN description
		(2) In the SPI x2 and x4 modes, this pin also serves as the [1]st bit of the SPI data bus. (3) In the parallel or BPI mode, this pin serves as the lowest bit of the data bus (4) In the Slave Serial mode, this pin serves as data input
D[1,2]	inpu, output	Multi-function configuration pin (1) In the SPI x2 and x4 modes, pin D[1] serves as the [2]nd bit connected to SPI flash's IO2, pin D[2] as the [3]rd bit connected to SPI flash's IO3.; (2) In the slave parallel or BPI mode, this pin serves as the [2:1] bits of the data bus.
D[3, 4, 5…15]	inpu, output	Multi-function configuration data pad In the Slave Parallel or BPI mode with x8 width, D[7:3] serves as the [7:3]th bit of the data bus; In the slave Parallel or BPI mode with x16 width, D[15:3] serves as the [15:3]th bit of the data bus.
RWSEL	input	Multi-function configuration pin. For selecting the read/write input in the Slave Parallel configuration mode (high for read and low for write). (1) When it is high, the Slave Parallel configuration mode reads data from the data bus; (2) When it is low, the Slave Parallel configuration mode writes data to the data bus; (3) Read and write can be switched only when CS_N is high.
DOUT_BUSY	output	Multi-function configuration pin. (1) During readback in the slave parallel mode, this pin indicates the device status; It indicates the data read from the bus is invalid when high. (2) In the serial configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK (3) In the SPI configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK.
IO_STATUS_C	input	Multi-function input pin; used for controlling whether the pull-up resistors for all user IOs are enabled during the configuration process. (1) When the signal is 0, the internal IO pull-up resistors, for user IOs, are enabled before or during configuration; (2) When the signal is 1, the internal IO pull-up resistors, for user IOs, are disable before or during configuration;
ADR[0, 1, …, 25]	output	Multi-function configuration pin, used for outputting addresses in the BPI configuration mode; (1) After configuration is completed, it can be used as a user IO
BFWE_N	output	Multi-function configuration pin, used for providing a low-level write enable signal for parallel NOR FLASH in the BPI configuration mode.
BFOE_N	output	Multi-function configuration pin, used for providing a low-level output enable signal for parallel NOR FLASH in the BPI configuration mode.
BFCE_N	output	Multi-function configuration pin, used for providing a low-level chip select control signal for parallel NOR FLASH in the BPI configuration mode；
BHDC	output	In BPI mode, there is high output during the configuration

PIN name	PIN type	PIN description
BLDC	output	In BPI mode, there is low output during the configuration
-- Clock, PLL, Oscillator Multi-function Pin		
GCLK[0,1,2,3…,30,31]	input	Dedicated Global Clock Input pin. Can also serve as a general user I/O, 8 PADs for each bank When serves as differential clock input, GCLK[1,3,5,…,27,29,31] are the internal valid input
PLL[0,1,2,3]_CLK[0,1,2,…,13,14,15]	input	Optional PLL reference clock input, PLL can directly input a clock from these pins; Optional PLL feedback clock input, PLL can externally feedback the clock from these pins.; Can also be used as general user I/Os.
--Differential Pin		
DIFFIO_[0,1,2,3]_[0…n][N,P]	I/O, true differential input/output	Transmitting and receiving differential signals. Used for transmitting and receiving LVDS signals. The suffix "P" indicates the "positive" signal and the suffix "N" indicates the "negative" signal. If not used as differential signal pins, these pins can serve as general user I/Os. Each IOBD tile is provided with a pair of differential signals.
DIFFI_[0,1,2,3]_[0…n]_[N,P]	I/O, true differential input	Differential signal receive pin. Can be used for receiving differential input signals. The suffix "P" indicates the "positive" signal and the suffix "N" indicates the "negative" signal. If not used as differential input pins, these pins can be used as general user I/Os; each IOBS tile is provided with a pair of differential inputs.
-- External Memory Interface Pin		
DQS[0,1,2,3,4,5][#]_[1,3]	DQS	Multi-function pin. Used to connect to the DQS/DQS# signal pins of external memory. Also used as general user I/Os.
DQ[0,1,2,3,4,5][#]_[1,3]	DQ	Multi-function pin, can connect to the DQ signal pins of external memory. Also used as general user I/Os.
Dedicated Pin		
--Configuration Pin, JTAG Pin		
CFG_DONE	Bidirectional (open-drain)	Dedicated pin for configuration state. Serves as a status output, driven low before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.
RST_N	input	Dedicated configuration input pin, internally weak pull-up, for restarting the configuration process, active-low. It is recommended that users externally pull up the RST_N with a resistor when using this pin. When this pin is low, the FPGA enters a reset state, and all IOs are in the High-z state.
CMPCS_B		No need to be connected, left floating
STAND_BY		No need to be connected, left floating
TCK	input	Dedicated JTAG test clock input pin
TMS	input	Dedicated JTAG test mode selection input pin
TDI	input	Dedicated JTAG test data input pin.
TDO	output	Dedicated JTAG test data output pin.
--Reference Pin		
VREF_[B0,B1,B2,B3]	input	External reference voltage pin, one for each bank. Provide reference voltage input for each BANK

PIN name	PIN type	PIN description
		When a VREF is used, all VREFs in that bank must be connected
Power Pin, Ground Pin		
VCC	POWER	Core power supply, 1.2V. Power supply for core logic
VCCAUX	POWER	3.3V auxiliary power supply for IOB, LDO, EFUSE, dedicated configuration IOB, and other modules
VCCIO[0,1,2,3]	POWER	IO BANK power
VSS	GROUND	GND relative to VCC & VCCAUX & VCCIO

2.2.1 Pin Name list

Table 2-3 Pin Name List

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B0	DIFFIO_B0_0P/IO_STATUS_C	C4	IO_1_P	63.6272	
B0	DIFFIO_B0_0N/VREF_B0	A4	IO_1_N	69.3802	
B0	DIFFIO_B0_1P	B5	IO_2_P	61.7613	
B0	DIFFIO_B0_1N	A5	IO_2_N	64.2707	
B0	DIFFIO_B0_2P	D5	IO_3_P	60.3003	
B0	DIFFIO_B0_2N	C5	IO_3_N	65.3794	
B0	DIFFIO_B0_3P	B6	IO_4_P	59.5118	
B0	DIFFIO_B0_3N	A6	IO_4_N	61.7158	
B0	DIFFIO_B0_4P	F7	IO_5_P	65.5907	
B0	DIFFIO_B0_4N	E6	IO_5_N	67.7429	
B0	DIFFIO_B0_5P	C7	IO_6_P	60.0543	
B0	DIFFIO_B0_5N	A7	IO_6_N	61.3401	
B0	DIFFIO_B0_6P	D6	IO_7_P	38.7126	
B0	DIFFIO_B0_6N	C6	IO_7_N	39.2564	
B0	DIFFIO_B0_14P	B8	IO_15_P	51.6305	
B0	DIFFIO_B0_14N	A8	IO_15_N	55.7962	
B0	DIFFIO_B0_15P/GCLK19/PLL0_CLK0/PLL1_CLK0	C9	IO_16_P	50.5437	
B0	DIFFIO_B0_15N/GCLK18/PLL0_CLK1/PLL1_CLK1	A9	IO_16_N	56.3094	
B0	DIFFIO_B0_16P/GCLK17/PLL0_CLK2/PLL1_CLK2	B10	IO_17_P	65.5979	
B0	DIFFIO_B0_16N/GCLK16/PLL0_CLK3/PLL1_CLK3	A10	IO_17_N	62.2796	
B0	DIFFIO_B0_17P/GCLK15/PLL0_CLK4/PLL1_CLK4	E7	IO_18_P	52.1098	
B0	DIFFIO_B0_17N/GCLK14/PLL0_CLK5/PLL1_CLK5	E8	IO_18_N	52.8164	
B0	DIFFIO_B0_18P/GCLK13/PLL0_CLK6/PLL1_CLK6	E10	IO_19_P	55.4503	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B0	DIFFIO_B0_18N/GCLK12/PLL0_CLK7/PLL1_CLK7	C10	IO_19_N	55.1716	
B0	DIFFIO_B0_19P	D8	IO_20_P	44.1528	
B0	DIFFIO_B0_19N/VREF_B0	C8	IO_20_N	46.8833	
B0	DIFFIO_B0_20P	C11	IO_21_P	56.3915	
B0	DIFFIO_B0_20N	A11	IO_21_N	59.7296	
B0	DIFFIO_B0_21P	F9	IO_22_P	45.189	
B0	DIFFIO_B0_21N	D9	IO_22_N	43.1743	
B0	DIFFIO_B0_29P	B12	IO_30_P	60.9184	
B0	DIFFIO_B0_29N/VREF_B0	A12	IO_30_N	62.3858	
B0	DIFFIO_B0_30P	C13	IO_31_P	76.0738	
B0	DIFFIO_B0_30N	A13	IO_31_N	77.9573	
B0	DIFFIO_B0_31P	F10	IO_32_P	57.3666	
B0	DIFFIO_B0_31N	E11	IO_32_N	57.2642	
B0	DIFFIO_B0_32P	B14	IO_33_P	71.0875	
B0	DIFFIO_B0_32N	A14	IO_33_N	74.6817	
B0	DIFFIO_B0_33P	D11	IO_34_P	37.48	
B0	DIFFIO_B0_33N	D12	IO_34_N	36.7031	
B1	DIFFI_B1_0P/ADR25	E13	IO_35_P	40.5724	DQ0_B1
B1	DIFFI_B1_0N/ADR24/VREF_B1	E12	IO_35_N	41.945	DQ0_B1
B1	DIFFI_B1_7P/ADR23	B15	IO_42_P	75.1963	DQ1_B1
B1	DIFFI_B1_7N/ADR22	B16	IO_42_N	78.9927	DQ1_B1
B1	DIFFI_B1_8P/ADR21	F12	IO_43_P	58.6543	DQ1_B1
B1	DIFFI_B1_8N/ADR20	G11	IO_43_N	57.8442	DQ1_B1
B1	DIFFI_B1_9P/ADR19	D14	IO_44_P	59.3582	DQ1_B1
B1	DIFFI_B1_9N/ADR18	D16	IO_44_N	60.714	DQ1_B1
B1	DIFFI_B1_10P/ADR17	F13	IO_45_P	45.65	DQS1_B1
B1	DIFFI_B1_10N/ADR16	F14	IO_45_N	46.5235	DQS1#_B1
B1	DIFFI_B1_11P/ADR15	C15	IO_46_P	81.869	DQ1_B1
B1	DIFFI_B1_11N/ADR14	C16	IO_46_N	83.0709	DQ1_B1
B1	DIFFI_B1_12P/ADR13	E15	IO_47_P	62.1079	DQ1_B1
B1	DIFFI_B1_12N/ADR12	E16	IO_47_N	61.746	DQ1_B1
B1	DIFFI_B1_13P/ADR11	F15	IO_48_P	56.3931	DQ2_B1
B1	DIFFI_B1_13N/ADR10	F16	IO_48_N	58.9251	DQ2_B1
B1	DIFFI_B1_14P/ADR9	G14	IO_49_P	53.5101	DQ2_B1
B1	DIFFI_B1_14N/ADR8	G16	IO_49_N	59.5681	DQ2_B1
B1	DIFFI_B1_15P/ADR7	H15	IO_50_P	58.1145	DQS2_B1
B1	DIFFI_B1_15N/ADR6	H16	IO_50_N	57.5077	DQS2#_

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
					B1
B1	DIFFI_B1_16P/ADR5	G12	IO_51_P	51.6122	DQ2_B1
B1	DIFFI_B1_16N/ADR4	H11	IO_51_N	50.8986	DQ2_B1
B1	DIFFI_B1_17P	H13	IO_52_P	46.7042	DQ2_B1
B1	DIFFI_B1_17N	H14	IO_52_N	45.9745	DQ2_B1
B1	DIFFI_B1_18P/GCLK11/PLL0_CLK8/PLL1_CLK8	J11	IO_53_P	49.9124	DQ2_B1
B1	DIFFI_B1_18N/GCLK10/PLL0_CLK9/PLL1_CLK9	J12	IO_53_N	51.3025	DQ2_B1
B1	DIFFI_B1_19P/GCLK9/PLL0_CLK10/PLL1_CLK10	J13	IO_54_P	57.1087	DQ2_B1
B1	DIFFI_B1_19N/GCLK8/PLL0_CLK11/PLL1_CLK11	K14	IO_54_N	52.1757	DQ2_B1
B1	DIFFI_B1_21P/GCLK7/PLL2_CLK8/PLL3_CLK8	K12	IO_56_P	74.1592	DQ3_B1
B1	DIFFI_B1_21N/GCLK6/PLL2_CLK9/PLL3_CLK9	K11	IO_56_N	72.1849	DQ3_B1
B1	DIFFI_B1_22P/GCLK5/PLL2_CLK10/PLL3_CLK10	J14	IO_57_P	48.3225	DQ3_B1
B1	DIFFI_B1_22N/GCLK4/PLL2_CLK11/PLL3_CLK11	J16	IO_57_N	56.4785	DQ3_B1
B1	DIFFI_B1_23P/ADR3	K15	IO_58_P	65.6726	DQ3_B1
B1	DIFFI_B1_23N/ADR2	K16	IO_58_N	68.0829	DQ3_B1
B1	DIFFI_B1_24P/ADR1	N14	IO_59_P	98.1297	DQS3_B1
B1	DIFFI_B1_24N/ADR0	N16	IO_59_N	96.0386	DQS3#_B1
B1	DIFFI_B1_25P/BFCE_N	M15	IO_60_P	82.4338	DQ3_B1
B1	DIFFI_B1_25N/BFOE_N	M16	IO_60_N	78.8844	DQ3_B1
B1	DIFFI_B1_26P/BFWE_N	L14	IO_61_P	53.1288	DQ3_B1
B1	DIFFI_B1_26N/BLDC	L16	IO_61_N	55.0556	DQ3_B1
B1	DIFFI_B1_28P/BHDC	P15	IO_63_P	83.4093	DQ4_B1
B1	DIFFI_B1_28N	P16	IO_63_N	83.0448	DQ4_B1
B1	DIFFI_B1_29P	R15	IO_64_P	86.0575	DQ4_B1
B1	DIFFI_B1_29N	R16	IO_64_N	90.3283	DQ4_B1
B1	DIFFI_B1_30P	R14	IO_65_P	91.0569	DQS4_B1
B1	DIFFI_B1_30N	T15	IO_65_N	89.6468	DQS4#_B1
B1	DIFFI_B1_31P	T14	IO_66_P	88.5362	DQ4_B1
B1	DIFFI_B1_31N	T13	IO_66_N	91.0482	DQ4_B1
B1	DIFFI_B1_32P	R12	IO_67_P	82.0063	DQ4_B1
B1	DIFFI_B1_32N	T12	IO_67_N	83.0241	DQ4_B1
B1	DIFFI_B1_33P	L12	IO_68_P	60.2676	DQ5_B1
B1	DIFFI_B1_33N/VREF_B1	L13	IO_68_N	56.1797	DQ5_B1

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B1	DIFFI_B1_39P	M13	IO_74_P	46.0531	DQ5_B1
B1	DIFFI_B1_39N/DOUT_BUSY	M14	IO_74_N	45.4711	DQ5_B1
B2	DIFFIO_B2_0N/CSO_N	T3	IO_75_N	67.8694	
B2	DIFFIO_B2_0P/INIT_FLAG_N	R3	IO_75_P	62.7189	
B2	DIFFIO_B2_1N/D9	N6	IO_76_N	58.6889	
B2	DIFFIO_B2_1P/D8	M6	IO_76_P	55.9593	
B2	DIFFIO_B2_2N	T4	IO_77_N	65.2333	
B2	DIFFIO_B2_2P	P4	IO_77_P	63.8189	
B2	DIFFIO_B2_3N/D6	L7	IO_78_N	67.6585	
B2	DIFFIO_B2_3P/D5	L8	IO_78_P	66.38	
B2	DIFFIO_B2_11N/D4	P5	IO_86_N	59.6462	
B2	DIFFIO_B2_11P/D3	N5	IO_86_P	62.4751	
B2	DIFFIO_B2_12N/RWSEL/VREF_B2	T5	IO_87_N	63.2333	
B2	DIFFIO_B2_12P/D7	R5	IO_87_P	60.4275	
B2	DIFFIO_B2_13N	T6	IO_88_N	59.597	
B2	DIFFIO_B2_13P	P6	IO_88_P	58.8905	
B2	DIFFIO_B2_21N/GCLK28/PLL2_CLK0/PLL3_CLK0	T7	IO_96_N	63.9294	
B2	DIFFIO_B2_21P/GCLK29/PLL2_CLK1/PLL3_CLK1	R7	IO_96_P	64.0769	
B2	DIFFIO_B2_22N/GCLK30/D15/PLL2_CLK2/PLL3_CLK2	M7	IO_97_N	55.1568	
B2	DIFFIO_B2_22P/GCLK31/D14/PLL2_CLK3/PLL3_CLK3	P7	IO_97_P	53.7641	
B2	DIFFIO_B2_23N/GCLK0/ECCLK/PLL2_CLK4/PLL3_CLK4	T8	IO_98_N	56.116	
B2	DIFFIO_B2_23P/GCLK1/D13/PLL2_CLK5/PLL3_CLK5	P8	IO_98_P	56.0794	
B2	DIFFIO_B2_24N/GCLK2/PLL2_CLK6/PLL3_CLK6	N8	IO_99_N	47.3281	
B2	DIFFIO_B2_24P/GCLK3/PLL2_CLK7/PLL3_CLK7	M9	IO_99_P	44.9512	
B2	DIFFIO_B2_25N	T9	IO_100_N	54.9946	
B2	DIFFIO_B2_25P	R9	IO_100_P	51.8736	
B2	DIFFIO_B2_30N/VREF_B2	M10	IO_105_N	59.9456	
B2	DIFFIO_B2_30P	L10	IO_105_P	61.9642	
B2	DIFFIO_B2_32N/D12	P9	IO_107_N	59.9426	
B2	DIFFIO_B2_32P/D11	N9	IO_107_P	59.6504	
B2	DIFFIO_B2_33N/D10	P11	IO_108_N	47.6494	
B2	DIFFIO_B2_33P/MODE_1	N11	IO_108_P	48.1463	
B2	DIFFIO_B2_34N/D2	P12	IO_109_N	41.7925	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B2	DIFFIO_B2_34P/D1	N12	IO_109_P	40.0453	
B2	DIFFIO_B2_37N/CS_N	T10	IO_112_N	70.7513	
B2	DIFFIO_B2_37P/D0	P10	IO_112_P	71.6585	
B2	DIFFIO_B2_38N	M11	IO_113_N	47.338	
B2	DIFFIO_B2_38P	M12	IO_113_P	45.1371	
B2	DIFFIO_B2_39N/MODE_0	T11	IO_114_N	64.6032	
B2	DIFFIO_B2_39P/CFG_CLK	R11	IO_114_P	64.4691	
B3	DIFFI_B3_0N/VREF_B3	A3	IO_115_N	68.2145	DQ0_B3
B3	DIFFI_B3_0P	B3	IO_115_P	67.1404	DQ0_B3
B3	DIFFI_B3_7N	F5	IO_122_N	64.7408	DQ1_B3
B3	DIFFI_B3_7P	F6	IO_122_P	67.8629	DQ1_B3
B3	DIFFI_B3_8N	E3	IO_123_N	56.1021	DQ1_B3
B3	DIFFI_B3_8P	E4	IO_123_P	58.4643	DQ1_B3
B3	DIFFI_B3_9N	F3	IO_124_N	63.946	DQ1_B3
B3	DIFFI_B3_9P	F4	IO_124_P	69.1595	DQ1_B3
B3	DIFFI_B3_10N	A2	IO_125_N	92.8616	DQS1#_B3
B3	DIFFI_B3_10P	B2	IO_125_P	91.8529	DQS1_B3
B3	DIFFI_B3_11N	G5	IO_126_N	68.9476	DQ1_B3
B3	DIFFI_B3_11P	G6	IO_126_P	65.8976	DQ1_B3
B3	DIFFI_B3_12N	B1	IO_127_N	94.3404	DQ1_B3
B3	DIFFI_B3_12P	C1	IO_127_P	95.3764	DQ1_B3
B3	DIFFI_B3_13N	D1	IO_128_N	82.2197	DQ2_B3
B3	DIFFI_B3_13P	D3	IO_128_P	79.6253	DQ2_B3
B3	DIFFI_B3_14N	C2	IO_129_N	90.251	DQ2_B3
B3	DIFFI_B3_14P	C3	IO_129_P	85.6859	DQ2_B3
B3	DIFFI_B3_15N	K6	IO_130_N	97.1993	DQS2#_B3
B3	DIFFI_B3_15P	K5	IO_130_P	96.5088	DQS2_B3
B3	DIFFI_B3_16N	E1	IO_131_N	81.9247	DQ2_B3
B3	DIFFI_B3_16P	E2	IO_131_P	79.6269	DQ2_B3
B3	DIFFI_B3_17N	L5	IO_132_N	79.1553	DQ2_B3
B3	DIFFI_B3_17P	L4	IO_132_P	81.3047	DQ2_B3

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B3	DIFFI_B3_18N/GCLK20/PLL0_CLK12/PLL1_CLK12	H3	IO_133_N	38.0847	DQ2_B3
B3	DIFFI_B3_18P/GCLK21/PLL0_CLK13/PLL1_CLK13	H4	IO_133_P	42.067	DQ2_B3
B3	DIFFI_B3_19N/GCLK22/PLL0_CLK14/PLL1_CLK14	H5	IO_134_N	66.6815	DQ2_B3
B3	DIFFI_B3_19P/GCLK23/PLL0_CLK15/PLL1_CLK15	J6	IO_134_P	67.3116	DQ2_B3
B3	DIFFI_B3_21N/GCLK24/PLL2_CLK12/PLL3_CLK12	J4	IO_136_N	55.2573	DQ3_B3
B3	DIFFI_B3_21P/GCLK25/PLL2_CLK13/PLL3_CLK13	K3	IO_136_P	53.8529	DQ3_B3
B3	DIFFI_B3_22N/GCLK26/PLL2_CLK14/PLL3_CLK14	F1	IO_137_N	85.1896	DQ3_B3
B3	DIFFI_B3_22P/GCLK27/PLL2_CLK15/PLL3_CLK15	F2	IO_137_P	85.4792	DQ3_B3
B3	DIFFI_B3_23N	G1	IO_138_N	87.0178	DQ3_B3
B3	DIFFI_B3_23P	G3	IO_138_P	84.1806	DQ3_B3
B3	DIFFI_B3_24N	H1	IO_139_N	79.7366	DQS3#_B3
B3	DIFFI_B3_24P	H2	IO_139_P	79.613	DQS3_B3
B3	DIFFI_B3_25N	J1	IO_140_N	89.8952	DQ3_B3
B3	DIFFI_B3_25P	J3	IO_140_P	91.437	DQ3_B3
B3	DIFFI_B3_26N	K1	IO_141_N	62.3097	DQ3_B3
B3	DIFFI_B3_26P	K2	IO_141_P	61.1316	DQ3_B3
B3	DIFFI_B3_28N	L1	IO_143_N	58.6187	DQ4_B3
B3	DIFFI_B3_28P	L3	IO_143_P	54.871	DQ4_B3
B3	DIFFI_B3_29N	M1	IO_144_N	59.2322	DQ4_B3
B3	DIFFI_B3_29P	M2	IO_144_P	57.0953	DQ4_B3
B3	DIFFI_B3_30N	N1	IO_145_N	69.8354	DQS4#_B3
B3	DIFFI_B3_30P	N3	IO_145_P	64.0639	DQS4_B3
B3	DIFFI_B3_31N	P1	IO_146_N	73.2527	DQ4_B3
B3	DIFFI_B3_31P	P2	IO_146_P	70.6315	DQ4_B3
B3	DIFFI_B3_32N	R1	IO_147_N	78.8263	DQ4_B3
B3	DIFFI_B3_32P	R2	IO_147_P	79.7704	DQ4_B3
B3	DIFFI_B3_38N	N4	IO_153_N	48.7308	DQ5_B3
B3	DIFFI_B3_38P	M5	IO_153_P	48.2839	DQ5_B3
B3	DIFFI_B3_39N/VREF_B3	M3	IO_154_N	47.2565	DQ5_B3
B3	DIFFI_B3_39P	M4	IO_154_P	46.6004	DQ5_B3

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	TMS	A15			
	TDI	C12			
	TCK	C14			
	TDO	E14			
B2	CMPCS_B	L11			
B2	CFG_DONE	P13			
	STAND_BY	P14			
B2	RST_N	T2			
	VCC	G7			
	VCC	G9			
	VCC	H8			
	VCC	H10			
	VCC	J7			
	VCC	J9			
	VCC	K8			
	VCC	K10			
	VCCAUX	E5			
	VCCAUX	F8			
	VCCAUX	F11			
	VCCAUX	G10			
	VCCAUX	H6			
	VCCAUX	J10			
	VCCAUX	L6			
	VCCAUX	L9			
	VCCIO0	B4			
	VCCIO0	B9			
	VCCIO0	B13			
	VCCIO0	D7			
	VCCIO0	D10			
	VCCIO1	D15			
	VCCIO1	G13			
	VCCIO1	J15			
	VCCIO1	K13			
	VCCIO1	N15			
	VCCIO1	R13			
	VCCIO2	N7			
	VCCIO2	N10			
	VCCIO2	R4			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	VCCIO2	R8			
	VCCIO3	D2			
	VCCIO3	G4			
	VCCIO3	J2			
	VCCIO3	K4			
	VCCIO3	N2			
	VSS	A1			
	VSS	A16			
	VSS	B7			
	VSS	B11			
	VSS	D4			
	VSS	D13			
	VSS	E9			
	VSS	G2			
	VSS	G8			
	VSS	G15			
	VSS	H7			
	VSS	H9			
	VSS	H12			
	VSS	J5			
	VSS	J8			
	VSS	K7			
	VSS	K9			
	VSS	L2			
	VSS	L15			
	VSS	M8			
	VSS	N13			
	VSS	P3			
	VSS	R6			
	VSS	R10			
	VSS	T1			
	VSS	T16			

2.2.2 Thermal Resistance

Table 2-4 Thermal Resistance

θJA(°C/W) (Flow: 0m/s)	θJB (°C/W)	θJC (°C/W)	θJA(°C/W) (Flow: 1m/s)	θJA(°C/W) (Flow: 2m/s)
19.8	11.6	8.8	16.9	15.9

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